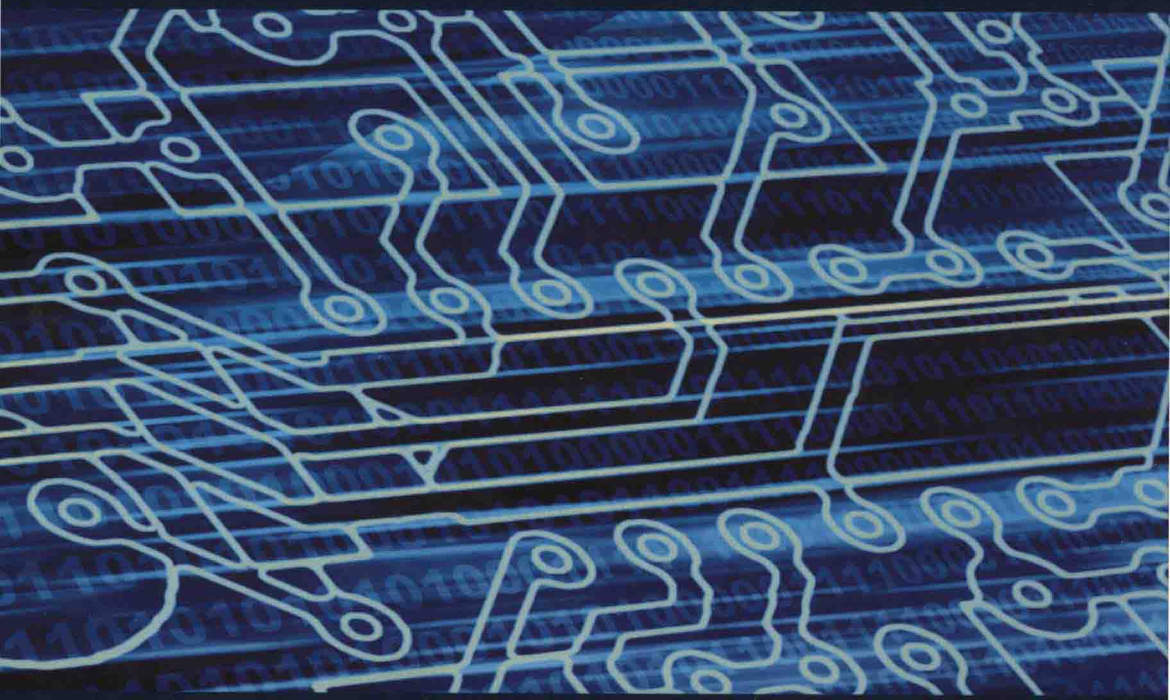
ELECTRONICS ENGINEERING SERIES

Digital Electronics 2

Sequential and Arithmetic Logic Circuits

Tertulien Ndjountche



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Digital Electronics 2

Preface

The omnipresence of electronic devices in everyday life is accompanied by the size reduction and the ever-increasing complexity of digital circuits. This comprehensive and easy-to-understand work deals with basic principles of digital electronics and allows the reader to grasp the subtleties of digital circuits from logic gates to finite-state machines. It presents all the aspects related to combinational logic and sequential logic. It introduces techniques to establish in a simple and concise manner logic equations, as well as methods for the analysis and design of digital circuits. Emphasis has been especially laid on design approaches that can be used to ensure a reliable operation of finite-state machines. Various programmable logic circuit structures and their applications are also presented. Each chapter includes practical examples and well-designed exercises with worked solutions.

This series of books discusses all the different aspects of digital electronics, following a descriptive approach combined with a gradual, detailed, and comprehensive presentation of basic concepts. The principles of combinational and sequential logic are presented, as well as the underlying techniques for the analysis and design of digital circuits. The analysis and design of digital circuits with increasing complexity is facilitated by the use of abstractions at the circuit and architecture levels. This work consists of three volumes devoted to the following subjects:

1) combinational logic circuits;

2) sequential and arithmetic logic circuits;

3) finite state machines.

A progressive approach has been chosen and the chapters are relatively independent of each other. To help master the subject matter and put into practice the different concepts and techniques, topics are complemented by a selection of exercises with solutions.

P.1. Summary

Volume 2 deals with sequential circuits and arithmetic and logic circuits. The logic state of the output of a sequential logic circuit can depend, at any given time, on the inputs but also on the previous logic state of the outputs. Depending on whether a clock signal is used to synchronize the output state change or not, a sequential circuit is said to be synchronous or asynchronous. Arithmetic circuits can be used to perform addition, subtraction, multiplication and division operations on digital data. Volume 2 contains the following seven chapters:

1) Latch and Flip-flop;

2) Binary Counters;

3) Shift Registers;

4) Arithmetic and Logic Circuits;

5) Digital Integrated Circuit Technology;

6) Semiconductor Memory;

7) Programmable Logic Circuits.

P.2. The reader

This work is an indispensable tool for all engineering students on a bachelors or masters course who wish to acquire detailed and practical knowledge of digital electronics. It is detailed enough to serve as a reference for electronic, automation and computer engineers.

Tertulien NDJOUNTCHE
June 2016

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Latch and Flip-Flop

1.1. Introduction

A latch or flip-flop is a bistable circuit that is most often used in applications that require data storage. Its chief characteristic is that the output is not dependent solely on the present state of the input but also on the preceding output state. A bistable circuit has two complementary outputs that can assume either of the two logic levels 0 or 1.

There are several common types of latches and flip-flops. Latches often have no dedicated input for the clock signal. They can be combined to implement level-triggered and edge-triggered flip-flops. Flip-flops can be triggered by one of the levels or one of the edges of a clock signal (or a digital signal).

1.2. General overview

A simple latch can be implemented using two NOR or two NAND logic gates.

A NOR gate based latch with initial conditions specified is represented in Figure 1.1(a). The characteristic equation for each of the outputs is determined by assuming that the logic gates have different propagation times[1] and this may be modeled as for a delay, Δ, between a signal that becomes available at the output and the feedback signal applied to the input. In this way, the logic circuit of the latch, as illustrated in Figure 1.1(b), may be transformed as shown in Figures 1.1(c) and 1.1(d).

1 Propagation delays in logic gates are assumed to take the form 1 and $1 + \Delta$, respectively.

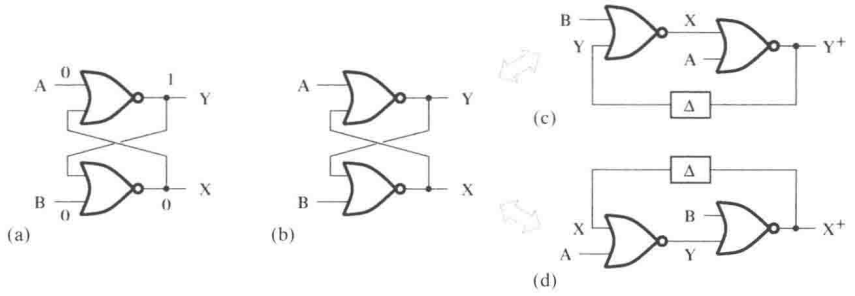

Figure 1.1. *a) NOR gate based latch with initial conditions specified; b) logic circuit for the latch and representations useful for the determination of c) Y^+ and d) X^+*

Referring to Figure 1.1(c), we can write:

$$X = \overline{B + Y} \qquad [1.1]$$

$$Y^+ = \overline{A + X} \qquad [1.2]$$

Substituting [1.1] into [1.2] yields:

$$\begin{aligned} Y^+ &= \overline{A + \overline{B + Y}} \qquad [1.3] \\ &= \overline{A} \cdot \overline{\overline{B + Y}} \\ &= \overline{A} \cdot (B + Y) \\ &= \overline{A} \cdot B + \overline{A} \cdot Y \qquad [1.4] \end{aligned}$$

Similarly, the circuit shown in Figure 1.1(d) can be characterized using the following logic equations:

$$X^+ = \overline{B + Y} \qquad [1.5]$$

$$Y = \overline{A + X} \qquad [1.6]$$

By substituting [1.5] into [1.6], we have:

$$\begin{aligned} X^+ &= \overline{B + \overline{A + X}} \qquad [1.7] \\ &= \overline{B} \cdot \overline{\overline{A + X}} \\ &= \overline{B} \cdot (A + X) \\ &= A \cdot \overline{B} + \overline{B} \cdot X \qquad [1.8] \end{aligned}$$

The characteristic equations of the NOR gate based latch are, thus, given by:

$$X^+ = A \cdot \overline{B} + \overline{B} \cdot X \qquad [1.9]$$

and

$$Y^+ = \overline{A} \cdot B + \overline{A} \cdot Y \qquad [1.10]$$

A	B	X	X^+	Y^+
0	0	0	0	1
0	0	1	1	0
0	1	0	1	0
0	1	1	1	0
1	0	0	0	1
1	0	1	0	1
1	1	0	0	0
1	1	1	0	0

Table 1.1. *State table of the NOR gate based latch*

For each output, the next state, X^+ or Y^+, depends on the present state, X or Y. In addition to the characteristic equations, the initial conditions must be specified to determine the operation of the latch. Table 1.1 gives the state table for the latch.

It must be noted that the two signals, X^+ and Y^+, are complementary except when both inputs, A and B, are set to 1.

Additionally, if the inputs A and B are simultaneously set to 0, the outputs can no longer be defined in a unique manner as the characteristic equations are verified by $(X, Y) = (1, 0)$ or by $(X, Y) = (0, 1)$. It is therefore impossible to predict the combination of the states held by the outputs.

In practice, sequential circuits are most often made to operate in the *fundamental mode*. This means that only one input can change states at any time. On the other hand, because of the difference in propagation delays between the logic gates, it is impossible to guarantee a simultaneous change in the state of two variables. Thus, the outputs of the latch are defined by $(X, Y) = (0, 1)$ when A is first set to 0 or by $(X, Y) = (1, 0)$ when B is first set to 0. In this case, the final state of the circuit is determined by the transient behavior, which depends on the order in which the state changes of the inputs take place. In general, if shifting from one state to another requires a change in at least two state variables, then a *race condition* will occur.

The race is said to be *non-critical* if the order in which the variables change state does not affect the final state of the circuit.

If, on the contrary, the circuit can assume two or more stable states depending on the order in which the variables change state, the race is said to be *critical*.

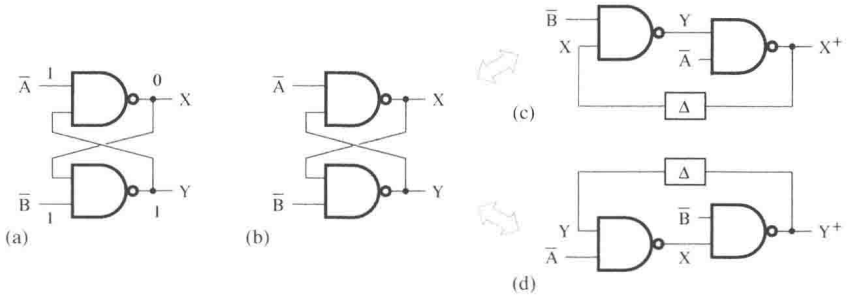

Figure 1.2. *a) NAND gate based latch with initial conditions specified; b) logic circuit of the latch and representations useful for the determination of c) X^+ and d) Y^+*

A NAND gate based latch with initial conditions specified is illustrated in Figure 1.2(a). Taking into account the fact that the differences in propagation delay of the two logic gates may translate into a delay, Δ, between an output and the feedback input, an equivalence may be established between the latch in Figure 1.2(b) and each representation shown in Figures 1.2(c) and 1.2(d).

The following logic equations may be derived based on the circuit shown in Figure 1.2(c):

$$X^+ = \overline{\overline{A} \cdot Y} \qquad [1.11]$$

$$Y = \overline{\overline{B} \cdot X} \qquad [1.12]$$

By substituting [1.12] into [1.11], we obtain:

$$X^+ = \overline{\overline{A} \cdot \overline{\overline{B} \cdot X}} \qquad [1.13]$$

$$= \overline{\overline{A}} + \overline{\overline{\overline{B} \cdot X}}$$

$$= A + \overline{B} \cdot X \qquad [1.14]$$

In the case of the circuit shown in Figure 1.2(d), the logic equations are written as follows:

$$X = \overline{\overline{A} \cdot Y} \quad [1.15]$$

$$Y^+ = \overline{\overline{B} \cdot X} \quad [1.16]$$

Substituting [1.15] into [1.16], we obtain:

$$Y^+ = \overline{\overline{B} \cdot \overline{\overline{A} \cdot Y}} \quad [1.17]$$

$$= \overline{\overline{B}} + \overline{\overline{A} \cdot Y}$$

$$= B + \overline{A} \cdot Y \quad [1.18]$$

The characteristic equations of the NAND gate based latch are therefore in the following form:

$$X^+ = A + \overline{B} \cdot X \quad [1.19]$$

and

$$Y^+ = B + \overline{A} \cdot Y \quad [1.20]$$

$\overline{A}$	$\overline{B}$	X	X^+	Y^+
1	1	1	1	0
1	1	0	0	1
1	0	1	0	1
1	0	0	0	1
0	1	1	1	0
0	1	0	1	0
0	0	1	1	1
0	0	0	1	1

Table 1.2. *State table of the NAND gate based latch*

The state table of the NAND gate based latch may be constructed, as shown in Table 1.2, based on characteristic equations and initial conditions.

We can see that the signals X^+ and Y^+ are complementary except when the two inputs $\overline{A}$ and $\overline{B}$ are set at 0.

In addition, the signals X^+ and Y^+ are only defined uniquely when the inputs $\overline{A}$ and $\overline{B}$ cannot change states from 0 to 1 simultaneously. Thus, the outputs of the latch

are defined by $(X, Y) = (0, 1)$ if the input $\overline{A}$ is first set to 1 or by $(X, Y) = (1, 0)$ if the input $\overline{B}$ is first set to 1. In this case, as the final state depends on the order in which the inputs change states, we have a critical race condition.

Among the combinations of states that the outputs of the latch can take, only those for which $X^+ = X$ and $Y^+ = Y$ are said to be *stable*.

1.2.1. *SR latch*

For the SR latch (S stands for *set*, and R for *reset*) represented in Figure 1.3, we can obtain the characteristic equations from equations [1.9] and [1.10], as follow:

$$Q^+ = \overline{R} \cdot S + \overline{R} \cdot Q = \overline{R} \cdot (S + Q) \qquad [1.21]$$

and:

$$\overline{Q^+} = \overline{S} \cdot R + \overline{S} \cdot \overline{Q} = \overline{S} \cdot (R + \overline{Q}) \qquad [1.22]$$

It must be noted that complementing Q^+ does not yield $\overline{Q^+}$. The state table is given in Table 1.3.

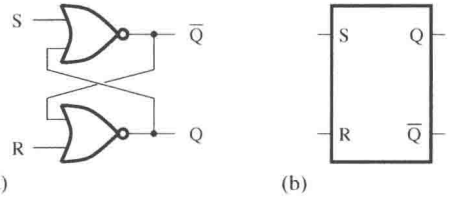

Figure 1.3. *SR latch: a) logic circuit; b) symbol*

S	R	Q	Q^+	$\overline{Q^+}$
0	0	0	0	1
0	0	1	1	0
0	1	0	0	1
0	1	1	0	1
1	0	0	1	0
1	0	1	1	0
1	1	0	*0*	*0*
1	1	1	*0*	*0*

Table 1.3. *State table of the SR latch*