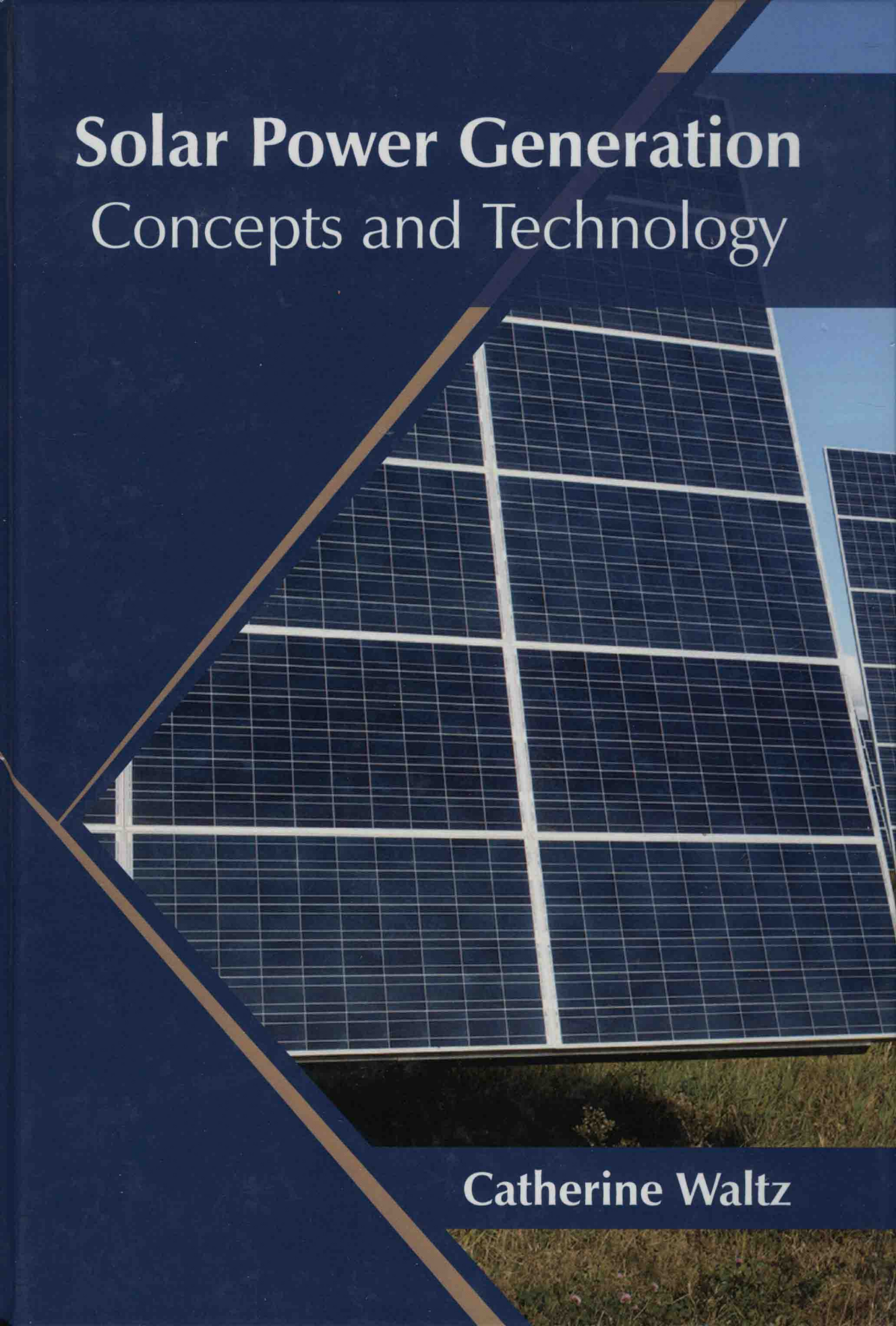
Solar Power Generation
Concepts and Technology



Catherine Waltz

Solar Power Generation: Concepts and Technology

Edited by Catherine Waltz

SYRAWOOD
PUBLISHING HOUSE
New York

Published by Syrawood Publishing House,
750 Third Avenue, 9th Floor,
New York, NY 10017, USA
www.syrawoodpublishinghouse.com

Solar Power Generation: Concepts and Technology
Edited by Catherine Waltz

International Standard Book Number: 978-1-68286-486-9 (Hardback)

Cataloging-in-Publication Data

Solar power generation : concepts and technology / edited by Catherine Waltz.
p. cm.
Includes bibliographical references and index.
ISBN 978-1-68286-486-9
1. Solar energy. 2. Photovoltaic power generation. I. Waltz, Catherine.
TJ810 .S65 2017
621.47--dc23

Printed in China.

Solar Power Generation: Concepts and Technology

PREFACE

This book was inspired by the evolution of our times; to answer the curiosity of inquisitive minds. Many developments have occurred across the globe in the recent past which has transformed the progress in the field.

Solar power generation is an important field in the area of renewable energy. The study of solar power generation concerns itself with the effective harnessing and storage of electricity that has been derived from solar power. The book on solar power generation discusses topics related to the technology of solar cells, efficient solar power harnessing and advanced technology that is being used in photovoltaic current generation. The researches included in this book aim to encapsulate the fields of solar power, solar power generation and the renewable energy generation. This book is appropriate for students seeking detailed information in this area as well as for experts. It will prove beneficial for researchers, experts and professionals engaged in the areas of environmental technology, sustainable energy engineering and energy economics.

This book was developed from a mere concept to drafts to chapters and finally compiled together as a complete text to benefit the readers across all nations. To ensure the quality of the content we instilled two significant steps in our procedure. The first was to appoint an editorial team that would verify the data and statistics provided in the book and also select the most appropriate and valuable contributions from the plentiful contributions we received from authors worldwide. The next step was to appoint an expert of the topic as the Editor-in-Chief, who would head the project and finally make the necessary amendments and modifications to make the text reader-friendly. I was then commissioned to examine all the material to present the topics in the most comprehensible and productive format.

I would like to take this opportunity to thank all the contributing authors who were supportive enough to contribute their time and knowledge to this project. I also wish to convey my regards to my family who have been extremely supportive during the entire project.

Editor

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A New Fast Peak Current Controller for Transient Voltage Faults for Power Converters

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‡ These authors contributed equally to this work.

Abstract: Power converters are the basic unit for the transient voltage fault ride through capability for most renewable distributed generators (DGs). When a transient fault happens, the grid voltage will drop suddenly and probably will also suffer a phase-jump event as well. State-of-the-art voltage fault control techniques regulate the current injected during the grid fault. However, the beginning of the fault could be too fast for the inner current control loops of the inverter, and transient over-current would be expected. In order to avoid the excessive peak current of the methods presented in the literature, a new fast peak current control (FPCC) technique is proposed. Controlling the peak current magnitude avoids undesirable disconnection of the distributed generator in a fault state and improves the life expectancy of the converter. Experimental and simulation tests with high power converters provide the detailed behaviour of the method with excellent results.

Keywords: distributed generators (DGs); voltage ride through (VRT); fast peak current control (FPCC); phase-jump ride through (PJRT); photo-voltaic (PV) systems; dip voltage

1. Introduction

Power is typically produced at a wide range of generation plants. Some years ago, for renewable power sources, it was allowed to switch off the source when a voltage fault occurred. Back then, disconnection of that power sources had little, if any, impact on the recovery capability of the electric power grid after a fault. Nowadays, a high penetration of renewable distributed generators (DGs) [1–4] has toughened the grid connection minimum technical requirements (MTRs) worldwide [5–13]. MTRs include voltage sags and phase-jump capability, frequency active power regulation and anti-islanding techniques, among others.

The voltage ride through (VRT) capability requirement has been widely described in recent grid codes [5–13]. Tables 1 and 2 point out some of the most popular MTRs for photo-voltaic (PV) plants about VRT.

First, a maximum allowed voltage profile is defined for voltage excursions. If the fault reaches the error profile, the inverter is allowed to disconnect. German legislation [5] usually is taken as the reference for other legislation. A zero-voltage transient fault is required for 0.15 s. Recent legislation imposes a zero-voltage fault, too, like the Puerto Rican or Jordanian legislation [7,13]. However, other

legislation is imposing smaller voltage sag magnitude requirements, but longer in time, for example the Chilean and Romanian grid codes [11,12].

Table 1. Minimum technical requirements (MTRs) review for voltage ride through (VRT) capabilities of photo-voltaic (PV) plants (A). German association of energy and water industries: BDEW; Puerto Rico Electric Power Authority: PREPA; National energy regulator of South Africa: NERSA; Spanish electric grid: REE.

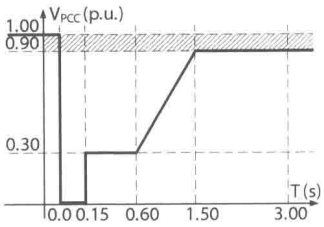
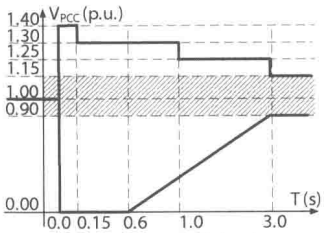
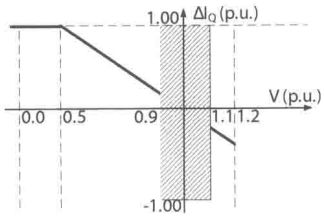
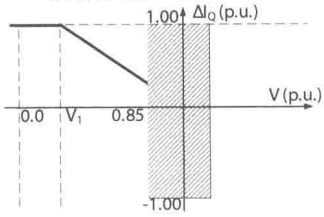
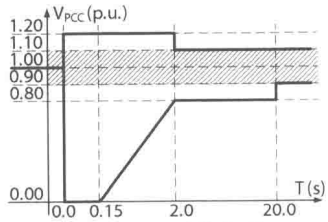
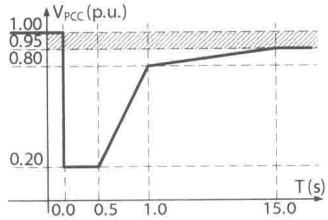
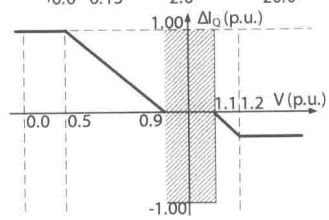
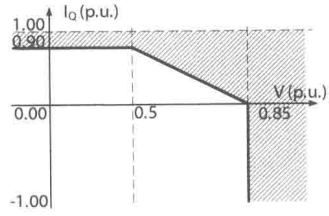
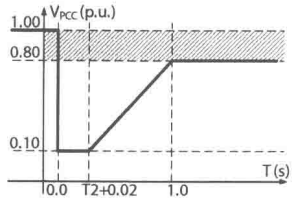
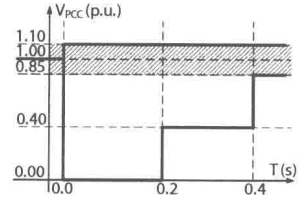
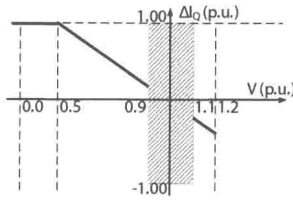
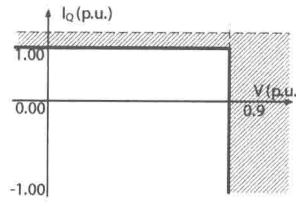
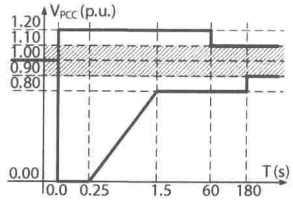
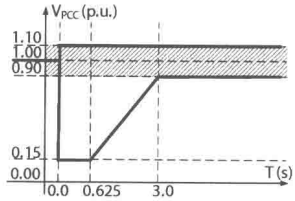
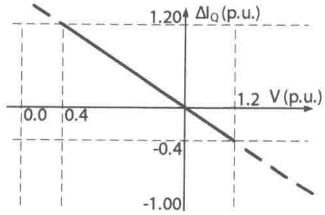
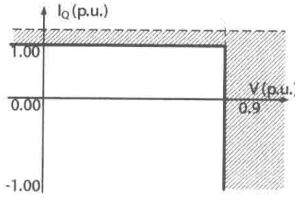
Country	**Germany**	**Puerto Rico**
Standard	BDEW	PREPA
VRT profile		
I_q **VRT**		
I_d **VRT**	0	0
Recovery time	5 s	5 s
Phase jump	N/D	N/D
Country	**South Africa**	**Spain**
Standard	NERSA	REE
VRT profile		
I_q **VRT**		
I_d **VRT**	Previous fault I_d	0
Recovery time	5 s	N/D
Phase jump	Up to 40°	N/D

Table 2. MTRs review for VRT capabilities of PV plants (B). National Commission of Energy: CNE; Electrotechnical Italian Committee: CEI; Electricity Regulatory Commission: ERC; Romanian Electricity Authority: Transelectrica.

Country	Chile	Italy
Standard	CNE	CEI
VRT profile		
I_q **VRT**		
I_d **VRT**	Previous fault I_d	0
Recovery time	N/D	N/D
Phase jump	N/D	N/D
Country	**Jordan**	**Romania**
Standard	ERC	Transelectrica
VRT profile		
I_q **VRT**		
I_d **VRT**	0	0
Recovery time	60 s	350 ms
Phase jump	N/D	N/D

Then, some requirements are imposed over the power generation during the voltage excursions in order to help the system stability. An injection of reactive current (I_q) is always required. Older grid codes, like the Spanish or Italian legislation [8,9], usually require generating the maximum possible capacitive current. However, most recent grid codes usually require a droop relationship between capacity current and the depth of the voltage sag, in order to provide a softener recovery [6,7,12,13].

There are two choices for the active current (I_d) requirement: to follow the previous value to the fault state, for example the South African and Chilean cases [6,12]; or to drop the reference to zero, but consumption is not allowed, like the German and Puerto Rican cases [5,7].

A recovery time after the fault requirements could be needed, as well. It could vary from milliseconds [11] to minutes [13].

Finally, most recent grid codes are also including phase-jump fault requirements, for example the South African grid code [6].

The worst scenarios cover the necessity to remain connected against 40° phase-jumps and 0.0 p.u. low voltage excursions, for three-phase and mono-phase faults. A sudden occurrence of this type of fault could cause a peak in the converter output current. Therefore, these current peaks cause unit errors and disconnections, being a hazard to the unit safety.

Together with the operation mode and the imposed limits, response time is crucial in these kinds of events, whose durations are in the order of milliseconds. At the beginning of the fault, any delay could be critical, because the grid voltage could change very fast. Figure 1 shows an uncontrolled peak current due to a severe low voltage excursion in a three-phase power converter.

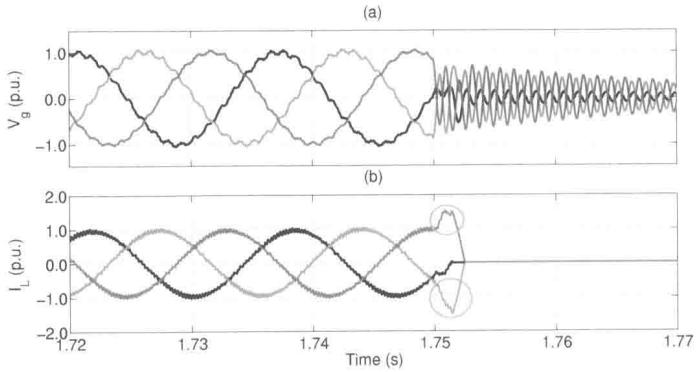


Figure 1. Peak current fault under a severe low voltage excursion. (**a**) Transient low voltage profile; (**b**) stack converter output currents; uncontrolled peak currents marked with green circles.

There is much research on power converter controllers during grid fault conditions [14–19], but unfortunately, there is not enough analysis about the uncontrolled beginning of the fault. A new fast peak current control (FPCC) is proposed to help the converter control limiting the over-current peak of the converter at the beginning of the fault. Consequently, hardware and software current protection could be avoided, improving the MTRs compliance. Further, lower peak current reduces insulated gate bipolar transistors (IGBTs)' degradation and unexpected disconnections from the grid of the power converters, so mean time between failures (MTBF) increases.

This manuscript is organized as follows: Section 2 analyzes in detail the proposed method theory; Sections 3 and 4 show the test results; discussions are given in Section 5; Finally, the materials and methods used are pointed out in Section 6.

2. Fast Peak Current Control Method

2.1. Power Converter Control Strategy

A two-level three-phase topology has been selected for the study. Industrial high-power grid-tie converters usually use a single-stage inverter topology, with an LC output filter [20,21].

Figure 2 shows a classical DG converter control block scheme. The controller is divided into four layers. The highest level controller generates the appropriate references for the middle controller. The middle level controller reacts by modifying the response as a function of the environment agents, which could limit the inverter capability. Typically, special voltage sag control will be placed at this

layer. Then, the low level controller includes the inner current control loop that sets the inverter control actions following the references. Finally, the hardware level controller translates the control signals to the physical pulses of the converter.

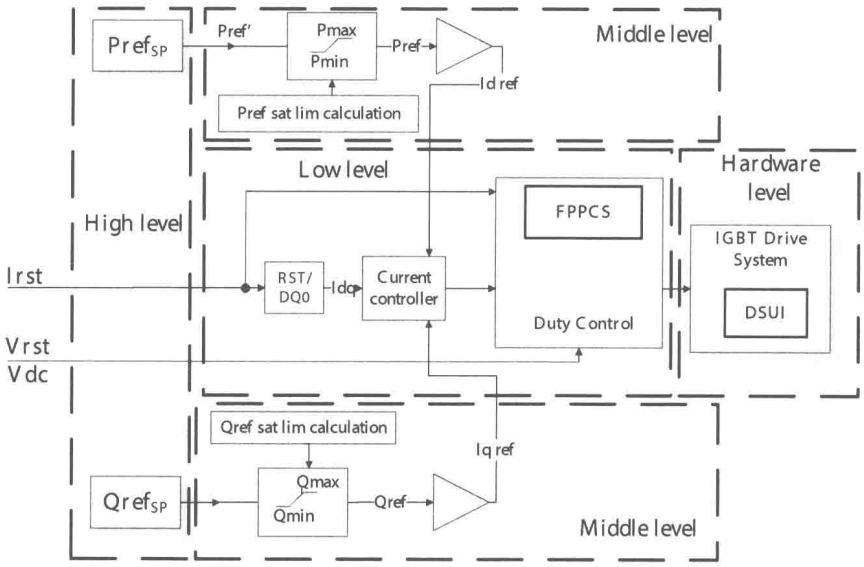


Figure 2. Simplified control block scheme of a distributed generator (DG) power converter.

The proposed FPCC will be improved with two individual actions. Gray boxes in Figure 2 show where these actions take place. On the one hand, in the lower level, the duty cycle control signal is saturated with a theoretical current limit, called the fast predictive peak current saturation (FPPCS) method. On the other hand, at the hardware level, the delay of duty control signal updating is reduced without modifying pulse width modulation (PWM) switching frequency with a technique denoted as duty signal updating improvement (DSUI).

2.2. Fast Predictive Peak Current Saturation Method

Figure 3 shows a simplified single-line model of the converter as an ideal controlled voltage source. This model has been widely presented in the literature [22]. The converter output line-to-line voltage (V_{gRS}, V_{gST}) is defined by an impedance (Z_{sc}) and a grid voltage source. The measured voltage could be used to build up an equivalent voltage source model (V_{nR}, V_{nS}, V_{nT}) connected to the virtual neutral point of the converter model (noted by the dashed lines in Figure 3).

Equation (1) shows the relationship of the inductor voltage (V_L) with the voltage source model of Figure 3 and with the differential equation of an inductor:

$$V_L = \begin{cases} D\frac{V_{dc}}{2} - V_n \\ L\frac{dI_L}{dt} \end{cases} \quad (1)$$

where V_{dc} is the DC-link voltage, V_n is the grid voltage, D is the DG duty control signal in the range of $[-1, 1]$, L is the inductive value of the filter value and I_L is the current across the inductance. Since the controller is executed periodically at a fixed frequency F_s, Equation (1) could be discretized, and D would be given by Equation (2):

$$D_k = 2\frac{L(I_{L_{k+1}} - I_{L_k})F_s + V_{n_k}}{V_{dc_k}} \quad (2)$$

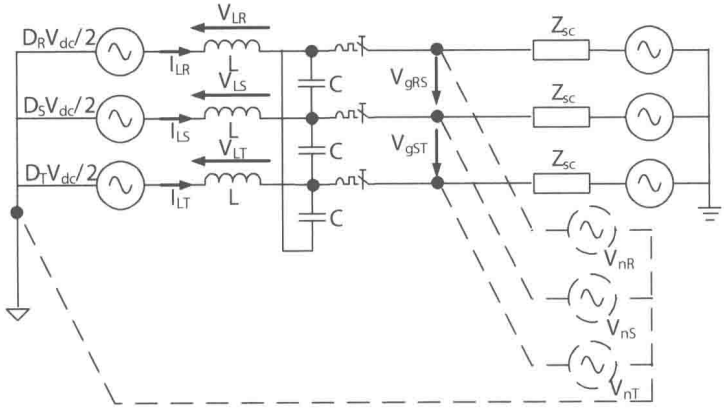


Figure 3. Simplified inverter voltage source model.

Equation (2) gives the relationship between I_L time evolution and the control signal value. Consequently, the current measurement on the next step control could be predicted. Imposing a control law restriction with a maximum current threshold I_{FPPCS}, Equation (3) sets a theoretical maximum control signal:

$$\begin{aligned} D_{\max R_k} &= 2\frac{L(I_{FPPCS}-I_{R_k})F_s+V_{g_k}}{V_{dc_k}} \\ D_{\max S_k} &= 2\frac{L(I_{FPPCS}-I_{S_k})F_s+V_{g_k}}{V_{dc_k}} \\ D_{\max T_k} &= 2\frac{L(I_{FPPCS}-I_{T_k})F_s+V_{g_k}}{V_{dc_k}} \end{aligned} \tag{3}$$

where $D_{\max R_k}$, $D_{\max S_k}$ and $D_{\max T_k}$ are the maximum duty allowed control signals for the defined I_{FPPCS} in each phase and I_{R_k}, I_{S_k} and I_{T_k} are the measured currents of the three phases at the k instant.

2.3. Duty Signal Updating Improvement Method

Typically, PWM techniques update only their control signals in the valleys and peaks of the triangular carrier, T_0 and T_2 respectively (see Figure 4), guaranteeing non-desirable firing, the switching frequency remaining constant and avoiding extra power losses [23].

Figure 4 shows a typical delay added in a power converter controller. If the control processor needs the computational time (T_c) since the last sampling time (T_0), then an additional delay of T_m will be inserted before the action will be executed, because the control signal can only be updated in the peaks and the valleys. The proposed technique updates the control signal at T_1 with some restrictions. Then, only T_c delay happens, and the peak current under faulty conditions will drop.

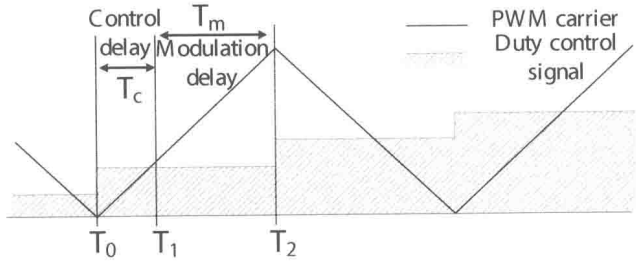


Figure 4. Typical delay added in a power converter controller. The measures are taken at T_0, but T_c is needed to calculate the next control signal. Finally, the control signal is updated and applied at T_2. Pulse width modulation: PWM.

As an example, Figure 5 shows all four possible cases in the up-slope PWM carrier semi-cycle, but similar cases could be exposed in the down-slope semi-cycle. On the one hand, during the

up-slope, if the previous control signal (D_0) is greater than the triangular carrier value at T_1, no extra transition is guaranteed, and the new control signal (D_1) could be updated without any additional switching in the semi-cycle (Cases c and d in Figure 5). On the other hand, if D_0 is lower than the triangular carrier at T_1, at least three transitions may occur if D_1 is updated at T_1: the first one belongs to the D_0 level; a second transition happens at T_1; and a third transition will happen at the D_1 level. Consequently, the control signal will be updated in the next valley or peak to avoid extra switching (Case a in Figure 5). Finally, Case b does not produce any extra-switching, but neither modifies the control output.

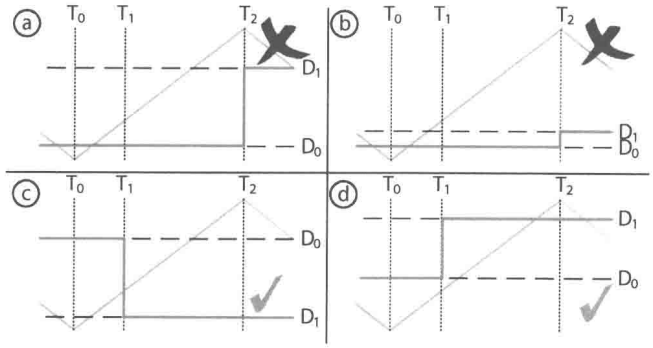


Figure 5. All four possible duty updating cases in the rising PWM semi-cycle. The control signal could be updated at T_1 in Cases c and d, but must be updated at T_2 in Cases a and b.

Graphically, Figure 6 shows an example of PWM signals generated in Cases a and c. In Case c, the duty signal is updated (blue line) without producing extra switching, reducing the on state of the semiconductor. However, in Case a, the control signal must be updated in T_2 (solid blue line); otherwise, two switching events will happen (dotted red line).

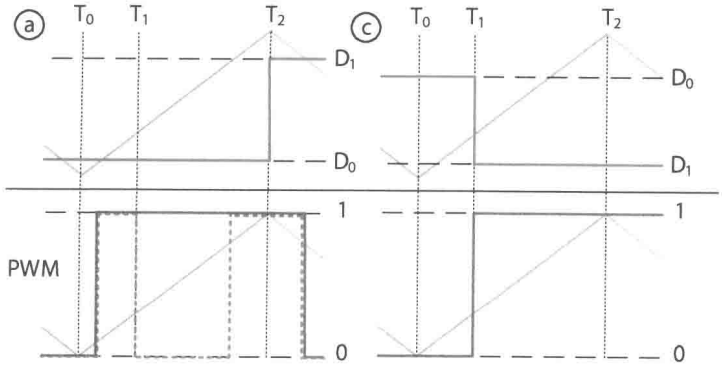


Figure 6. PWM signals generated with Cases a and c of the rising PWM semi-cycle. The red dotted line points out possible malfunctioning with two switchings in the same semi-cycle if the proposed rule is not applied. The blue line points out PWM signals generated with the duty signal updating improvement (DSUI) method.

Following the same steps, along the modulation down-slope cycle, if D_0 is lower than the modulation value at T_1, the control signal could be updated without any change in the switching frequency. Figure 7 shows all four possible cases on the down-slope semi-cycle.

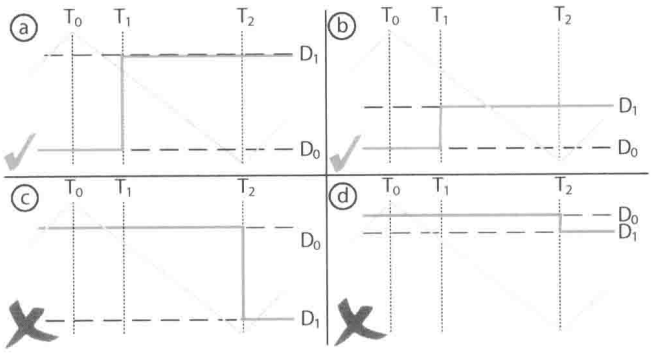


Figure 7. All four possible duty updating cases in the falling PWM semi-cycle. The control signal could be updated at T_1 in Cases a and b, but must be updated at T_2 in Cases c and d.

Fortunately, not all cases are relevant with respect to current faults. Therefore, a study could be made to determine the effectiveness of the improvement in these special cases. There are two fault conditions: a positive and a negative over-current peak. From here, the up-slope case will be analyzed, but a similar reasoning could be done for the down-slope semi-cycle.

According to Equation (2), at instant $k = 1$, the worst over-current peak (I_{L_0}) would happen if the current peak fault was add up over the maximum current value modulated. Consequently, D_0 is expected to be positive and big enough. In addition, if a dangerous peak current happened, the controller would have to drop I_L to a safety region. According to Equation (2), to take down I_{L_1}, D_1 will be very low. Therefore, if a positive over-current peak happens, Case c of Figure 5 is expected. As previously mentioned, this is one of the allowed cases to refresh the control signal, so the over-current peak will be reduced.

A similar reasoning could be made with a negative over-current fault. On the one hand, now, D_0 is expected to be negative and big enough. On the other hand, from Equation (2), the D_1 expected value will be very high. Consequently, if a negative over-current peak happens, Case a or d of Figure 5 is expected. If Case d happens, the control signal will be updated, and the over-current peak will be reduced. Unfortunately, if Case a happens, the method will not act in this semi-cycle.

Figure 5 points out that T_c influences the effectiveness of the method. If T_c is forced to zero, all control steps will be in the c and d cases, so it is important to have a small delay T_c to short the measured peak current in most situations.

Finally, one more action could be performed to reduce the over-current peak. A fault happening in semi-cycle k will be measured at the beginning of the next semi-cycle $k + 1$, and the control action will be placed at T_1 in the best case or at the beginning of $k + 2$ in the worst case. Therefore, the maximum delay could be $2T_s$ or $T_s + T_c$.

If T_c is relatively short, a new control step could be done at the middle of the semi-cycle. This control signal will be applied with the same rules as the others, so in a general way, it will be placed at the final part of the semi-cycle. In this case, if a fault happens at the middle of the semi-cycle k', it will be measured at the beginning of the next control step $k' + 1$, and the control action will be placed at T_1 in the best case or at the beginning of $k' + 2$ in the worst case. Therefore, the maximum delay could be T_s or $0.5 \cdot T_s + T_c$. Assuming V_L constant in a short period of time during the fault condition:

$$I_L = \frac{1}{L}\int V_L \mathrm{d}t \longrightarrow \Delta I_L = \frac{V_L}{L} \cdot T_{\text{delay}} \tag{4}$$