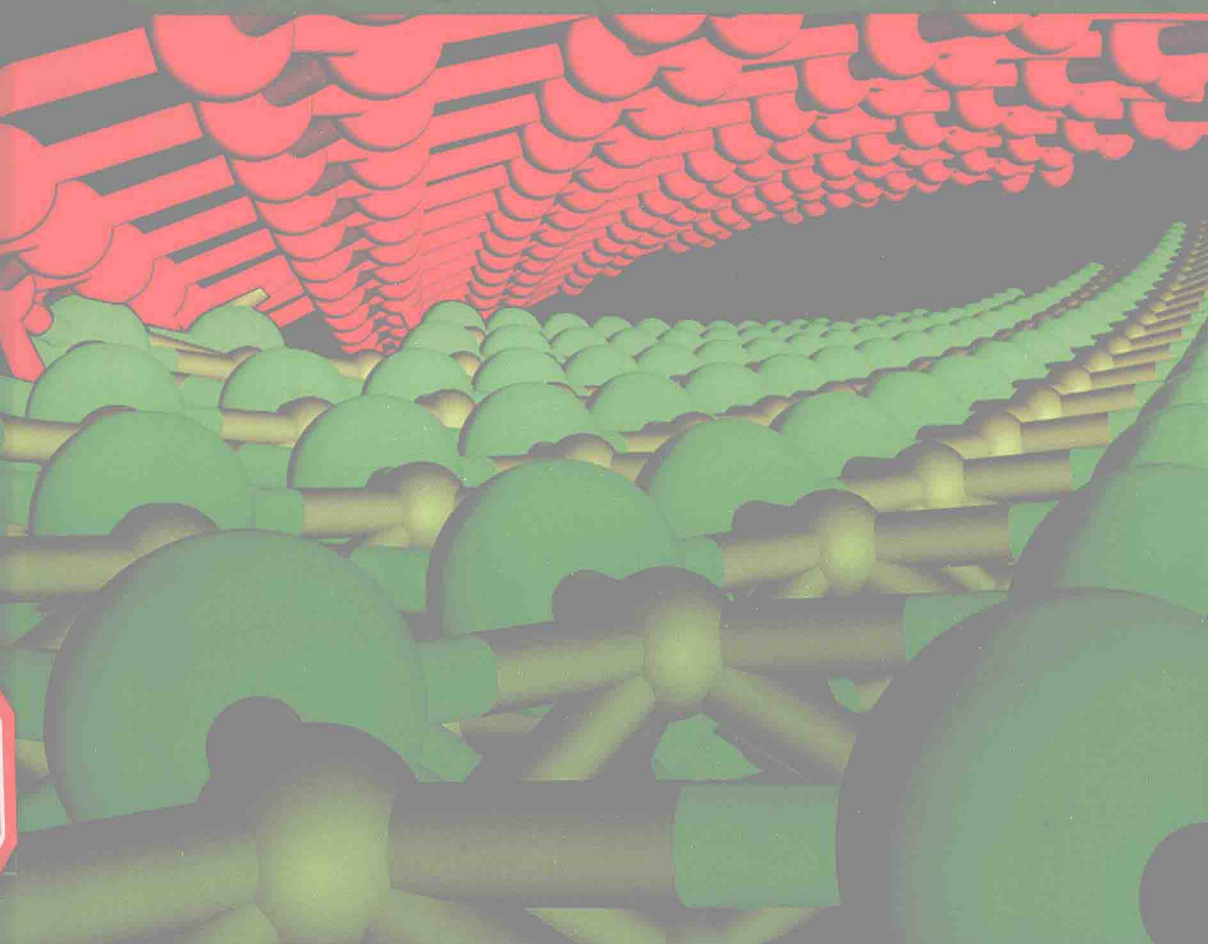
LEONARD J. BRILLSON

# AN ESSENTIAL GUIDE TO ELECTRONIC MATERIAL SURFACES AND INTERFACES



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# An Essential Guide to Electronie Material Surfaces and Interfaces

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# An Essential Guide to Electronic Material Surfaces and Interfaces

# Preface

This book is intended to introduce scientists, engineers, and students to surfaces and interfaces of electronic materials. It is designed to be a concise but comprehensive guide to the essential information needed to understand the physical properties of surfaces and interfaces, the techniques used to measure them, and the methods now available to control them. The book is organized to provide readers first with the basic parameters that describe semiconductors, then the key features of their interfaces with vacuum, metal, and other semiconductors, followed by the many experimental and theoretical techniques available to characterize electronic material properties, semiconductor surfaces, and their device applications, and finally our current understanding of semiconductor interfaces with metals and with other semiconductors – understanding that includes the methods, both macroscopic and atomic-scale, now available to control their properties.

Electronic material surfaces and interfaces has become an enormous field that spans physics, chemistry, materials science, and electrical engineering. Its development in terms of new materials, analytic tools, measurement and control techniques, and atomic-scale understanding is the result of nearly 70 years of activity worldwide. This book is intended to provide researchers new to this field with the primary results and a framework for new work that has developed since then. More in-depth information is provided in a Track II, accessed online, that provides advanced examples of concepts discussed in the text as well as selected derivations of important relationships. The problem sets following each chapter provide readers with exercises to strengthen their understanding of the material presented. Figures for use by instructors are available from the accompanying website. For more advanced and detailed information, the reader is referred to *Surfaces and Interfaces of Electronic Materials* (Wiley-VCH, Weinheim, 2010) as well as the lists of Further Reading following each chapter.

On a personal note, the author wishes to acknowledge his Ph.D. thesis advisor, Prof. Eli Burstein at the University of Pennsylvania and Dr. Charles B. Duke at Xerox Corporation in Webster, New York for their inspiration and mentoring. Here at The Ohio State University, he thanks his many Electrical & Computer Engineering and Physics colleagues who have provided such a stimulating environment for both teaching and research. Most of all, the author's deepest thanks are to his wife, Janice Brillson, for her patience, love, and support while this book was written.

Columbus, Ohio July 31, 2015

# About the Companion Websites

This book is accompanied by Instructor and Student companion websites:

www.wiley.com\go\brillson\electronic

The Instructor website includes

- Supplementary materials
- PPT containing figures
- Advanced topics
- Solutions to problems

The student website includes

- Supplementary materials
- Advanced topics

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# 1

# Why Surfaces and Interfaces of Electronic Materials

## 1.1 The Impact of Electronic Materials

This is the age of materials – we now have the ability to design and create new materials with properties not found in nature. Electronic materials are one of the most exciting classes of these new materials. Historically, electronic materials have meant semiconductors, the substances that can emit and react to light, generate and control current, as well as respond to temperature, pressure, and a host of other physical stimuli. These materials and their coupling with insulators and metals have formed the basis of modern electronics and are the key ingredient in computers, lasers, cell phones, displays, communication networks, and many other devices. The ability of these electronic materials to perform these functions depends not only on their inherent properties in bulk form but also, and increasingly so, on the properties of their surfaces and interfaces. Indeed, the evolution of these materials over the past 70 years has been for ever decreasing size and increasing complexity, features that have driven ever increasing speeds and the ability to manage ever larger bodies of information. In turn, these are enabling our modern day quality of life.

## 1.2 Surface and Interface Importance as Electronics Shrink

Surfaces and interfaces are central to microelectronics. One of the most common microelectronic devices is the transistor, whose function can illustrate the interfaces involved and their increasing importance as the scale of electronics shrinks. Figure 1.1 shows the basic structure of a transistor and the functions of its interfaces. Current passes from a *source* metal to a *drain* metal through a semiconductor, in this case, Si. Voltage applied to a *gate* metal positioned between the source and drain serves to attract or repel charge

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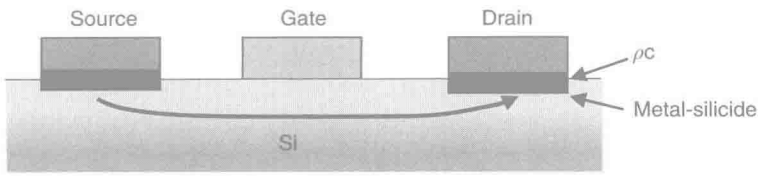


***Figure 1.1*** *Source–gate–drain structure of a silicon transistor. (Brillson 2010. Reproduced with permission of Wiley.)*

from the semiconductor region, the "*channel*", through which current travels. The result is to control or "gate" the current flow by this third electrode. This device is at the core of the microelectronics industry.

The interfaces between the semiconductor, metal, and insulator of this device play a central role in its operation. Barriers to charge transport across the metal–semiconductor interface are a major concern for all electronic devices. Low resistance contacts at Si source and drain contacts typically involve metals that produce interface reactions, for example, Ti contacts that react with Si with high temperature annealing to form $TiSi_2$ between Ti and Si, as shown in Figure 1.2a. These reacted layers reduce such barriers to charge transport and the contact resistivity $\rho_C$. Such interfacial silicide layers form low resistance, planar junctions that can be integrated into the manufacturing process for integrated circuits and whose penetration into the semiconductor can be controlled on a nanometer scale.

The gate–semiconductor interface is another important interface. This junction may involve either: (i) a metal in direct contact with the semiconductor where the interfacial barrier inhibits charge flow or (ii) as widely used in Si microelectronics, a metal–insulator–semiconductor stack to apply voltage without current leakage to the semiconductor's channel region (Figure 1.2b). Lattice sites within the insulator and at the insulator–semiconductor interface can trap charges and introduce electric dipoles that oppose the voltage applied to the gate metal and its control of the channel current. A major goal of the microelectronics industry since the 1950s has been to minimize the formation of these localized charge states.

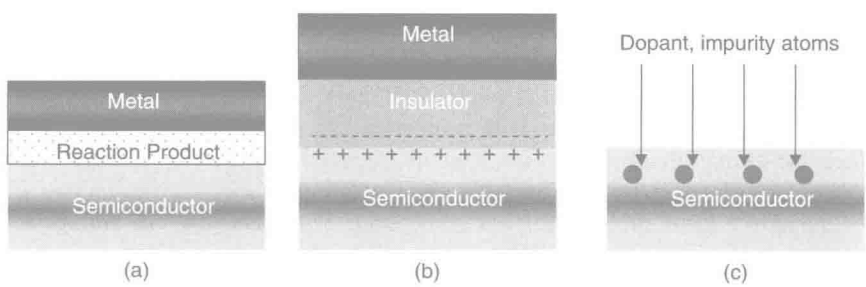


***Figure 1.2*** *Interfaces involved in forming the transistor structure including: (a) the source or drain metal–semiconductor contact with a reacted interface, (b) the gate metal–semiconductor contact separated by an insulator in and near which charges are trapped, and (c) dopant impurity atoms implanted below the surface of a semiconductor to control its carrier concentration. (Brillson 2010. Reproduced with permission of Wiley.)*

A third important interface involves the implantation of impurity atoms into the semiconductor to add donor or acceptor "dopants" that control the transistor's n- or p-type carrier type and density within specific regions of the device. This process involves acceleration and penetration of ionized atoms at well-defined depths, nanometers to microns, into the semiconductor, as Figure 1.2c illustrates. This ion implantation also produces lattice damage that high temperature annealing can heal. However, such annealing can introduce diffusion and unintentional doping in other regions of the semiconductor that can change their electronic activity. Outdiffusion of semiconductor constituents due to annealing is also possible, leaving behind electronically active lattice sites. Precise design of materials, surface and interface preparation, thermal treatments, and device architectures are required in order to balance these competing effects.

At the circuit level, there are multiple interfaces between semiconductors, oxides, and metals. For Si transistors, the manufacturing process involves (i) growing a Si boule in a molten bath that can be sectioned into wafers, (ii) oxidizing, diffusing, and implanting with dopants, (iii) overcoating with various metal and organic layers, (iv) photolithographically patterning and etching the wafers into monolithic arrays of devices, and (v) dicing the wafer into individual circuits that can be mounted, wire bonded, and packaged into chips. Within individual circuit elements, there can be many layers of interconnected conductors, insulators, and their interfaces. Figure 1.3 illustrates the different materials and interfaces associated with a 0.18 μm transistor at the bottom of a multilayer Al–W–Si-oxide dielectric assembly [1]. Reaction, adhesion, interdiffusion, and the formation of localized electronic states must be carefully controlled at all of these interfaces during the many patterning, etching, and annealing steps involved in assembling the full structure. The materials used in this multilayer device architecture have continued to change over decades to compensate for the otherwise increasing electrical resistance as interconnects between layers shrink into the nanometer regime. These microelectronic materials and architectures continue to evolve in order to achieve higher speeds, reliability, and packing density. This continuing evolution highlights the importance of interfaces since they are an increasing proportion of the entire structure as circuit sizes decrease and become ever more complex.

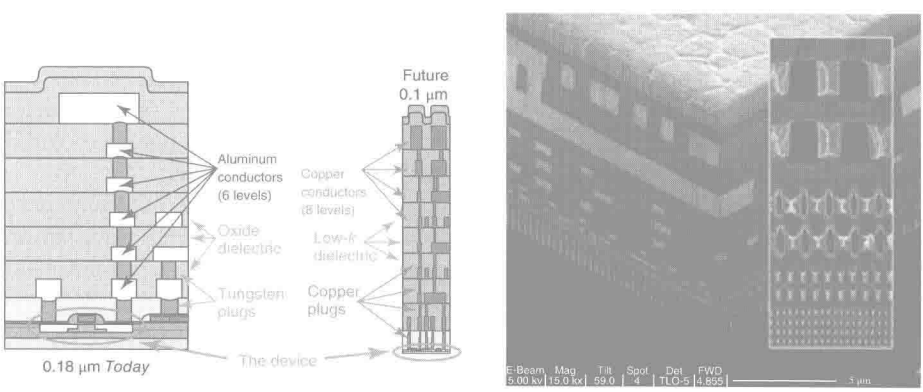


***Figure 1.3*** *Multilayer, multi-material interconnect architectures at the nanoscale. Feature size of interconnects at right is 45 nm [1].*

Besides transistors, many other electronic devices rely on interfaces for their operation. For example, solar cells operate by converting incident light into free electrons and holes that separate and generate current or voltage in an external circuit. The charge separation requires built-in electric fields that occur at metal–semiconductor or semiconductor–semiconductor interfaces. These will be discussed in later chapters. Transistors without metal gates are another such device. Channel current is controlled instead by molecules that adsorb on this otherwise free surface, exchanging charge and inducing electric fields analogous to that of a gate. Interfaces are also important in devices that generate photons, microwaves, and acoustic waves. These devices require low resistance contacts to inject current or apply voltage to the layer that generates the radiation. Otherwise, power is lost at these contacts, reducing or totally blocking power conversion inside the semiconductor. Semiconductor cathodes that emit electrons when excited by incident photons are also sensitive to surface conditions. Surface chemical treatments of specific semiconductors are required in order to promote the emission of multiple electrons when struck by single photons, useful for electron pulse generation or photomultipliers.

For devices on the quantum scale, surfaces and interfaces have an even larger impact. A prime example is the quantum well, one of the workhorses of optoelectronics. Here a semiconductor is sandwiched between two larger gap semiconductors that localize both electrons and holes in the smaller gap semiconductor. This spatial overlap between electrons and holes increases electron–hole recombination and light emission. Since the quantum well formed by this sandwich is only a few monolayers thick, the allowed energies of electrons and holes inside the well are quantized at discrete energies, which promotes efficient carrier population inversion and laser light emission. Imperfections at the interfaces of these quantum wells introduce alternative pathways for recombination that reduce the desired emission involving the quantized states. Such recombination is even more serious for three-dimensional quantum wells, termed *quantum dots*. Another such example is the *two-dimensional electron gas* (2DEG) formed when charges accumulate in narrow interfacial layers, only a few tens of nanometers thick, between two semiconductors. The high carrier concentration, high mobility 2DEG is the basis of *high electron mobility transistors* (HEMTs). As with quantum wells, lattice defects at the interface can produce local electric fields that scatter charges, reduce mobility, and alter or even destroy the 2DEG region. Yet another quantum-scale structure whose interfaces play a key role is the *cascade laser*, based on alternating high- and low-bandgap semiconductors. In this structure, charge must tunnel through monolayer thin barrier layers, formed by the higher band gap semiconductors, into quantized energy levels. Here again, efficient tunneling depends on interfaces without significant imperfections that could otherwise introduce carrier scattering.

In addition to carrier scattering and recombination, the alignment of energy levels between constituents is a major feature of interfaces. How energy levels align between a semiconductor and a metal, as well as between two semiconductors, is a fundamental issue that is still not well understood. The interface band alignment determines the barriers to charge transport between constituents and the carrier confinement between them. There are several factors that can play a role: (i) the band structure of the constituents at the junction, (ii) the conditions under which the interface forms, and (iii) any subsequent thermal or chemical processing. Hence, it is important to measure and understand the properties of these interfaces at the microscopic, indeed atomic, level in order to learn and