国外电子信息精品著作(影印版)

时钟发生器在片上系统处理器中的应用

Clock Generators for SOC Processors

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内 容 简 介

本书针对在SOC芯片上使用的全集成频率合成器的设计，从电路和系统的角度对锁相环的原理和设计进行了分析。特别是在电路层次上，讨论了深亚微米CMOS数字工艺中的低电压模拟电路的设计，有比较大的参考意义。在对锁相环基本工作原理分析的基础之上，本书分析了具体的时钟产生方案和电路设计问题，并进一步讨论了锁相环的应用。本书还包括了PLL可测试性设计的内容。最后还从宏观角度讨论了SOC时钟域的设计。书中包含的大量实际问题分析应该有助于读者更好地理解时钟产生器设计中的核心问题。

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《国外电子信息精品著作》序

20世纪90年代以来，信息科学技术成为世界经济的中坚力量。随着经济全球化的进一步发展，以微电子、计算机、通信和网络技术为代表的信息技术，成为人类社会进步过程中发展最快、渗透性最强、应用面最广的关键技术。信息技术的发展带动了微电子、计算机、通信、网络、超导等产业的发展，促进了生命科学、新材料、能源、航空航天等高新技术产业的成长。信息产业的发展水平不仅是社会物质生产、文化进步的基本要素和必备条件，也是衡量一个国家的综合国力、国际竞争力和发展水平的重要标志。在中国，信息产业在国民经济发展中占有举足轻重的地位，成为国民经济重要支柱产业。然而，中国的信息科学支持技术发展的力度不够，信息技术还处于比较落后的水平，因此，快速发展信息科学技术成为我国迫在眉睫的大事。

要使我国的信息技术更好地发展起来，需要科学工作者和工程技术人员付出艰辛的努力。此外，我们要从客观上为科学工作者和工程技术人员创造更有利于发展的环境，加强对信息技术的支持与投资力度，其中也包括与信息技术相关的图书出版工作。

从出版的角度考虑，除了较好较快地出版具有自主知识产权的成果外，引进国外的优秀出版物是大有裨益的。洋为中用，将国外的优秀著作引进到国内，促进最新的科技成就迅速转化为我们自己的智力成果，无疑是值得高度重视的。科学出版社引进一批国外知名出版社的优秀著作，使我国从事信息技术的广大科学工作者和工程技术人员能以较低的价格购买，对于推动我国信息技术领域的科研与教学是十分有益的事。

此次科学出版社在广泛征求专家意见的基础上，经过反复论证、仔细遴选，共引进了接近30本外版书，大体上可以分为两类，第一类是基础理论著作，第二类是工程应用方面的著作。所有的著作都涉及信息领域的最新成果，大多数是2005年后出版的，力求“层次高、内

容新、参考性强”。在内容和形式上都体现了科学出版社一贯奉行的严谨作风。

当然，这批书只能涵盖信息科学技术的一部分，所以这项工作还应该继续下去。对于一些读者面较广、观点新颖、国内缺乏的好书还应该翻译成中文出版，这有利于知识更好更快地传播。同时，我也希望广大读者提出好的建议，以改进和完善丛书的出版工作。

总之，我对科学出版社引进外版书这一举措表示热烈的支持，并盼望这一工作取得更大的成绩。

中国科学院院士
中国工程院院士
2006 年 12 月

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About the Author

Amr M. Fahim received his B.A.Sc, M.A.Sc, and Ph.D. degrees from the University of Waterloo in Computer Engineering in 1996 and Electrical Engineering in 1997, and 2000 respectively.

During his graduate studies, he has had research collaboration twice with industry. In May - August 1996, he worked with Rockwell Semiconductor Systems (currently Mindspeed) in Newport Beach, California designing low-power PLL-based on-chip clock generators for microprocessors. In June - December 1999, he worked with Texas Instruments designing low-power RF fractional-N frequency synthesizers.

Upon completion of his Ph.D. degree in 2000, he joined Qualcomm Inc., San Diego, CA, where he spent four years driving the development of mixed-signal IC cores for clocking generator systems for integrated analog/digital Mobile Station Modem (MSM) chipsets. He is currently with Skyworks Solutions Inc. in Irvine, CA, working on mixed-signal and radio frequency integrated circuit (RFIC) designs. His research interests include design and analysis of low-power integrated frequency synthesis techniques and mixed-signal/RF system-on-a-chip (SoC) processors. He has authored over 25 papers and has several U.S. and European patents to his credit. He has also been a reviewer for numerous papers sent for publication including the IEEE Journal of Solid-State Circuits, IEEE Transactions on Circuits and Systems II, Midwest Symposium on Circuits and Systems, and VLSI Symposium.

Preface

This book examines the issue of design of fully integrated frequency synthesizers suitable for system-on-a-chip (SOC) processors. This book takes a more global design perspective in jointly examining the design space at the circuit level as well as at the architectural level. The coverage of the book is comprehensive and includes summary chapters on circuit theory as well as feedback control theory relevant to the operation of phase locked loops (PLLs). On the circuit level, the discussion includes low-voltage analog design in deep submicron digital CMOS processes, effects of supply noise, substrate noise, as well device noise. On the architectural level, the discussion includes PLL analysis using continuous-time as well as discrete-time models, linear and nonlinear effects of PLL performance, and detailed analysis of locking behavior.

The material then develops into detailed circuit and architectural analysis of specific clock generation blocks. This includes circuits and architectures of PLLs with high power supply noise immunity and digital PLL architectures where the loop filter is digitized. Methods of generating low-spurious sampling clocks for discrete-time analog blocks are then examined. This includes sigma-delta fractional-N PLLs, Direct Digital Synthesis (DDS) techniques and non-conventional uses of PLLs. Design for test (DFT) issues as they arise in PLLs are then discussed. This includes methods of accurately measuring jitter and built-in-self-test (BIST) techniques for PLLs. Finally, clocking issues commonly associated to system-on-a-chip (SOC) designs, such as multiple clock domain interfacing and partitioning, and accurate clock phase generation techniques using delay-locked loops (DLLs)

are also addressed. The book provides numerous real world applications, as well as practical rules-of-thumb for modern designers to use at the system, architectural, as well as the circuit level. This book is well suited for practitioners as well as graduate level students who wish to learn more about time-domain analysis and design of frequency synthesis techniques.

Foreword

Current literature is filled with textbooks and research papers describing frequency synthesizers from a front-end wireless transceiver perspective. The emphasis has historically been on evaluating the frequency synthesizer's performance in the frequency domain, i.e. in terms of phase noise and spurious signals. As microprocessor frequency surge, the need to understand digital requirements for low-jitter and the design of low-jitter frequency synthesizers and clock generator becomes every increasingly important. This book is dedicated to the time-domain (i.e. jitter) design and analysis of frequency synthesizers and clock generators for microprocessor applications. Such explanations are often scattered through literature and, to my knowledge, has not recently been gathered into one comprehensive textbook.

This book also focuses on the CMOS IC implementation of such synthesizers. An entire chapter is dedicated to low-voltage mixed-signal integrated circuit design in deep submicron CMOS technologies. Subsequent chapters discuss the design and analysis of the most common frequency synthesizer, the phase-locked loop (PLL), as well as state-of-the-art innovative architectures suitable for system-on-a-chip (SOC) processors. Design for Testability (DFT) is also discussed in the context of frequency synthesizers in SOC processors. The book concludes by discussing some of the most common issues that arise in clock interfacing, clock distribution, and accurate delay generation through delay-locked loops (DLLs) as they apply to SOC processors. Such issues mainly arise from having to communicate data and clock signals across multiple clock and power

domains. The book provides numerous real world applications, as well as practical rules-of-thumb for modern designers to use at the system, architectural, as well as the circuit level.

Contents

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Chapter 1

INTRODUCTION

1.1 What are System-on-a-Chip Processors?

System-on-a-chip (SoC) technology is the integration of all the necessary electronic circuits and devices for a specified system into a single integrated circuit (IC) package. This typically includes an embedded microprocessor or controller, dedicated logic, memory, and some analog circuitry, such as analog-to-digital (A/D) converters or digital-to-analog (D/A) converters. In some cases, such as Bluetooth processors, this may include an entire RF wireless transceiver packaged into a single chip.

System-on-a-chip processors have been enabled by rapid advances in microelectronics, specifically complementary metal oxide semiconductor (CMOS) technology. The computing power of microprocessors has been increasing exponentially following Moore's Law. Such advances have brought new design challenges and opportunities that have never been previously anticipated. These design challenges include reducing power consumption, enhancing packaging density and reliability, and development of design automation tools to handle billions of transistors.

Advances SoC technology has already profoundly changed our society. Today mobile communication is affordable and available in most parts of the world. Wireless internet access is becoming a reality. Soon one will be able to browse the internet at tens of megabit per second data rates from a handheld device anywhere in the world.

The future of SoC technology offers new and radical concepts. As nanosensors are being integrated in SoC devices, nanorobots are soon to be a reality. Nanorobots may have profound medical applications such as creating programmable antivirus devices. Other nanoscale SoC devices can

have integrated video processors attached to optic nerve endings to enable vision to the blind.

One dominant trends of SoC processors is increased computing power, which entails increased clock speeds. This naturally makes clock partitioning and generation in SoC processors a very important topic. This book is dedicated to a detailed discussion on the design and analysis of clock generation units used in SoC processors. This book also addresses the issues of clock partitioning in SoC processors.

1.2 Organization

This book is divided up into nine chapters including this introduction chapter. Chapter 2 discusses phase-locked loop (PLL) fundamentals. PLLs are the most common implementation of a clock generation unit for SoC processors. Chapter 3 discusses the design challenges of PLL circuit blocks implemented in deep sub-micrometer CMOS technologies. Specifically, low-voltage CMOS analog design is addressed. Once PLL fundamentals and CMOS circuit implementation of PLLs have been discussed, chapter 4 provides a detailed jitter analysis in PLLs. This includes jitter definitions, power supply coupling noise effects on PLLs, oscillator jitter analysis, as well as jitter performance of closed-loop PLL systems. Chapter 5 explores the reduction of jitter in PLLs at the architectural level. Such architectures include supply voltage regulated PLL topologies, adaptive PLL topologies, and delay-locked loop (DLL) based frequency multiplication topologies. The performance of the various clock generation architectures is analyzed in detail and is compared with one another. In chapter 6, an alternative paradigm to PLL design is considered, where the loop filter is completely digitized. In chapter 7, clock generators that are specific to digital signal processing (DSP) applications are given. Modern techniques for design for testability (DFT) for PLLs are given. This includes methods of characterization and verification of embedded PLLs, jitter measurement techniques, and PLL built-in-self-test (BIST) techniques. Finally, chapter 9 concludes the book by a discussion on more global issues such as clock partitioning and skew control on clock signals in large SoC processors.

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