国外电子与通信教材系列

微电子制造科学原理与工程技术

（第二版）

The Science and Engineering of Microelectronic Fabrication

Second Edition

英文版

[美] Stephen A. Campbell 著

電子工業出版社
Publishing House of Electronics Industry
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内 容 简 介

本书系统地介绍了微电子制造科学原理与工程技术，覆盖了集成电路制造所涉及的所有基本单项工艺，包括光刻、等离子体和反应离子刻蚀、离子注入、扩散、氧化、蒸发、气相外延生长、溅射和化学气相淀积等。对每一种单项工艺，不仅介绍了它的物理和化学原理，还描述了用于集成电路制造的工艺设备。本书还介绍了各种先进的工艺技术，如快速热处理、下一代光刻、分子束外延和金属有机物化学气相淀积等。在此基础上本书讨论了如何将这些单项工艺集成为各种常见的集成电路工艺技术，如 CMOS 技术、双极型技术和砷化镓技术，还介绍了微电子制造的新领域，即微机械电子系统及其工艺技术。

本书可作为高等学校微电子专业本科生和研究生相应课程的教科书或参考书，也可供与集成电路制造工艺技术有关的专业技术人员学习参考。

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序

2001年7月间，电子工业出版社的领导同志邀请各高校十几位通信领域方面的老师，商量引进国外教材问题。与会同志对出版社提出的计划十分赞同，大家认为，这对我国通信事业、特别是对高等院校通信学科的教学工作会很有好处。

教材建设是高校教学建设的主要内容之一。编写、出版一本好的教材，意味着开设了一门好的课程，甚至可能预示着一个崭新学科的诞生。20世纪40年代MIT林肯实验室出版的一套28本雷达丛书，对近代电子学科、特别是对雷达技术的推动作用，就是一个很好的例子。

我国领导部门对教材建设一直非常重视。20世纪80年代，在原教委教材编审委员会的领导下，汇集了高等院校几百位富有教学经验的专家，编写、出版了一大批教材；很多院校还根据学校的特点和需要，陆续编写了大量的讲义和参考书。这些教材对高校的教学工作发挥了极好的作用。近年来，随着教学改革不断深入和科学技术的飞速进步，有的教材内容已比较陈旧、落后，难以适应教学的要求，特别是在电子学和通信技术发展神速、可以讲是日新月异的今天，如何适应这种情况，更是一个必须认真考虑的问题。解决这个问题，除了依靠高校的老师和专家撰写新的符合要求的教科书外，引进和出版一些国外优秀电子与通信教材，尤其是有选择地引进一批英文原版教材，是会有好处的。

一年多来，电子工业出版社为此做了很多工作。他们成立了一个“国外电子与通信教材系列”项目组，选派了富有经验的业务骨干负责有关工作，收集了230余种通信教材和参考书的详细资料，调来了100余种原版教材样书，依靠由20余位专家组成的出版委员会，从中精选了40多种，内容丰富，覆盖了电路理论与应用、信号与系统、数字信号处理、微电子、通信系统、电磁场与微波等方面，既可作为通信专业本科生和研究生的教学用书，也可作为有关专业人员的参考材料。此外，这批教材，有的翻译为中文，还有部分教材直接影印出版，以供教师用英语直接授课。希望这些教材的引进和出版对高校通信教学和教材改革能起一定作用。

在这里，我还要感谢参加工作的各位教授、专家、老师与参加翻译、编辑和出版的同志们。各位专家认真负责、严谨细致、不辞辛劳、不怕琐碎和精益求精的态度，充分体现了中国教育工作者和出版工作者的良好美德。

随着我国经济建设的发展和科学技术的不断进步，对高校教学工作会不断提出新的要求和希望。我想，无论如何，要做好引进国外教材的工作，一定要联系我国的实际。教材和学术专著不同，既要注意科学性、学术性，也要重视可读性，要深入浅出，便于读者自学；引进的教材要适应高校教学改革的需要，针对目前一些教材内容较为陈旧的问题，有目的地引进一些先进的和正在发展中的交叉学科的参考书；要与国内出版的教材相配套，安排好出版英文原版教材和翻译教材的比例。我们努力使这套教材能尽量满足上述要求，希望它们能放在学生们的课桌上，发挥一定的作用。

最后，预祝“国外电子与通信教材系列”项目取得成功，为我国电子与通信教学和通信产业的发展培土施肥。也恳切希望读者能对这些书籍的不足之处、特别是翻译中存在的问题，提出意见和建议，以便再版时更正。

吴佑寿

中国工程院院士、清华大学教授

“国外电子与通信教材系列”出版委员会主任

出 版 说 明

进入21世纪以来，我国信息产业在生产和科研方面都大大加快了发展速度，并已成为国民经济发展的支柱产业之一。但是，与世界上其他信息产业发达的国家相比，我国在技术开发、教育培训等方面都还存在着较大的差距。特别是在加入WTO后的今天，我国信息产业面临着国外竞争对手的严峻挑战。

作为我国信息产业的专业科技出版社，我们始终关注着全球电子信息技术的发展方向，始终把引进国外优秀电子与通信信息技术教材和专业书籍放在我们工作的重要位置上。在2000年至2001年间，我社先后从世界著名出版公司引进出版了40余种教材，形成了一套“国外计算机科学教材系列”，在全国高校以及科研部门中受到了欢迎和好评，得到了计算机领域的广大教师与科研工作者的充分肯定。

引进和出版一些国外优秀电子与通信教材，尤其是有选择地引进一批英文原版教材，将有助于我国信息产业培养具有国际竞争能力的技术人才，也将有助于我国国内在电子与通信教学工作中掌握和跟踪国际发展水平。根据国内信息产业的现状、教育部《关于“十五”期间普通高等教育教材建设与改革的意见》的指示精神以及高等院校老师们反映的各种意见，我们决定引进“国外电子与通信教材系列”，并随后开展了大量准备工作。此次引进的国外电子与通信教材均来自国际著名出版商，其中影印教材约占一半。教材内容涉及的学科方向包括电路理论与应用、信号与系统、数字信号处理、微电子、通信系统、电磁场与微波等，其中既有本科专业课程教材，也有研究生课程教材，以适应不同院系、不同专业、不同层次的师生对教材的需求，广大师生可自由选择和自由组合使用。我们还将与国外出版商一起，陆续推出一些教材的教学支持资料，为授课教师提供帮助。

此外，“国外电子与通信教材系列”的引进和出版工作得到了教育部高等教育司的大力支持和帮助，其中的部分引进教材已通过“教育部高等学校电子信息科学与工程类专业教学指导委员会”的审核，并得到教育部高等教育司的批准，纳入了“教育部高等教育司推荐——国外优秀信息科学与技术系列教学用书”。

为做好该系列教材的翻译工作，我们聘请了清华大学、北京大学、北京邮电大学、东南大学、西安交通大学、天津大学、西安电子科技大学、电子科技大学等著名高校的教授和骨干教师参与教材的翻译和审校工作。许多教授在国内电子与通信专业领域享有较高的声望，具有丰富的教学经验，他们的渊博学识从根本上保证了教材的翻译质量和专业学术方面的严格与准确。我们在此对他们的辛勤工作与贡献表示衷心的感谢。此外，对于编辑的选择，我们达到了专业对口；对于从英文原书中发现的错误，我们通过与作者联络、从网上下载勘误表等方式，逐一进行了修订；同时，我们对审校、排版、印制质量进行了严格把关。

今后，我们将进一步加强同各高校教师的密切关系，努力引进更多的国外优秀教材和教学参考书，为我国电子与通信教材达到世界先进水平而努力。由于我们对国内外电子与通信教育的发展仍存在一些认识上的不足，在选题、翻译、出版等方面的工作中还有许多需要改进的地方，恳请广大师生和读者提出批评及建议。

电子工业出版社

教材出版委员会

Preface

The intent of this book is to introduce microelectronic processing to a wide audience. I wrote it as a textbook for seniors and/or first-year graduate students, but it may also be used as a reference for practicing professionals. The goal has been to provide a book that is easy to read and understand. Both silicon and GaAs processes and technologies are covered, although the emphasis is on silicon-based technologies. The book assumes one year of physics, one year of mathematics (through simple differential equations), and one course in chemistry. Most students with electrical engineering backgrounds will also have had at least one course in semiconductor physics and devices including *pn* junctions and MOS transistors. This material is extremely useful for the last five chapters and is reviewed in the first sections of Chapters 16, 17, and 18 for students who haven't seen it before or find that they are a bit rusty. One course in basic statistics is also encouraged but is not required for this course.

Microelectronics textbooks necessarily divide the fabrication sequence into a number of unit processes that are repeated to form the integrated circuit. The effect is to give the book a survey flavor: a number of loosely related topics each with its own background material. Most students have difficulty recalling all of the background material. They have seen it once, two or three years and many final exams ago. It is important that this fundamental material be reestablished before studying new material. Distributed through each chapter of this book are reviews of the science that underlies the engineering. These sections, marked with an "°", also help make the distinction between the immutable scientific laws and the applications of those laws, with all the attendant approximations and caveats, to the technology at hand. Optical lithography, for instance, may have a limited life, but diffraction will always be with us.

A second problem that arises in teaching this type of course is that the solution of the equations describing the process often cannot be done analytically. Consider diffusion as an example. Fick's laws have analytic solutions, but they are only valid in a very restricted parameter space. Predeposition diffusions are done at high concentrations at which the simplifying assumption used in the solution derivation are simply not valid. In the area of lithography even the simplest solutions of the Fresnel equations are beyond the scope of the book. In this text a widely used simulation program called SUPREM III[1] has been used to provide more meaningful examples of the sort of real-world dopant redistribution problems that the microelectronic fabrication engineer might face. The software is intended to augment, not replace, learning the fundamental equations that describe microelectronic processing. Typical installations include VAX-, SUN-, Apollo-, and DOS-based microcomputers. The book also enriches the basic material with additional sections and chapters on process integration for various technologies and on more advanced processes. This additional material is in sections marked with a "+". If time does not permit covering these sections, they may be omitted without loss of the basic content of the course.

The second edition has added a variety of topics to keep it current. Most notably a new chapter has been added to reflect new applications for microfabrication processes. Called microelectromechanical

[1]SUPREM III is a trademark of the Board of Trustees of the Leland Stanford Junior University.

systems (MEMS), this exciting area promises to open up many new areas for microfabrication. The new Chapter 19 was written by Dr. Gregory Cibuzar, who manages the Microtechnology Laboratory at the University of Minnesota and has worked on MEMS for a number of years. If you have questions or comments on this area, you can contact Greg directly at cibuzar@ece.umn.edu.

Finally, one has to acknowledge that, no matter how many times this material is reviewed, it cannot be guaranteed to be free of all the (hopefully) minor errors. In the past, publishers have provided errata when errors were sufficiently numerous or egregious. Even when errata are published, they are very difficult to get to those people who have already bought the book. This means that the average reader is often unaware of most of the corrections until a new or revised edition of the book is released. This book will have an errata file that anyone can access at any time. We will also provide minor additions to the book that were not available at press time. You can access the file by going to the Oxford University Press web site for the book, http://www.oup-usa.org/isbn/0195136055.html. As time goes on I will be adding other minor updates and new topics on this site as well. If you find something that you feel needs correction or clarification in the book, I invite you to notify me at my e-mail address, Campbell@ece.umn.edu. Please be sure to include your justification, citing published references.

Minneapolis

S.A.C.

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Part I

Overview and Materials

This course is unlike many that you may have taken in that the material that will be covered is primarily a number of unit processes that are quite distinct from each other. The book then has the flavor of a survey of topics that will be covered rather than a linear progression. This part of the book will lay the foundations that will be needed to later understand the various fabrication processes.

Grove giveth and Gates taketh away.[1]

The first chapter will provide a roadmap of the course and an introduction to integrated circuit fabrication. The processes that are covered are briefly described in a qualitative manner and the relationships between the various topics are discussed. A simple example of a semiconductor technology, the fabrication of integrated resistors, is used to demonstrate a flow of these processes which we will call a technology. Extensions of the technology to include capacitors and MOSFETs are also discussed.

The second chapter will introduce the topic of crystal growth and wafer production. The chapter contains basic materials information that will be used throughout the rest of the book. This includes crystal structure and crystal defects, phase diagrams, and the concept of solid solubility. Unlike the other unit processes that will be covered in the later chapters, very few integrated circuit fabrication facilities actually grow their own wafers. The topic of wafer production, however, demonstrates some of the important properties of semiconductor materials that will be important both during the fabrication process and to the eventual yield and performance of the integrated circuit. The differences in the production of silicon and GaAs wafers are discussed.

[1] Bob Metcalfe (inventor of Ethernet).

Chapter 1

An Introduction to Microelectronic Fabrication

The electronics industry has grown rapidly in the past four decades. This growth has been driven by a revolution in microelectronics. In the early 1960s, putting more than one transistor on a piece of semiconductor was considered cutting edge. Integrated circuits (ICs) containing tens of devices were unheard of. Digital computers were large, slow, and extremely costly. Bell Labs, which had invented the transistor a decade earlier, rejected the concept of ICs. They reasoned that in order to achieve a working circuit all of the devices must work. Therefore, to have a 50% probability of functionality for a 20 transistor circuit, the probability of device functionality must be $(0.5)^{1/20} = 0.966$, or 96.6%. This was considered to be ridiculously optimistic at the time, yet today integrated circuits are built with billions of transistors.

Early transistors were made from germanium, but most circuits are now made on silicon substrates. We will therefore emphasize silicon in this book. The second most popular material for building ICs is gallium arsenide (GaAs). Where appropriate, the book will discuss the processes required for GaAs ICs. Although GaAs has a higher electron mobility than silicon, it also has several severe limitations including low hole mobility, less stability during thermal processing, a poor thermal oxide, high cost, and perhaps most importantly, much higher defect densities. Silicon has therefore become the material of choice for highly integrated circuits, and GaAs is reserved for circuits that operate at very high speeds but with low to moderate levels of integration. Currently the most common application of GaAs is analog circuits operating at speeds in excess of a gigahertz (10^9 Hz). More recently microelectronic fabrication techniques have been used to build a variety of structures including micromagnetics, optical devices, and micromechanical structures. In some cases these structures have also been integrated into chips containing electronic circuitry. A popular nonelectronic application, micromechanical (MEMS) structures will be introduced later in this book.

To chart the progress of silicon microelectronics it is easiest to follow one type of chip. Memory chips have had essentially the same function for many years, making this type of analysis meaningful. Furthermore, they are extremely regular and can be sold in large volumes, making technology customization for the chip design economical. As a result, memory chips have the highest density of all ICs. Figure 1.1 shows the density of dynamic random access memories (DRAMs) as a function of time. The vertical axis is logarithmic. The density of these circuits increase by increments of 4×. Each of these increments takes approximately three years. One of the most fundamental changes in the fabrication process that allows this technology evolution is the minimum feature size that can be

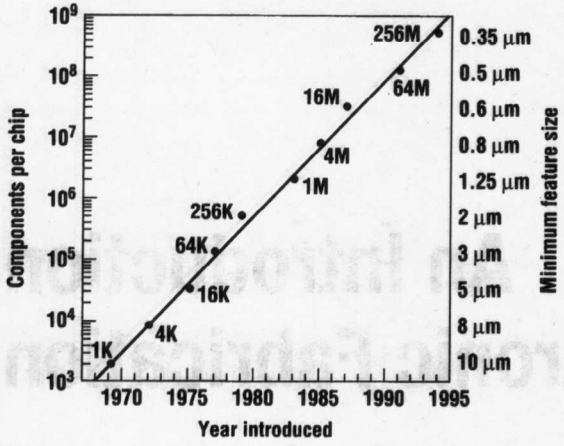

Figure 1.1 Memory and minimum feature sizes for dynamic random access memories as a function of time.

printed on the chip. Not only does this increase IC density, the shorter distances that electrons and holes have to travel improve the transistor speed. Part of the IC performance improvement comes from this increased transistor performance, and part of it comes from being able to pack the transistors closer together, decreasing the parasitic capacitance. The right-hand side of Figure 1.1 shows that ICs have progressed from 10 microns (μm) (1 μm = 10^{-4} cm) to well under 1 μm. For sake of reference, Figure 1.2 shows an electron micrograph of a silicon based IC, along with a human hair. The vertical and horizontal lines are metal wires used to interconnect the transistors. The transistors themselves are below the metal and are not visible in the micrograph. At this rate of progress, gigabit chips with 0.25-μm features will be seen by the time you read this book.

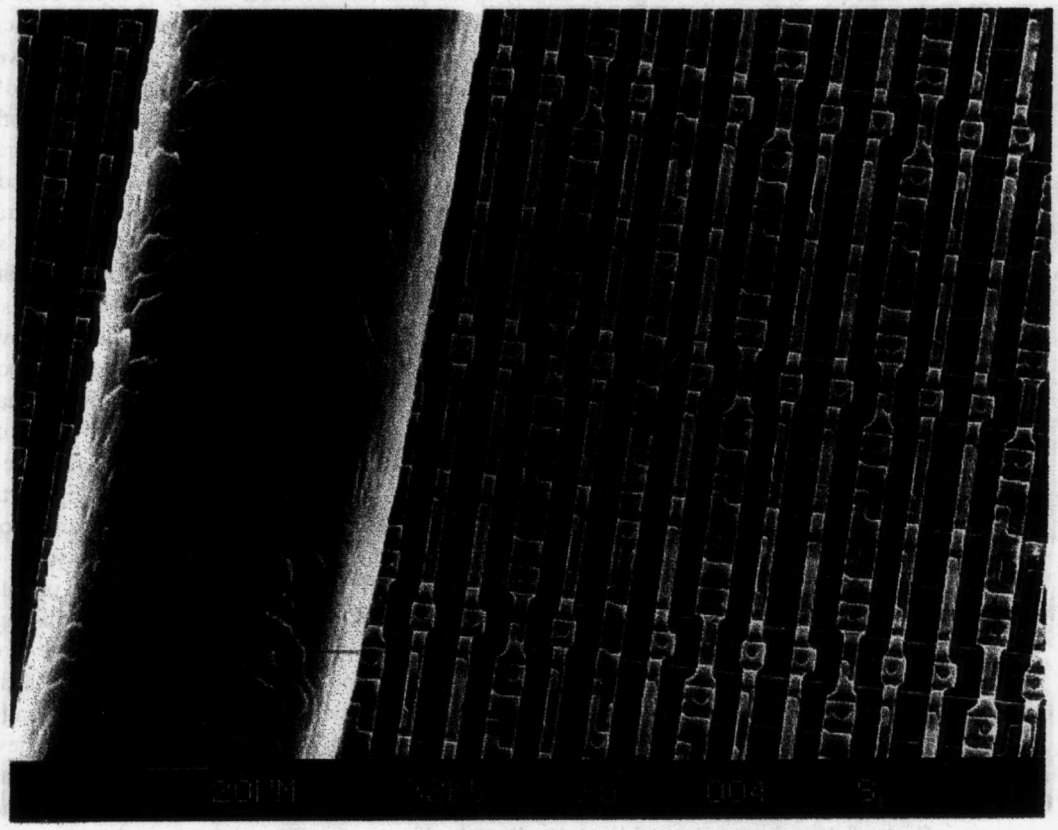

Figure 1.2 Scanning electron micrograph (SEM) of an IC circa mid-1980s. The visible lines correspond to metal wires connecting the transistors.

At first glance, these incredible densities and the associated design complexity would seem extremely daunting. This book, however, will focus on how these circuits are built rather than how they are designed or how the transistors operate. The fabrication process is similar no matter how many transistors are on the chip. The first half of the book will cover the basic operations required to build an IC. Using mechanical construction as an analogy, these would include steps such as forging, cutting, bending, drilling, and welding. These steps will be called unit processes in this text. If one knows how to do each of these steps for a certain material (e.g., steel), and if the machines and material required are available, they could be used to make a ladder, or a high-pressure cylinder, or a small ship. The required number and order of the steps will clearly depend on what is being built, but the basic unit processes remain the same. Furthermore, once a sequence that produces a good ship has been worked out, other ships of similar design could probably be built with the same process. The design of the ship, that is, what goes where, is a separate task. The shipbuilder is handed a set of blueprints to which he or she must build.

The collection and ordering of these unit processes for making a useful product will be called a *technology*. Part V of the book will cover some of the basic fabrication technologies. Whether the technology is used to make microprocessors, I/O controllers, or any other digital function is largely immaterial to the fabrication process. Even many analog designs can be built using a technology very similar to that used to build most digital circuits. An IC, then, starts with a need for some sort of electronic device. A designer or group of designers translates the requirements into a circuit design; that is, how many transistors, resistors, and capacitors must be used, what values they must have, and how they must be interconnected. The designer must have some input from the fabricator. In the shipbuilding example, the blueprints must somehow reflect the limitation that the shipbuilder cannot put rivets over weld joints or use small rivets and still expect them to hold very high pressures. The builder must therefore give the designer a document that says what can and cannot be done. In microelectronics this document is called the *design rules* or *layout rules*. They specify how small or large some features can be or how close two different features can be. If the design conforms to these rules, the chip can be built with the given technology.

1.1 Microelectronic Technologies: A Simple Example

Instead of blueprints, the circuit designer hands the IC fabricator a set of photomasks. The photomasks are a physical representation of the design that has been produced in accordance with the layout rules. As an example of this interface, assume that a need exists for an IC consisting of a simple voltage divider as shown in Figure 1.3. The technology to build this design is shown in Figure 1.4. Silicon wafers will be used as the substrate since they are flat, reasonably inexpensive, and most IC processing equipment is set up to handle them. The production of these substrates will be discussed in Chapter 2. Since the wafer is at least somewhat conductive, an insulating layer must first be deposited to prevent leakage between adjacent resistors. Alternatively, a thermal oxide of silicon could be grown, since it is an excellent insulator. The thermal oxidation of silicon is covered in Chapter 4. Next a conducting layer is deposited that will be used for the resistors. Several techniques for depositing both insulating and conducting layers will be discussed in Chapters 12–14.

This conducting layer must be divided up into individual resistors. This can be done by removing portions of the conducting layer, leaving rectangles of the film that are isolated from each other. The resistor value is given by

$$R = \rho \frac{L}{W \cdot t}$$

where ρ is the material resistivity, L is the resistor length, W is the resistor width, and t is the thickness of the layer. The designer can therefore select different values of resistors by choosing the width to

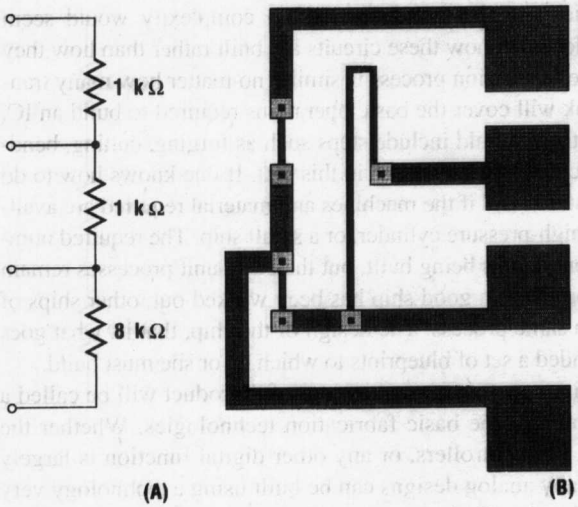

Figure 1.3 A simple resistor voltage divider. At left is a circuit representation: at right is a physical layout. The layers shown at right are resistor, contact, and low-resistance metal.

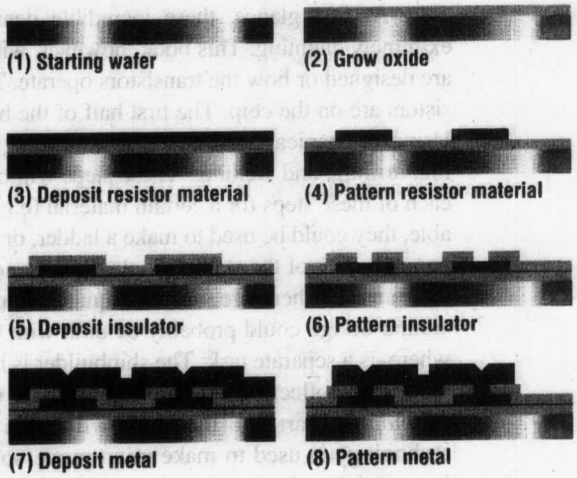

Figure 1.4 The technology flow for fabricating the resistor IC shown in Figure 1.3.

length ratio, subject to the limits specified by the layout rules. The technologist chooses the film thickness and the material (and therefore ρ) to give the designer an appropriate range of resistivities without forcing him to resort to extreme geometries. Since ρ and t are determined during the fabrication and are approximately constant across a wafer, the ratio ρ/t is more often specified than ρ or t individually. This ratio is called the *sheet resistance*, ρ_s. It has units of $\Omega/\square$ where the number of squares is the ratio of the length to width of the resistor line.

The resistor information from the design, namely L and W for each resistor, must be transferred from the photomask to the wafer. This is done using a process called *photolithography*. The most commonly used type of photolithography is *optical lithography*. In this process, a photosensitive layer called *photoresist* is first spread on the wafer (Figure 1.5). Light shining through the mask exposes the resist in the regions of the wafer where some of the metal resistor layer must be removed. In these exposed regions, a photochemical reaction occurs in the resist that causes it to be easily dissolved in a developer solution. After the develop step, the photoresist remains only in the areas where a resistor is desired. The wafer is then immersed in an acid that dissolves the exposed metal layer but does not significantly attack the resist. When the etch is complete, the wafers are removed from the acid bath, rinsed, and the photoresist is removed. The photolithographic process will be covered in Chapters 7 through 9. Chapter 11 will cover etching.

Although the resistors have now been formed, they still need to be interconnected and metal lines must be brought to the edge of the chip, where they can later be attached to metal wires for contact to the external world. This latter operation, called *packaging*, will not be covered in this text. If the metal lines have to cross over the resistors, another insulating layer must be deposited. To make electrical contact to the resistors, one can open up holes in the insulating layer using the same photolithographic and etch processes we had used for patterning the resistors, although the composition of the acid bath may be different. Finally, the fabrication sequence can be completed by depositing a