



# **Systematic Design of Analog CMOS Circuits**

**Using Pre-Computed Lookup Tables**

**Paul G. A. Jespers and  
Boris Murmann**



**Willy Sansen, KU Leuven** 

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**Bernhard Boser, University of California, Berkeley**

"This book fixes what has been broken with analog design for more than twenty years. I recommend it to experts and novices alike."

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Discover a fresh approach to efficient and insight-driven analog integrated circuit design in nanoscale-CMOS with this hands-on guide.

- Expert authors present a sizing methodology that employs SPICE-generated lookup tables, enabling close agreement between hand analysis and simulation.
- Illustrates the exploration of analog circuit tradeoffs using the  $g_m/I_D$  ratio as a central variable in script-based design flows, captured in downloadable Matlab code.
- Includes over forty detailed worked examples, including the design of low-noise and low-distortion gain stages, and operational transconductance amplifiers.

Whether you are a professional analog circuit designer, a researcher, or a graduate student, this book will provide you with the theoretical know-how and practical tools you need to acquire a systematic and re-use oriented design style for analog integrated circuits in modern CMOS.

**Paul G. A. Jespers** is a Professor Emeritus of the Université Catholique de Louvain and a Life Fellow of the IEEE.

**Boris Murmann** is a Professor of Electrical Engineering at Stanford University, and a Fellow of the IEEE.



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“Analog design generates insight, but requires expertise. To build up such expertise, analytic models are used to create design procedures. Indeed, analytic models easily allow device sizing from specifications. They lack accuracy, however. The models of present-day nanometer MOS transistors have become rather complicated. On the other hand SPICE simulations do provide the required accuracy but don’t generate as much insight. The use of SPICE-generated lookup tables, as described in this book, provides an excellent compromise. The accuracy is derived from SPICE and the design procedure itself is made through MATLAB employing parameters like  $g_m/I_D$ . As a result a considerable amount of intuition can be built up. Such design procedure is highly recommended to whoever wants to gain insight by doing analog design, without losing the accuracy of real SPICE simulations.”

**Willy Sansen, KU Leuven**

“With the advent of sub-micron MOS transistors more than two decades ago, traditional design based on the square-law model is no longer adequate. Alternatives such as ‘tweaking’ with SPICE or relying on more sophisticated device models do not provide the circuit insight necessary for optimized design or are too mathematically complex.

The design methodology presented in this book overcomes these shortcomings. A focus on fundamental design parameters – dynamic range, bandwidth, power dissipation – naturally leads to optimized solutions, while relying on transistor data extracted with the simulator ensures agreement between design and verification. Comprehensive design examples of common blocks such as OTAs show how to readily apply these concepts in practice.

This book fixes what has been broken with analog design for more than twenty years. I recommend it to experts and novices alike.”

**Bernhard Boser, University of California, Berkeley**

“The authors present a clever solution to capture the precision of the best MOSFET models, current or future, in a comprehensive and efficient design flow compatible with nanometric CMOS processes. In this book, you will also enjoy a wealth of invaluable information to deepen your analog design skills.”

**Yves Leduc, Polytech Nice Sophia**

**To my granddaughter Zérane  
PGAJ**

**To my wife Yukiko  
BM**





# Symbols and Acronyms

$A_v$	Small-signal voltage gain
$A_{v0}$	Low frequency small-signal voltage gain
$A_{intr}$	Intrinsic gain
$A_{VT}$	Pelgrom coefficient for threshold voltage mismatch
$A_\beta$	Pelgrom coefficient for current factor mismatch
ACM	Advanced Compact Model
CLM	Channel Length Modulation
CSM	Charge Sheet Model
$C$	Capacitor value
$C_{ox}$	Oxide capacitance per unit area
$C_{gb}$	Gate-to-bulk capacitance
$C_{gd}$	Gate-to-drain capacitance
$C_{gs}$	Gate-to-source capacitance
$C_j$	Junction capacitance
$C_C$	Compensation capacitance
CMOS	Complementary Metal Oxide Semiconductor
$C_{self}$	Self-loading capacitance of an amplifier
$D$	Diffusion constant
DIBL	Drain-Induced Barrier Lowering
EKV	Enz, Krumenacher and Vittoz compact model
FO	Fan-out (ratio between load and input capacitances of a circuit)
$f$	Frequency in Hz
$f_c$	Cutoff frequency ( $-3\text{dB}$ frequency)
$f_T$	Transit frequency
$f_u$	Unity gain frequency (where $ A_v  = 1$ )
$g_{ds}$	Output conductance
$g_m$	Gate transconductance
$g_{mk}$	$k^{\text{th}}$ derivative of $I_D$ with respect to $V_{GS}$
$g_{mb}$	Bulk transconductance
$g_{ms}$	Source transconductance
HD <sub>2</sub> , HD <sub>3</sub>	Fractional harmonic distortion of order 2, 3, ...
$i$	Normalized drain current
IGS	Intrinsic Gain Stage

$I_D$	DC drain current
$I_S$	Specific current
$I_{Ssq}$	Square specific current ( $W = L$ )
$I_{Su}$	Unary specific current ( $W = 1 \mu\text{m}$ )
$J_D$	Drain current density ( $I_D/W$ )
$L$	Gate length
$N$	Impurity concentration
$n$	Subthreshold slope factor
$q$	Normalized mobile charge density
$q_S, q_D$	Normalized mobile charge density at the source and drain
$Q_i$	Mobile charge density
RHP	Right Half Plane
$S_{VT0}$	Threshold voltage sensitivity factor with respect to $V_{DS}$
$S_{IS}$	Specific current sensitivity factor with respect to $V_{DS}$
$U_T$	Thermal voltage $kT/q$
$V_X$	DC voltage component at node x
$v_x$	AC voltage component at node x
$v_X$	Total voltage at node x, $v_X = V_X + v_x$
$V_{EA}$	Early voltage
$V_I$	DC component of input voltage
$v_i$	AC component of input voltage
$v_I$	Total input voltage $v_I = V_I + v_i$
$v_{id}$	Differential input voltage, AC component
$V_S, V_G, V_D$	Source, gate and drain voltage with respect to bulk (DC)
$V_{GS}, V_{DS}$	Gate and drain voltage with respect to the source (DC)
$v_{gs}, v_{ds}$	Incremental gate and drain voltage with respect to the source
$v_{gs,pk}, v_{ds,pk}$	Incremental gate and drain voltage amplitude (sinusoid)
$V_P$	Pinch-off voltage with respect to the bulk
$V_{Dsat}$	Drain saturation voltage
$v_{sat}$	Saturation velocity of mobile carriers
$V_T$	Threshold voltage
$V_{OV}$	Gate overdrive voltage, $V_{GS} - V_T$
$W$	Transistor width
WI, MI, SI	Weak, moderate and strong-inversion
$\beta$	Current factor <sup>1</sup> ( $\mu C_{ox} W/L$ )
$\gamma$	Backgate effect parameter
$\gamma_n, \gamma_p$	Thermal noise factor for n-channel and p-channel devices <sup>2</sup>
$\mu$	Mobility
$\mu_o$	Low-field mobility
$\rho$	Normalized transconductance efficiency

<sup>1</sup> The symbol  $\beta$  is also used to denote the feedback factor in amplifier circuits. The distinction is usually clear from the context.

<sup>2</sup> The distinction from the backgate effect parameter  $\gamma$  is usually clear from the context.



$\psi_s$	Surface potential
$\omega$	Angular frequency ( $2\pi f$ )
$\omega_c$	Angular cutoff frequency ( $2\pi f_c$ )
$\omega_T$	Angular transit frequency ( $2\pi f_T$ )
$\omega_{Ti}$	Angular transit frequency considering only $C_{gs}$ (instead of $C_{gg}$ )

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