国外电子信息精品著作(影印版)

系统集成：从晶体管设计到大规模集成电路

System Integration: From Transistor Design to Large Scale Integrated Circuits

Hoffmann K.

科学出版社
www.sciencep.com

国外电子信息精品著作（影印版）

系统集成：从晶体管设计到大规模集成电路

Hoffmann K.

科学出版社
北京

图字：01-2006-7266

内 容 简 介

本书涉及集成电路组件的集成和设计的较宽范围的内容，提供给读者用简单公式估计晶体管几何尺寸和推演电路行为的方法。本书广泛覆盖场效应管的设计、MOS管的建模和数字CMOS集成电路设计基础以及MOS存储器结构和设计。本书突出了片上系统设计和集成方面知识的需求，在单本书中覆盖半导体物理学、数字VLSI设计和模拟集成电路，介绍了集成电路半导体组件的基本行为和基于CMOS与BiCMOS工艺的数字和模拟集成电路的设计。

图书在版编目(CIP)数据

系统集成：从晶体管设计到大规模集成电路：英文/（德）霍夫曼编著. —影印版. —北京：科学出版社，2007.1
（国外电子信息精品著作）

ISBN 978-7-03-018255-5

Ⅰ.系… Ⅱ.霍… Ⅲ.集成电路-研究-英文 Ⅳ.TN4

中国版本图书馆CIP数据核字(2006)第149503号

责任编辑：余 丁/责任印制：安春生/封面设计：陈 敬

科学出版社出版
北京东黄城根北街16号
邮政编码：100717
http://www.sciencep.com

天时彩色印刷有限公司印刷

科学出版社发行 各地新华书店经销

*

2007年1月第 一 版 开本：B5(720×1000)
2007年1月第一次印刷 印张：32
印数：1—3 000 字数：803 000

定价：66.00元

（如有印装质量问题，我社负责调换〈双青〉）

《国外电子信息精品著作》序

20世纪90年代以来，信息科学技术成为世界经济的中坚力量。随着经济全球化的进一步发展，以微电子、计算机、通信和网络技术为代表的信息技术，成为人类社会进步过程中发展最快、渗透性最强、应用面最广的关键技术。信息技术的发展带动了微电子、计算机、通信、网络、超导等产业的发展，促进了生命科学、新材料、能源、航空航天等高新技术产业的成长。信息产业的发展水平不仅是社会物质生产、文化进步的基本要素和必备条件，也是衡量一个国家的综合国力、国际竞争力和发展水平的重要标志。在中国，信息产业在国民经济发展中占有举足轻重的地位，成为国民经济重要支柱产业。然而，中国的信息科学支持技术发展的力度不够，信息技术还处于比较落后的水平，因此，快速发展信息科学技术成为我国迫在眉睫的大事。

要使我国的信息技术更好地发展起来，需要科学工作者和工程技术人员付出艰辛的努力。此外，我们要从客观上为科学工作者和工程技术人员创造更有利于发展的环境，加强对信息技术的支持与投资力度，其中也包括与信息技术相关的图书出版工作。

从出版的角度考虑，除了较好较快地出版具有自主知识产权的成果外，引进国外的优秀出版物是大有裨益的。洋为中用，将国外的优秀著作引进到国内，促进最新的科技成就迅速转化为我们自己的智力成果，无疑是值得高度重视的。科学出版社引进一批国外知名出版社的优秀著作，使我国从事信息技术的广大科学工作者和工程技术人员能以较低的价格购买，对于推动我国信息技术领域的科研与教学是十分有益的事。

此次科学出版社在广泛征求专家意见的基础上，经过反复论证、仔细遴选，共引进了接近30本外版书，大体上可以分为两类，第一类是基础理论著作，第二类是工程应用方面的著作。所有的著作都涉及信息领域的最新成果，大多数是2005年后出版的，力求“层次高、内

容新、参考性强”。在内容和形式上都体现了科学出版社一贯奉行的严谨作风。

当然，这批书只能涵盖信息科学技术的一部分，所以这项工作还应该继续下去。对于一些读者面较广、观点新颖、国内缺乏的好书还应该翻译成中文出版，这有利于知识更好更快地传播。同时，我也希望广大读者提出好的建议，以改进和完善丛书的出版工作。

总之，我对科学出版社引进外版书这一举措表示热烈的支持，并盼望这一工作取得更大的成绩。

中国科学院院士

中国工程院院士

2006 年 12 月

Preface

This book is based on one with the title *VLSI Design*, published by Oldenbourg for the first time in 1990 and followed by four further editions. A substantially revised version with the title *System Integration* was published by Oldenbourg in 2003 and is the basis for this book. It includes lectures which the author teaches at the Bundeswehr University in Munich for graduate students and topics for adult education of professional engineers and physicists.

In order to introduce the book it is appropriate to consider more closely the history of silicon integrated circuits and how the design environment has changed over the years.

The development began with the integration of a couple of bipolar transistors on a piece of silicon. A similar development with field effect (MOS) transistors started later because of several technical problems. The number of integrated MOS circuits produced increased over the years enormously, compared to the number of bipolar circuits. The better chip area utilization together with simplified processes and circuits with reduced power consumption are some reasons for this development.

Due to a dramatic reduction in geometries and the availability of n-channel and p-channel transistors simultaneously on the same chip in so-called CMOS technologies, it is now possible to integrate millions of MOS transistors to a system on one chip.

This trend to ever-increasing chip density is going to continue in the foreseeable future, whereby physical constraints are probably not a limiting factor. It is more likely that the increase in complexity, in conjunction with production costs, will slow down this development.

CMOS processes are today and will be in the future mainstream technologies for integrating complex systems on chips. Despite this, bipolar technologies with a lower level of integration offer attractive solutions to the designer, particular in the area of analog and high frequency designs. These options are especially appealing when a BICMOS technology is available. The advantages of using bipolar and MOS transistors simultaneously in innovative designs of large scale integrated circuits are manifold.

The development of large scale integrated systems on a chip has changed the environment of circuit designers dramatically over the years. Initially hand calculations were sufficient to design a circuit. This became extremely troublesome with the ever-increasing transistor count. The situation was eased by the introduction of circuit simulation programs. But the number of transistors per chip continued to increase. The testing of the design, e.g. for electrical parameters, electrical rules, or the layout for design rule violations prior to production, became a problem. This conflict was eased

with the introduction of appropriate CAD tools. Unfortunately other handicaps unfolded. The technologies became more complex due to the continued scaling of transistor geometries. New effects had to be taken into account in the design. This meant further that the accuracy of the transistor models used in the circuit simulation programs was no longer sufficient. As a consequence, many improved transistor models were developed and will be developed and adopted to each new technology. A further implication of the scaled transistor geometries is that quality and lifetime questions of a product gain more and more significance, not to mention the testing of these properties.

It is obvious from this discussion, that not one designer but a whole team of specialists has to be available to cope with the challenges. If something is overlooked in the design phase, the IC might not work or work only at a particular voltage, temperature, and timing condition – an undesirable situation, as the system has to be analyzed and a redesign started.

To cope with the mentioned or similar problems it is necessary to understand thoroughly the physical interrelationship between the function of integrated circuit components like transistors and their impact on circuit performance in an integrated system.

The reader is thus introduced in the first four chapters to the basic behavior and design of modern semiconductor components of integrated circuits.

With this background, the design of digital and analog circuits is presented in the six following chapters, with the emphasis on CMOS implementations. One goal of these chapters is to derive simple equations for an estimate of transistor performance, geometry sizing, and circuit behavior. If one starts a design without this information the possibility exists that an inappropriate circuit will be selected, innovations be suppressed or unnecessary simulation runs performed without the desired success. Or if one starts a failure analysis and in due cause a redesign without this knowledge, a wrong conclusion may be drawn.

Acknowledgments

The author would like to thank all those who contributed to the manuscript and its correction. These are the members of the Bundeswehr University, Munich, Dr Kowarik, Dr Kraus, and Dr Pfeiffer, and the graduate students, who were an invaluable help in providing ideas for ease of complex presentations. The artwork was done excellently by Mr W. Barth. The author is also deeply grateful to many colleagues at Siemens and Infineon for their contribution.

Finally, I would like to express my extreme gratitude to my wife Gisela for doing excellent proofreading and for enduring the long months while this book was being written. She has been a constant support and help during the writing of this manuscript.

Kurt Hoffmann
Munich, Germany

Physical Constants and Conversion Factors

Conversion factors

$1\,\text{eV} = 1.602 \cdot 10^{-19}\,\text{J [Ws]}$

$1\,\text{m} = 10^{3}\,\text{mm} = 10^{6}\,\mu\text{m} = 10^{9}\,\text{nm}$

$1\,\text{F} = 10^{6}\,\mu\text{F} = 10^{9}\,\text{nF} = 10^{12}\,\text{pF} = 10^{15}\,\text{fF}$

Physical constants

Symbol	Parameter	Value
Q	Magnitude of electronic charge	$1.602 \cdot 10^{-19}\,\text{C [As]}$
k	Boltzmann constant	$1.38 \cdot 10^{-23}\,\text{JK}^{-1}\,[\text{Ws K}^{-1}]$
$kT/q = \phi_t$	Temperature voltage	0.026 V at 300 K
ε_0	Permittivity of free space	$8.854 \cdot 10^{-14}\,\text{Fcm}^{-1}$
ε_{ox}	Dielectric constant of silicon dioxide	3.9

Important electrical properties of semiconductors

	Ge	Si	GaAs	Unit
Band-gap E_G	0.66	1.12	1.42	eV
Dielectric constant ε_r	16	11.9	13.1	
Intrinsic carrier concentration n_i	$2.4 \cdot 10^{13}$	$1.45 \cdot 10^{10}$	$1.79 \cdot 10^{6}$	cm^{-3}
Effective density of states				
Conduction band N_C	$1.04 \cdot 10^{19}$	$2.8 \cdot 10^{19}$	$4.7 \cdot 10^{17}$	cm^{-3}
Valence band N_V	$6.0 \cdot 10^{18}$	$1.04 \cdot 10^{19}$	$7.0 \cdot 10^{18}$	cm^{-3}

Symbols

Symbol	Description	Units
General		
C	Capacitance	F
C'	Capacitance per area	Fm^{-2}
C^*	Capacitance per perimeter	Fm^{-1}
Q	Charge	C
ρ	Charge per volume	Cm^{-3}
σ	Charge per area	Cm^{-2}
ϕ	Semiconductor voltage	V
V	Applied voltage	V
Detail		
A	Area	m^2
a, (a_o)	Small-signal gain v_o/v_i (at $\omega \to 0$)	
B_F, B_R	Current gain; forward, reverse	
BV	Breakdown voltage	V
b_E	Emitter width	m
C_d	Diffusion capacitance	F
C_{gdo}, C_{gso}	Overlap capacitance: gate drain, gate source	F
C_j, (C_{jo})	Depletion capacitance (at $V_{PN} = 0\,V$)	F
C_{be}, C_{bc}	BE- and BC-capacitance	F
C_{je}, C_{jc}	BE- and BC-depletion capacitance	F
C_{jeo}, C_{jco}	BE- and BC-depletion capacitance at $V = 0\,V$	F
C'_{ox}	Oxide capacitance per area	Fm^{-2}
D	Electrical displacement	Cm^{-2}
D_n, D_p	Diffusion coefficient: electrons, holes	m^2/s
d_{ox}	Oxide thickness	m
$\mathcal{E}$	Electrical field	Vm^{-1}
E_F, E_C, E_V	Energy: Fermi level, conduction and valance band edge	eV
E_i	Electron energy at intrinsic Fermi level	eV
E_G	Band-gap	eV
E_{ox}, E_{Si}	Electrical field: oxide, silicon	Vm^{-1}
F	Probability of occupation by an electron	
f, f_T	Frequency, transit frequency	1/s
G	Rate of generation of electron–hole pairs	$1/m^3\,s$
g_o	Conductance	Ω^{-1}
g_m	Transconductance (gate)	Ω^{-1}

Symbol	Description	Units
g_{mb}	Transconductance (substrate)	Ω^{-1}
g_π	Input conductance	Ω^{-1}
I	Current	A
I_C, I_E, I_B	Current: collector, emitter, base	A
I_{Co}	Collector current at $V_{BC} = 0\,V$	A
I_{KF}, I_{KR}	Knee current: forward, reverse	A
I_S	Saturation current	A
I_{SS}, (I_{SSo})	Transport current ($V_{BC} = 0\,V$)	A
I_{DS}	Drain source current	A
J_n, J_p	Current density: electrons, holes	Am^{-2}
k	Boltzmann constant	$1.38 \cdot 10^{-23}\,JK^{-1}$
k_n, k_p	Gain factor of the process: n-channel, p-channel	AV^{-2}
L	Length, channel length (drawn)	m
l_E	Emitter length	m
l	Effective channel length	m
M	Grading coefficient	
N	Emission coefficient	
N_A, N_D	Acceptor and donor density	m^{-3}
N_C, N_V	Effective density of states: conduction band, valence band	m^{-3}
n_o, p_o	Density at equilibrium: electrons, holes	m^{-3}
n_n, p_n	Density in n-doped region: electrons, holes	m^{-3}
n_{no}, p_{no}	Density at equilibrium in n-doped region: electrons, holes	m^{-3}
n_p, p_p	Density in p-doped region: electrons, holes	m^{-3}
n_{po}, p_{po}	Density at equilibrium in p-doped region: electrons, holes	m^{-3}
n_i	Intrinsic density of electrons and holes	m^{-3}
n_{iB}, n_{iE}	Intrinsic density: base, emitter	m^{-3}
n'_p	Excess electron density in p-doped region	m^{-3}
p'_n	Excess hole density in n-doped region	m^{-3}
P	Power dissipation	W
Q	Magnitude of electronic charge	$1.602 \cdot 10^{-19}\,C$
Q_p, Q_n	Charge: holes, electrons	C
Q_B, (Q_{Bo})	Base majority charge ($V_{BC} = 0\,V$)	C
R	Recombination factor	$1/m^3\,s$
R_E	Emitter resistor	Ω
R_B	Base resistor	Ω
R_C	Collector resistor	Ω
R_S	Sheet resistance	$\Omega/\square$
T	Temperature	K (°C)
t	Time	s
t_d	Delay time	s
t_r	Rise time	s
t_f	Fall time	s
t_S	Storage time, switching time	s
U	Netto generation rate	$1/m^3\,s$
V_{AF}, V_{AR}	Early voltage: forward, reverse	V
V_{BC}	Voltage between base and collector	V
V_{BE}	Voltage between base and emitter	V
V_{CC}, V_{DD}	Positive power-supply voltages	V

V_{CE}	Voltage between collector and emitter	V
V_{DS}	Voltage between drain and source	V
V_{FB}	Flat band voltage	V
V_{GB}	Voltage between gate and bulk	V
V_{GS}	Voltage between gate and source	V
V_I	Input voltage	V
V_{PN}	Voltage between p- and n-doped region	V
V_Q	Output voltage	V
V_{SB}	Voltage between source and bulk	V
V_{SS}	Negative power-supply voltage	V
V_{Ton}, V_{Top}	Threshold voltage: n- and p-channel transistor ($V_{SB} = 0\,V$)	V
V_{Tn}, V_{Tp}	Threshold voltage: n- and p-channel transistor	V
v_n, v_p	Average drift velocity: electrons, holes	m/s
v_{sat}	Saturation velocity	m/s
w	Effective MOS transistor width	m
w_E	Effective emitter length	m
x_d	Depletion region width of MOS transistor	m
x_j	Depth of source and drain diffusion	m
x_p, x_n	Width of depletion region: p-doped and n-doped region	m
x_B, (x_{Bo})	Base width ($V_{BC} = 0\,V$)	m
Z	Inverter sizing parameter	
β	Small-signal current gain i_o/i_g or i_o/i_b	
β_n, β_p	Gain factor: n- and p-channel transistor	AV^{-2}
γ	Body-effect parameter	$V^{1/2}$
ε_0	Permittivity of free space	$8.854 \cdot 10^{-12}\,Fm^{-1}$
ε_{ox}	Dielectric constant of silicon dioxide	3.9
ε_{Si}	Dielectric constant of silicon	11.9
λ	Channel length modulation factor	V^{-1}
μ_n, μ_p	Mobility: electrons, holes	m^2/Vs
ρ_d	Depletion charge per volume	Cm^{-3}
ρ_B	Base resistivity	Ωm
σ_g	Gate charge per area	Cm^{-2}
σ_n	Inversion layer charge per area	Cm^{-2}
σ_d	Depletion region charge per area	Cm^{-2}
σ_{SS}	Interface charge per silicon/silicon-dioxide area	Cm^{-2}
σ	Conductance	$(\Omega m)^{-1}$
τ_T	Effective transit time	s
τ_n, τ_p	Effective transit time, lifetime: electrons, holes	s
τ_F, τ_R	Effective transit time: forward, reverse	s
ϕ_C	Channel voltage, contact voltage	V
ϕ_F	Fermi potential, Fermi voltage	V
ϕ_i	Built-in voltage	V
ϕ_{ox}	Voltage across oxide layer	V
ϕ_t	Thermal voltage kT/q	V
ϕ_S	Surface potential, surface voltage	V
ω	(Angular) frequency	1/s
ω_T	Unit-gain (angular) frequency	1/s
ω_p	−3 dB bandwidth, pole-(angular) frequency	1/s
ω_z	Zero-(angular) frequency	1/s

Contents