

Integrated Circuits and Semiconductor Devices: Theory and Application

second edition

**GORDON J. DEBOO
CLIFFORD N. BURROUS**

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Preface

The organization of this second edition is substantially the same as that of the first, and the changes reflect the results of a questionnaire completed by users of the first edition. There are two main differences between the two editions. The first is that many new topics have been introduced. For example, in response to the increasing use of digital technology in all areas of electronics, Chapter 5 now includes sections on microprocessors, CMOS, I²L, three-state logic, RAM/ROM memories, error detection and correction, encoders and code converters, multiplexers and demultiplexers, and additional LSI examples such as calculators and digital watches. Other chapters have been updated or expanded so that there are new sections on phase-locked loops, IC transducers, displays, and opto-isolators. The second difference is that many more worked examples have been added within the text.

The book covers virtually all semiconductor devices and ICs and is intended to serve two groups. The first group consists of electronics students at a number of different levels, including community and junior college, engineering technology, industrial training, and extension courses. The second group consists of practicing engineers, engineering technicians, physicists, and those in related fields who need to update their knowledge of electronic techniques involving semiconductor devices. For both groups, the book is a review of the basic theory and application of integrated circuits and semiconductor devices.

The material is based on an extremely popular course of a similar nature and purpose taught in the San Francisco Bay area by the authors. The text is frequently used in one of the last courses in a two- or four-year electronics-technology curriculum to complete the student's background in integrated circuits and semiconductor devices other than bipolar transistors. It is the authors' hope that the text will help close the gap between academic instruction and industrial practice, thereby better preparing students for their role in industry. The prerequisites for a course using this book include basic semiconductor physics, basic circuit analysis, and an introduction to transistors. A brief review of the hybrid- π approach to bipolar-transistor analysis is given in the appendix.

The book has five parts. First, junction and metal oxide semiconductor

field effect transistors are covered. The second part introduces integrated circuits, including operational amplifiers, other linear integrated circuits, digital integrated circuits, and integrated-circuit fabrication. Optoelectronic devices are dealt with in the third part, with subsections on light sources, displays, photodetectors, and source-detector combinations. The fourth part contains a chapter on thyristors such as silicon-controlled rectifiers and triacs. The last section covers miscellaneous semiconductors such as diodes and unijunction transistors.

A feature of the text is that the level of mathematics required is generally not above elementary algebra. Useful and valid approximations are used wherever possible to avoid obscuring principles with unwieldy mathematics. Examples are practical and often use data from actual data sheets. The book is up to date and comprehensive, yet written for the Community College level. A paperback instructor's guide is available to supplement the text. It contains problem solutions, instruction hints, and suggested experiments which can be performed with listed inexpensive versions of semiconductor devices, ICs, and conventional test equipment.

Many thanks are due Mr. Don Billings of NASA/Ames and Mr. Hans Sorenson of Hewlett-Packard, for their constructive criticism and suggestions regarding the second edition, and to the very helpful reviewers of the first edition.

Gordon J. Deboo
Clifford N. Burrous

Contents

Preface xi

FIELD EFFECT DEVICES

Chapter 1 Junction Field Effect Transistors 3

1-1 Introduction 3

1-2 Theory of operation 5

1-3 JFET parameters 11

Notation

Definitions

Parameter interrelationships

1-4 Biasing 20

1-5 Small-signal JFET amplifiers 23

Single-stage amplifiers

Effects of circuit capacitances on the different configurations

JFETs as FM-receiver front ends

JFET-bipolar combinations

Noise considerations in using JFETs

1-6 JFET switching circuits 41

1-7 JFETs as voltage-controlled resistors 46

1-8 Comparisons of n - and p -channel JFETs 48

Problems 49

Chapter 2 Metal Oxide Semiconductor Field Effect Transistors 51

2-1 Introduction 51

2-2 Theory of operation of the MOSFET 52

MOSFET fabrication and operation

MOSFET symbols

Gate breakdown

2-3 MOSFET parameters 57

2-4 Biasing 60

2-5 Circuits taking advantage of special MOSFET characteristics 62

MOSFETs as load resistors

Electrometers

Amplifiers for signals from high source impedances

MOSFETs as output devices

MOSFETs as choppers

The MOSFET at high frequencies

MOSFETs at very low temperatures

2-6 MOSFETs in integrated circuits 70

2-7 MOSFET, JFET, and bipolar-transistor comparison 71

Problems 73

INTEGRATED CIRCUITS

Chapter 3 Linear Integrated Circuits 79

3-1 Introduction 79

3-2 Integrated-circuit fabrication 79

3-3	Circuit design for linear integrated circuits	88
	General considerations	
	Current sources	
	Differential pairs	
3-4	LIC Applications	95
	Temperature-stabilized DC amplifiers	
	Phase-locked loops	
	MOS/bipolar amplifier	
	Integrated-circuit pressure transducers	
	Monolithic rms-voltage measuring device	
	Monolithic voltage regulators	
	Integrated-circuit multipliers	
3-5	High-frequency integrated circuits	108
	Video amplifiers	
	Intermediate-frequency amplifiers	
	Radio-frequency amplifiers	
3-6	Computer-aided design	111
	Problems	112
	References	114
Chapter 4	Operational Amplifiers	115
4-1	Introduction	115
4-2	The ideal operational amplifier	121
4-3	Analysis of operational-amplifier circuits	122
	The comparator	
	The voltage follower	
	The inverting amplifier	
	The noninverting amplifier	
	The summing amplifier	
	The subtracting amplifier	
	The integrator	
	The differentiator	
	A constant-amplitude phase shifter	
	RC-active filters	
	A linear rectifier	
	Instrumentation amplifiers	
4-4	Nonideal operational amplifiers	138
	Effect of finite open-loop gain	
	Effect of finite bandwidth	
	Effect of finite input resistance	
	Effect of nonzero output resistance	
	Effect of offset and drift	
	Effects of noise	
4-5	Types of operational amplifiers available	157
4-6	Miscellaneous operational-amplifier circuits	158
	Offset cancellation	
	Multiple inputs	
	Differentiator noise	
	Integrator drift	
	Nonlinear function generators	
	Logarithmic amplifiers	
	The gyrator	
	Operational-amplifier pulse circuits	

4-7	Summary of operational-amplifier formulas	166
4-8	Analysis of operational-amplifier circuits by inspection	168
	Problems	169

Chapter 5 Digital Integrated Circuits 175

5-1	Introduction	175
5-2	Basic building blocks	177
5-3	Integrated-circuit logic	192
	DCTL	
	RTL	
	RCTL	
	DTL	
	TTL	
	Schottky TTL	
	ECL	
	I ² L	
	P and NMOS logic	
	CMOS logic	
	Three-state logic	
	Practical considerations	
5-4	Integrated-circuit memories	213
5-5	Other integrated-circuit subsystems	224
	Introduction	
	Counters	
	Shift registers	
	Multiplexing	
	Decoding/demultiplexing	
	Encoders and code conversion	
	Arithmetic operations	
	Digital-to-analog and analog-to-digital conversion	
5-6	Integrated-circuit systems	252
	Digital voltmeter	
	Calculator	
	Digital watches and clocks	
5-7	Microprocessors	260
	Function of a microprocessor	
	Microprocessor design compared with random-logic design	
	Microprocessor software	
	A microprocessor application	
	Problems	266
	References	268

OPTOELECTRONICS

Chapter 6 Light Sources and Displays 271

6-1	Basic physics of light	271
6-2	Light sources	277
	Natural light sources	
	Incandescent lamps	
	Gas discharge lamps	
	Light-emitting diodes	
	Gas and ruby lasers	
	Semiconductor injection lasers	

6-3	Displays	303
	Digital-display-technology comparison	
	Digital-display decoding/driving and multiplexing	
	LED displays	
	Liquid-crystal displays	
	Problems	312
	References	314
Chapter 7	Photodetectors and Source-Detector Combinations	315
7-1	Photodetectors	315
	Basic photodetector parameters	
	Bulk photoconductors (photoresistors)	
	Photodiodes	
	Solar cells	
	Phototransistors	
	Photofield effect transistors	
	Photothyristors	
	Infrared detectors	
	Ultraviolet detectors	
	Photoposition detectors	
7-2	Source-detector combinations (opto-isolators)	350
	Bulk photoconductor opto-isolators	
	LED/phototransistor opto-isolators	
	Problems	356
	References	361

THYRISTORS

Chapter 8	Thyristors	365
8-1	Introduction—the thyristor family	365
8-2	Silicon-controlled rectifiers	371
	SCR theory of operation	
	SCR characteristics and ratings	
	SCR triggering and turn-off methods	
	SCR power-conversion circuits	
	SCR replacements for electromechanical devices	
	SCR motor speed control	
	SCR logic circuits	
8-3	The triac (bidirectional triode thyristor)	408
	Triac theory of operation	
	Triac characteristics, ratings, and nomenclature	
	Triac triggering and turn-off methods	
	Triac circuits	
8-4	Other thyristors	418
	Problems	418
	References	420

MISCELLANEOUS SEMICONDUCTOR DEVICES

Chapter 9	Miscellaneous Semiconductor Devices	423
9-1	Rectifier diodes	423
9-2	Zener diodes	427

9-3	Voltage-variable capacitance diodes	432
9-4	Schottky diodes	436
9-5	Unijunction transistors	437
	Introduction	
	Basic theory of operation	
	Nomenclature, characteristics, and structures	
	The UJT relaxation oscillator	
	UJT thyristor trigger circuits	
	Complementary unijunction transistors (CUJTS)	
	Programmable unijunction transistors (PUTS)	
	Comparison of UJTS	
	Problems	455
	References	458
Appendix	Bipolar-Transistor Circuit Analysis Using the Hybrid-Pi Equivalent Circuit	459
A-1	Hybrid-pi equivalent circuit	459
A-2	Some useful approximations	464
	Answers to Selected Problems	470
Index		473

part

1 field Effect Devices

chapter 1

Junction Field Effect Transistors

1-1 INTRODUCTION

The *field effect transistor (FET)* is a semiconductor device that combines the small size and low power requirements of the bipolar transistor with the high input impedance of the vacuum tube.

There are two kinds of FET, although within each classification there are many variations. In this chapter the abbreviation JFET will be used to denote the *junction field effect transistor*. The abbreviation MOSFET will be used to denote the *metal oxide semiconductor (MOS) FET*, which is discussed in Chap. 2. The differences between these two field effect devices will become apparent as the discussion proceeds.

In contrast to bipolar transistors, in which the controlling effect is a *current* (the base current), both JFETs and MOS devices have very small input currents, which are due to leakage effects. The controlling *effect* is a *field* produced by an input voltage, which is why JFETs and MOS devices are called *field effect* transistors.

Figure 1-1 is a comparison of the symbols for a JFET, a bipolar transistor, and a vacuum tube. Also included is the symbol for a diode. Whereas there is only one polarity for vacuum tubes, there are two polarities of JFET available, just as there are in the case of bipolar transistors. Figure 1-1a shows an *n*-channel JFET, a term that will be explained later. Consider the biasing of the input diode of each of the three devices. For the *n*-channel JFET shown, the gate (or input) is marked with an arrow, which indicates the polarity of the input diode. (For a *p*-channel device, the arrow would have been drawn in the opposite direction.) The symbol for a diode is given in Fig. 1-1d. If the anode is sufficiently positive with respect to the cathode, the diode will conduct. If the anode is not sufficiently positive or is negative with respect to the cathode, virtually no current will flow. The arrows on JFETs and bipolar transistors follow the same convention. For a silicon diode, about 0.6 V of positive bias is required for conduction.

From the typical voltages shown in Fig. 1-1a, it can be seen that the JFET input diode is reversed-biased, which produces a high input impedance. The situation is similar for the vacuum tube for which the grid is the anode of the input diode. In the case of the bipolar transistor, however, the arrow shows that the base-emitter diode is forward-biased, thereby giving rise to a relatively low

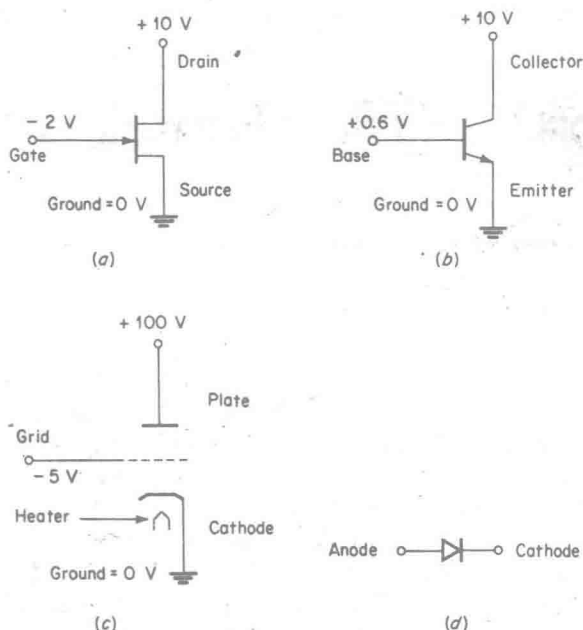


Fig. 1-1 JFET symbol compared with those for a bipolar transistor, a vacuum tube and a diode: (a) JFET (n -channel); (b) bipolar transistor; (c) vacuum tube; (d) diode.

input impedance. The input resistance of a JFET ranges from 10^8 to $10^{12}\ \Omega$, and for the bipolar transistor from about 10^2 to $10^6\ \Omega$.

In a broad sense the drain, gate, and source of a JFET correspond to the collector, base, and emitter of a bipolar transistor and to the plate, grid, and cathode of a vacuum tube. When biased as a voltage amplifier, there is current flow in a JFET from source to drain, and this current flow is controlled by the gate voltage. In a bipolar-transistor, which is a current-controlled device, the flow of current from emitter to collector is controlled by the base current. While it is true that a base voltage exists, the relationship between base current and collector current is more linear than that between base voltage and collector current. The JFET, like the vacuum tube, can be thought of as a voltage-controlled device because, when it is used as an amplifier, the gate or grid currents are for all practical purposes zero.

Although first described as early as 1954, the JFET was slow to come into general use, partly because of manufacturing difficulties and partly because of the rapid development of the bipolar transistor. The JFET has more than fulfilled its early promise and now finds application in virtually every phase of circuit design.

In addition to being a high-input-impedance, low-bias current amplifier, the JFET may be used as an analog switch, as a voltage-variable resistor, as a very high frequency amplifier with low cross-modulation distortion, and as a device with an adjustable temperature coefficient, which can be set to be positive, negative, or nearly zero.

1-2 THEORY OF OPERATION

JFETs operate by means of the creation and control of the *depletion layer* that exists in all reverse-biased *pn* junctions. Figure 1-2a represents an unbiased *pn* junction. The left-hand or *p* region has excess holes, which are available for conduction. The right-hand or *n* region has excess electrons, which are also available for conduction.

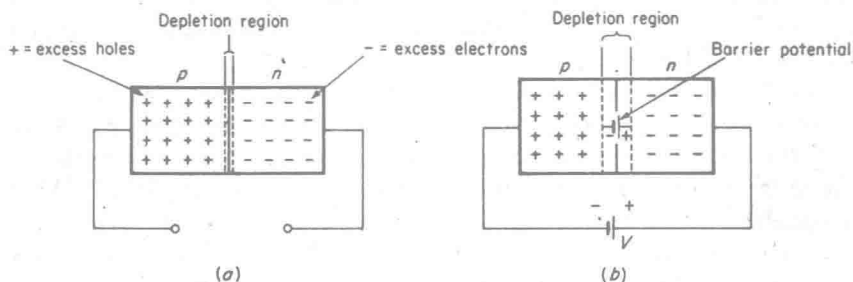


Fig. 1-2 Formation of a depletion region: (a) *pn* junction with no bias; (b) *pn* junction with bias.

There is a tendency for current carriers to diffuse from a region of high concentration to one of low concentration. Since there is a high concentration of electrons in the *n* region and a low concentration of electrons in the *p* region, electrons tend to diffuse from the *n* region to the *p* region. Similarly, holes tend to diffuse from the *p* region (high concentration of holes) to the *n* region (low concentration of holes). However, the *n* and *p* regions are both electrically neutral; so when electrons leave the *n* region, they “uncover” immobile positive ions, thereby leaving a net positive charge on the *n* side of the *pn* junction. Similarly, a net negative charge is created on the *p* side of the *pn* junction. Thus an internal “battery” or *barrier potential* is set up, and its polarity is such as to preclude further crossing of the junction by charge carriers. Therefore, diffusion of charge carriers is not complete, and instead there is a rearrangement of the holes and electrons within the crystal structure, which produces a narrow region *depleted* of charge carriers. This region is called a *depletion region*.

With no external bias applied as in Fig. 1-2a, the depletion region is very thin, and for purposes of explanation of JFET operation we can consider it negligibly thin. However, an externally applied reverse-biased potential (Fig. 1-2b) has the effect of *widening* the depletion region. This is because the + side of the external battery attracts electrons and “pulls” them away from the *n* side of the junction. Similarly, the - side of the battery “pulls” holes away from the *p* side of the junction. Thus the barrier potential or “height” is increased.

The significance of depletion regions as far as JFETs are concerned is that it is possible to electrically change the resistance of a piece of semiconductor material by changing the concentration of charge carriers with an externally

applied electric field. This is true even though there is no pn junction in the normal conduction path of a JFET, which is *along* the depletion region, not *across* the junction as in a bipolar transistor.

Conduction in JFETs is always by majority charge carriers only, which is why they are called *unipolar* transistors. This is in contrast to bipolar transistors, in which both majority and minority charge carriers are involved in current flow. Since there are two kinds of current carrier in semiconductors, electrons and holes, it is natural that there should be two polarities of JFET. Those employing electron conduction are called n types, and those employing hole conduction are called p types; n and p types are similar in their modes of operation except for reversal of all polarities.

A JEFT may be visualized (Fig. 1-3) as a conductive bar or channel, usually of silicon, at each end of which are ohmic contacts called the *source* and *drain*. (An ohmic contact is one not involving a pn junction.) A third ohmic contact is made to the material on either side of the channel, as shown in Fig. 1-3. When appropriately biased, the gate voltage influences the resistance between the source and the drain and hence the flow of current between these two terminals.

Figure 1-3 represents an n -channel device. The starting material is a piece of p -type silicon (A) into which is diffused an n -type region (B). A p region (C) is then diffused into the n region, leaving a thin channel of n material. Ohmic contacts for the source and drain are made by metallizations at each end of the n channel. This n channel is the conductive part of the device. With no voltages applied, the impedance between the source and drain will be an ohmic resistance, the resistance depending on the dimensions of the n channel. In fact, the resistance can be calculated as for any other resistor from the well-known formula

$$R = \frac{\rho L}{WT} \quad (1-1)$$

where ρ = resistivity of the material

L = length of the channel

W = channel width

T = channel thickness

L , W , and T are indicated on Fig. 1-3.

The third ohmic contact, the gate, is connected to both p regions. Notice that the gate and the channel form two pn junctions, and that the channel thickness t is the distance between the two transition regions from p to n material. Figure 1-4a is a two-dimensional representation of a cross section of the device shown in Fig. 1-3.

Application of a reverse gate-to-channel bias will produce a depletion layer at each transition region, as described earlier with the help of Fig. 1-2. The shape

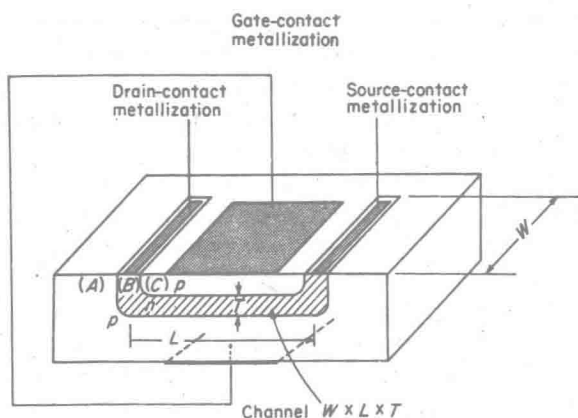


Fig. 1-3 JFET *n*-channel device showing connections to *p* and *n* regions.

and extent of the depletion regions and their effect depend on how much bias is applied and where. In Fig. 1-4 we shall assume that the drain-to-source voltage V_{DS} is positive, while the gate-to-source voltage V_{GS} is negative. These are appropriate bias polarities for an *n*-channel JFET. The same principles apply to a *p*-channel JFET, but with all polarities reversed.

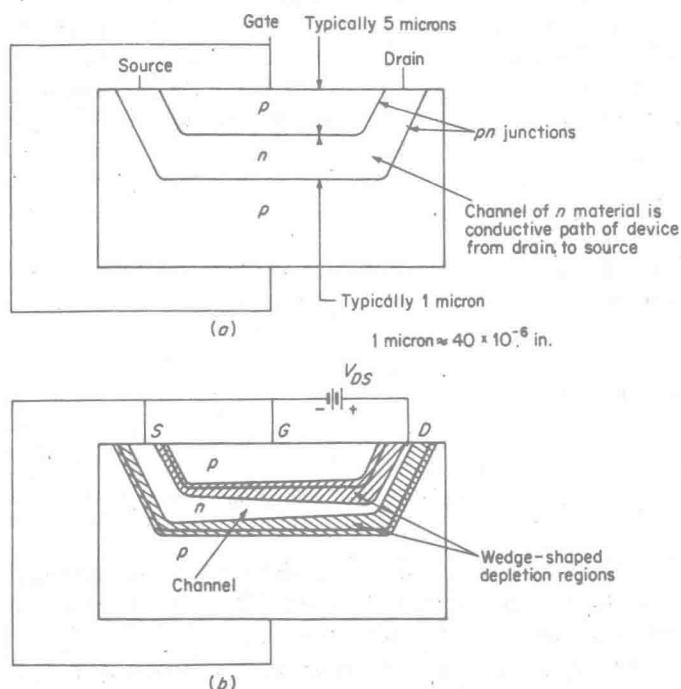


Fig. 1-4 Cross section of an *n*-channel JFET showing effect of bias on depletion regions: (a) no bias; (b) with bias.