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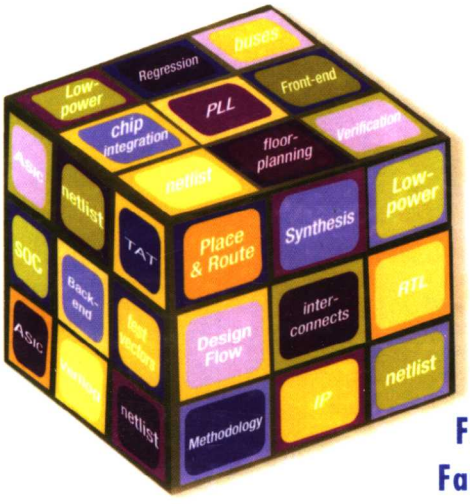
A Practical Approach



Farzad Nekoogar
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机械工业出版社
China Machine Press

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出版者的话

文艺复兴以降，源远流长的科学精神和逐步形成的学术规范，使西方国家在自然科学的各个领域取得了垄断性的优势；也正是这样的传统，使美国在信息技术发展的六十多年间名家辈出、独领风骚。在商业化的进程中，美国的产业界与教育界越来越紧密地结合，计算机学科中的许多泰山北斗同时身处科研和教学的最前线，由此而产生的经典科学著作，不仅擘划了研究的范畴，还揭橥了学术的源变，既遵循学术规范，又自有学者个性，其价值并不会因年月的流逝而减退。

近年，在全球信息化大潮的推动下，我国的计算机产业发展迅猛，对专业人才的需求日益迫切。这对计算机教育界和出版界都既是机遇，也是挑战；而专业教材的建设在教育战略上显得举足轻重。在我国信息技术发展时间较短、从业人员较少的现状下，美国等发达国家在其计算机科学发展的几十年间积淀的经典教材仍有许多值得借鉴之处。因此，引进一批国外优秀计算机教材将对我国计算机教育事业的发展起积极的推动作用，也是与世界接轨、建设真正的世界一流大学的必由之路。

机械工业出版社华章图文信息有限公司较早意识到“出版要为教育服务”。自1998年开始，华章公司就将工作重点放在了遴选、移译国外优秀教材上。经过几年的不懈努力，我们与Prentice Hall，Addison-Wesley，McGraw-Hill，Morgan Kaufmann等世界著名出版公司建立了良好的合作关系，从它们现有的数百种教材中甄选出Tanenbaum，Stroustrup，Kernighan，Jim Gray等大师名家的一批经典作品，以“计算机科学丛书”为总称出版，供读者学习、研究及庋藏。大理石纹理的封面，也正体现了这套丛书的品位和格调。

“计算机科学丛书”的出版工作得到了国内外学者的鼎力襄助，国内的专家不仅提供了中肯的选题指导，还不辞劳苦地担任了翻译和审校的工作；而原书的作者也相当关注其作品在中国的传播，有的还专程为其书的中译本作序。迄今，“计算机科学丛书”已经出版了近百个品种，这些书籍在读者中树立了良好的口碑，并被许多高校采用为正式教材和参考书籍，为进一步推广与发展打下了坚实的基础。

随着学科建设的初步完善和教材改革的逐渐深化，教育界对国外计算机教材的需求和应用都步入一个新的阶段。为此，华章公司将加大引进教材的力度，在“华章教育”的总规划之下出版三个系列的计算机教材：除“计算机科学丛书”之外，对影印版的教材，则单独开辟出“经典原版书库”；同时，引进全美通行的教学辅导书“Schaum's Outlines”系列组成“全美经典学习指导系列”。为了保证这三套丛书的权威性，同时也为了更好地为学校和老师们服务，华章公司聘请了中国科学院、北京大学、清华大学、国防科技大学、复旦大学、上海交通大学、南京大学、浙江大学、中国科技大学、哈尔

滨工业大学、西安交通大学、中国人民大学、北京航空航天大学、北京邮电大学、中山大学、解放军理工大学、郑州大学、湖北工学院、中国国家信息安全测评认证中心等国内重点大学和科研机构在计算机的各个领域的著名学者组成“专家指导委员会”，为我们提供选题意见和出版监督。

这三套丛书是响应教育部提出的使用外版教材的号召，为国内高校的计算机及相关专业的教学度身订造的。其中许多教材均已为M. I. T.，Stanford，U.C. Berkeley，C. M. U. 等世界名牌大学所采用。不仅涵盖了程序设计、数据结构、操作系统、计算机体系结构、数据库、编译原理、软件工程、图形学、通信与网络、离散数学等国内大学计算机专业普遍开设的核心课程，而且各具特色——有的出自语言设计者之手、有的历经三十年而不衰、有的已被全世界的几百所高校采用。在这些圆熟通博的名师大作的指引之下，读者必将在计算机科学的宫殿中由登堂而入室。

权威的作者、经典的教材、一流的译者、严格的审校、精细的编辑，这些因素使我们的图书有了质量的保证，但我们的目标是尽善尽美，而反馈的意见正是我们达到这一终极目标的重要帮助。教材的出版只是我们的后续服务的起点。华章公司欢迎老师和读者对我们的工作提出建议或给予指正，我们的联系方法如下：

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To our older brother Farhad, who opened the gate to great opportunities for both of us.

—Farzad and Faranak

List of Abbreviations

AAL1	ATM Adaptation Layer 1
AAL2	ATM Adaptation Layer 2
ABV	Assertion-Based Verification
AC	Alternating Current
ADC	Analog-to-Digital Converter
ADPCM	Adaptive Differential Pulse Code Modulation
ASIC	Application-Specific Integrated Circuit
ATM	Asynchronous Transfer Mode
ATPG	Automatic Test Pattern Generation
BFM	Bus Functional Model
BGA	Ball Grid Array
BIST	Built-In Self Test
CAD	Computer Aided Design
CELP	Code Excited Linear Predictive
CMOS	Complementary Metal Oxide Semiconductor
CODEC	COder/DECoder
CPCI	Compact Peripheral Component Interconnect
CTV	Cable TV
CVS	Concurrent Versions System
DAC	Digital-to-Analog Converter

DC	Direct Current
DDR	Double Data Rate
DDS	Digital Data Service
DFT	Design For Test
DIP	Dual In-Line Package
DLL	Digital Link Layer
DMA	Direct Memory Access
DRAM	Dynamic Random Access Memory
DRC	Design Rule Check
DSL	Digital Subscriber Line
DSM	Deep Sub-Micron
DSP	Digital Signal Processing/ Digital Signal Processor
DTMF	Dual-Tone Multi Frequency
DUT	Design Under Test
ECO	Engineering Change Orders
EDA	Electronic Design Automation
EDIF	Electronic Design Interchange Format
ERC	Electrical Rule Check
ESD	Electrostatic Discharge
FIFO	First-In First-Out
FPGA	Field Programmable Gate Array
FSM	Finite State Machine
GND	Ground
GPS	Global Positioning System
HDL	Hardware Description Language
HLB	Hierarchical Layout Block
HW/SW	Hardware/Software
ICs	Integrated Circuits
ILM	Interface Logic Models
IP	Intellectual Property
IP	Internet Protocol
IPO	In Place Optimization
IR	commonly refers to voltage drop from V = IR
ISDN	Integrated Services Digital Network
ITU	International Telecommunication Union
JTAG	Joint Test Action Group

K-maps	Karnaugh maps
LEC	Line Echo Canceller
LVS	Layout Versus Schematic
MAC	Media Access Control
MII	Media Independent Interface
MPEG	Moving Picture Experts Group
MPU	MicroProcessor Unit
MVIP	Multi Vendor Integration Protocol
NMOS	N-channel Metal-Oxide-Semiconductor
NRE	Non-Recurring Engineering
OCB	On-Chip Buses
OCP	Open Core Protocol
OIF	Optical Internetworking Forum
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect
PCM	Pulse Code Modulation
PGA	Pin Grid Array
PIP	Picture In Picture
PLL	Phase Locked Loops
PMOS	P-channel Metal-Oxide-Semiconductor
PSTN	Public Switched Telephone Network
PVT	Process, Voltage, and Temperature
QFP	Quad Flat Pack
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RCS	Revision Control System
RGB	Red-Green-Blue
RISC	Reduced Instruction Set Computer
RMII	Reduced Media Independent Interface
RT	Register Transfer
RTL	Register Transfer Level
SB	SiliconBackplane
SCSA	Signal Computing System Architecture
SDC	SDRAM Controller
SDF	Standard Delay Format
SDRAM	Synchronous Dynamic Random Access Memory

Serdes	Serializer/Deserializer
SFI	Serdes-to-Framer Interface
SI	Signal Integrity
SOC	System On a Chip
SOP	Small Outline Package
SPI-4P2	System Packet Interface Level 4 Phase 2
STA	Static Timing Analysis
STB	Set Top Box
STV	Satellite TV
TAT	Turn Around Time
TCP	Transfer Control Protocol
TDM	Time Division Multiplexing
TSI	Time Slot Interchange
TTM	Time To Market
UDP	User Datagram Protocol
USB	Universal Serial Bus
UTOPIA	Universal Test Operation PHY Interface for ATM
VAD	Voice Activity Detector
VC	Virtual Components
VCI	Virtual Component Interface
VHDL	VHSIC (Very high-speed integrated circuit) Hardware Description Language
VOCODER	Voice CODER
VoIP	Voice over IP
VoN	Voice over Network
VSIA	Virtual Socket Interface Alliance
WAN	Wide Area Network
WLM	Wire Load Models
xDSL	Digital Subscriber Line
XNF	Xilinx Netlist Format

Preface

The term SOC (system-on-a-chip) has been used in the electronic industry over the last few years. However, there are still a lot of misconceptions associated with this term. A good number of practicing engineers don't really understand the differences between ASICs and SOCs. The fact that the same EDA tools are used for both ASICs and SOCs design and verification doesn't help to reduce the misconceptions.

This book describes the practical aspects of ASIC and SOC design and verification. It reflects the current issues facing ASIC/SOC designers.

The following items characterize the book:

- It deals with everyday issues that ASIC/SOC designers have to face as opposed to generic textbook examples covered in other books.
- It emphasizes principles and techniques as opposed to specific tools. Once the designers understand the underlying principles of practical design, they can apply them with various tools.

- FPGAs will not be covered in this book. However, in Chapter 2 we cover a short section on FPGA to ASIC conversion. Earlier books have covered design and verification of FPGAs adequately.
- It provides tips and guidelines for front-end and back-end designs.
- Modern physical design techniques are covered.
- Low-power design techniques and methodologies are explored for both ASICs and SOCs.

This book is to be used for self-study by practicing engineers. Design and verification engineers who are working with ASICs and SOCs will find the book very useful. Upper-level undergraduate and graduate students in electrical engineering can use it as a reference book in courses in logic and chip design and related topics.

The material covered in the book requires understanding of EDA tools as well as front-end and back-end processes in chip design. An initial course in logic design is required.

The book is organized in the following fashion.

In Chapter 1 we introduce the goals of this manuscript. The differences between ASICs and SOCs are introduced. The concept of Intellectual Property (IP) is covered as well as an overview of design methodologies.

SOC design challenges such as integration of IPs are also covered.

A gateway VOIP (Voice Over IP) SOC example is given in this chapter.

Chapter 2 covers an overview of ASIC design concepts, methodology, and front-end design flow. Useful guidelines for hierarchical design methodology are presented such as placement-based synthesis and interface logic models. Some key questions that ASIC designers should consider when designing ASICs are presented. FPGA to ASIC conversion is covered in Section 2.3. An overview of verification and Design for Test (DFT) techniques are also presented in this chapter.

Chapter 3 continues with the VOIP SOC example from Chapter 1. Design for integration is covered in Section 3.2. Section 3.3 covers SOC verification planning guidelines such as resource planning and regression planning. Automation and IP verification are also covered in Section 3.3. This chapter ends with a detailed design example of a Set-Top Box (STB).

Chapter 4 covers an overview of the physical design flow. Some tips and guidelines for physical design are given such as logical vs. physical hierarchy, multiple placements and routing, and non-routable congested areas.

Two examples of modern physical-design techniques are presented in Section 4.4. These methods each overcome the problems associated with traditional physical design techniques.

In Chapter 5 we present low-power design techniques. In this chapter, sources of power dissipation in CMOS devices are discussed. Several methods of power optimization at various levels of abstraction for ASICS and SOCs are explained. These techniques include: algorithm-level optimization, architecture-level optimization, RT-level optimization, and gate-level optimization. Appendix A should be used in conjunction with this chapter.

Appendix A summarizes EDA low-power design tools from Sequence Design, Inc.

Appendix B gives an overview of OCP (Open Core Protocol) that is used as a core interface standard for IP integration.

Appendix C gives an introduction to Phase-Locked Loops which are widely used in almost all ASICs and SOCs.

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