计算机体系结构 I

COMPUTING: Software Development

HIGHER NATIONAL DIPLOMA

【英】苏格兰学历管理委员会（SQA）
Scottish Qualifications Authority

Unit Student Guide

Computer Architecture I **DG8F 04**

中国时代经济出版社

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计算机体系结构 Ⅰ

Computer Architecture 1

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Contents

1 Introduction to the Scottish Qualifications Authority

This Unit (DG8F 04 Computer Architecture 1) has been devised and developed by the Scottish Qualifications Authority (SQA). Here is an explanation of the SQA and its work:

The SQA is the national body in Scotland responsible for the development, accreditation, assessment, and certification of qualifications other than degrees.

Its website can be viewed on: www.sqa.org.uk

SQA's functions are to:

- devise, develop and validate qualifications, and keep them under review
- accredit qualifications
- approve education and training establishments as being suitable for entering people for these qualifications
- arrange for, assist in, and carry out, the assessment of people taking SQA qualifications

- quality assure education and training establishments which offer SQA qualifications

- issue certificates to candidates.

In order to pass SQA units, students must complete prescribed assessments. These assessments must meet certain standards.

The Unit Specification outlines the 3 Outcomes that students must complete in order to achieve this unit. The Specification also details the knowledge and/or skills required to achieve the outcome or outcomes. The Evidence Requirements prescribe the type, standard and amount of evidence required for each outcome or outcomes.

2 Introduction to the Unit

2.1 What is the Purpose of this Unit?

This Unit is designed to develop broad general knowledge and understanding of the theoretical concepts, principles, boundaries and scope of the mechanisms that underpin the use of digital computers. This includes the way in which the internal representation of data within the machine can be translated into output values which are meaningful to the user. Study of the Unit also provides a foundation knowledge of the mechanisms used by a processor to communicate with memory and external devices, how a processor deals with requests from external sources, and the characteristics and requirements of the devices that processors can be regularly expected to deal with. The study of the Unit will be of particular benefit to those who wish to undertake further study in the fields of computer programming, providing technical support to other users or new media production.

2.2 What are the Outcomes of this Unit?

Most computer data is represented numerically and in Outcome 1 you will learn how to convert values between different base number systems e.g.: denary, binary, hexadecimal, carry out arithmetic operations in these different base number systems and carry out Boolean Logic operations to process numerical data. You will also

learn how text characters are represented in computer storage.

In Outcome 2 you will learn about the following:

- The functional components of a computer system
- The physical and functional characteristics of memory
- Methods of communication between the CPU and peripheral devices
- Read/Write operations.

In **Outcome** 3 you will learn to identify all of the internal components of the CPU and to describe their function and operation. You will also discover how machine operations are organised and represented by analysing the Fetch/Execute cycle for given operations.

2.3 What do I Need to be Able to do in Order to Achieve this Unit?

Demonstrate an ability to manipulate and translate data representations.

Demonstrate an understanding of the functions of computer system components.

Demonstrate an understanding of the principles of Central Processor Unit (CPU) operation.

2.4 Approximate Study Time for This Unit

While the exact time allocated to this Unit is at the discretion of the Centre, the notational design length is 40 hours.

2.5 Equipment/Material Required for this Unit

- Physical samples of hardware including ROM, EPROM and RAM chips would be of benefit when studying Section 2. Ask your Tutor about these
- Similarly, physical samples of processor chips may be used to aid the delivery of Section 3
- You will require access to the Internet via a suitable PC or MAC computer as there are several references to websites throughout the learning materials.

2.6 Symbols Used in this Unit

The various Learning Materials sections are designed so that you can work at your own pace, with tutor support. As you work through the Learning Materials (see Chapter 5), you will encounter symbols. These symbols indicate that you are expected to do a task. **These tasks are not Outcome Assessments.** They are exercises designed to consolidate learning or encourage thought, in preparation for the Outcome Assessment (see Chapter 3—Assessment Information for this Unit).

Activity

This symbol indicates an Activity (A). In this Unit, you will be asked to undertake a variety of Activities (A). Usually, activities are used to improve or consolidate your understanding of the subject in general or a particular feature of it.

The activities will not serve this purpose if you refer to the responses prior to having attempted the Activity.

Self Assessed Question

This symbol indicates a Self Assessed Question. Using a Self Assessed Question helps you check your understanding of the content that you have already covered.

Everything is provided for you to check your own responses. Answers to the Self Assessed Questions are to be found at the back of the Unit Student Guide. Where suggested responses to activities are provided in the Unit Student Guide, **students are strongly discouraged from looking at these responses before they attempt the activity.** The activities throughout the Unit Student Guide will help you to prepare yourself for the formal assessments, and to identify topic areas in which you will require clarification and additional tutor support. The activities will not serve this purpose if you look at the answers before trying the activity!

Self Assessed Questions and activities are designed to be checked by you. No tutor input is necessary at this stage unless special help is requested, although from time to time your tutor may wish to view your responses to Self Assessed Questions to see how you are progressing.

3 Assessment Information for this Unit

3.1 What Do I Have to Do to Achieve This Unit?

To achieve this Unit you must pass the assessments for each Outcome.

Outcome 1

Evidence for all the knowledge and/or skills in this Outcome will be assessed using 20 multiple-choice questions. The questions presented must change on each assessment occasion. All Evidence Requirements must be covered at least ONCE with additional questions at the discretion of the centre.

1. Perform addition and subtraction between two binary values and two hexadecimal values not less than one byte long.

2. Convert

   - integer numbers in base ten (denary) to base sixteen (hexadecimal) and base sixteen to base ten
   - integer numbers in base ten (denary) to base two (binary) and base two to base ten
   - integer numbers in base two (binary) to base sixteen (hexadecimal)

- integer number in base sixteen (hexadecimal) to base two.

3. Apply standard Boolean operators (AND, OR, XOR and NOT) in relation to gates with binary inputs not less than eight bits.

4. Convert 7-bit ASCII text to binary, and binary values to 7-bit ASCII.

5. Convert modern character representations to characters and characters to modern character representations.

Outcome 2

Each candidate will be required to provide evidence of his/her knowledge and skills for the following:

1. Draw a block diagram of the major components of a computer system and bus connections describing the function of each block including the bus functions.

2. Describe the fundamental types of memory (RAM and ROM) that can be connected to a CPU and the reasons why they are included in a system. The candidate must provide a correct expansion of the name or acronym of at least five different types of memory. The list must be a sample of seven currently available types and must include (i) RAM, (ii) ROM, and could include (iii) DRAM, (iv)

PROM, (v) SRAM, (vi) EPROM, (vii) Flash memory. Describe the terms access speed and cycle time.

3. Differentiate between polling and interrupts as a way of transferring data between the CPU and peripheral devices. The candidate must correctly state, for two scenarios, whether a scenario describes a polled or interrupt driven approach. Any major disadvantages of the approach should be correctly stated. The scenarios need not be confined to computer systems, as long as the distinction between the two approaches remains clear.

4. Detail the sequence of events when a system performs activities using the system bus. The candidate must correctly trace the sequence of activities on the system buses for at least two different activities, sampled from (i) reading from memory, (ii) writing to memory, (iii) writing to an I/O port, (iv) reading from an I/O port. Such traces must not contain error rates higher than one error per eight steps.

5. Interpret graphical/tabular information from supplied materials.

Assessment for this Outcome must be based on ALL of the five items above. Different assessment events must sample different subsets. Alternative assessment instruments must use different values/scenarios as far as possible.

Outcome 3

The candidate should provide evidence to demonstrate his/her ability to:

1. State the function and operation of all the internal components of the processor including timing and control unit, decoder, instruction register, data buffer, MAR (memory address register), PC (program counter), general purpose register and ALU (arithmetic and logic unit).

2. Detail the activities involved in the fetch/execute cycle. The candidate will be required to provide a trace of the activities of the processor as it performs two different assembly level instructions. One instruction should be adding a value from memory to the accumulator; the second should be an indirect load of a value from memory to a general-purpose register. Evidence will be collected on a supplied pro-forma with spaces to record the values in registers as they change when the cycles of the fetch/execute cycle progress. The candidate must complete this exercise with no higher an error rate than one step in ten.

Assessment for this Outcome must be based on all of the topics detailed above. Alternative assessment instruments must use different values/scenarios.