国外电子信息精品著作(影印版)

可重构片上系统的系统级设计

System Level Design of Reconfigurable Systems-on-Chip

Nikolaos S. Voros
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内 容 简 介

系统级可编程 SOCs 可以解决 SOCs 遇到的一些问题。本书主要针对可编程 SOCs 进行说明，并且对系统在实际中的应用，有很高的指导价值。对于高端设计流程，主要采用了基于 C++语言的 Systemc 以及 OCAPI-XL 等两种方法，对可编程 SOCs 设计有指导意义。

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《国外电子信息精品著作》序

20世纪90年代以来，信息科学技术成为世界经济的中坚力量。随着经济全球化的进一步发展，以微电子、计算机、通信和网络技术为代表的信息技术，成为人类社会进步过程中发展最快、渗透性最强、应用面最广的关键技术。信息技术的发展带动了微电子、计算机、通信、网络、超导等产业的发展，促进了生命科学、新材料、能源、航空航天等高新技术产业的成长。信息产业的发展水平不仅是社会物质生产、文化进步的基本要素和必备条件，也是衡量一个国家的综合国力、国际竞争力和发展水平的重要标志。在中国，信息产业在国民经济发展中占有举足轻重的地位，成为国民经济重要支柱产业。然而，中国的信息科学支持技术发展的力度不够，信息技术还处于比较落后的水平，因此，快速发展信息科学技术成为我国迫在眉睫的大事。

要使我国的信息技术更好地发展起来，需要科学工作者和工程技术人员付出艰辛的努力。此外，我们要从客观上为科学工作者和工程技术人员创造更有利于发展的环境，加强对信息技术的支持与投资力度，其中也包括与信息技术相关的图书出版工作。

从出版的角度考虑，除了较好较快地出版具有自主知识产权的成果外，引进国外的优秀出版物是大有裨益的。洋为中用，将国外的优秀著作引进到国内，促进最新的科技成就迅速转化为我们自己的智力成果，无疑是值得高度重视的。科学出版社引进一批国外知名出版社的优秀著作，使我国从事信息技术的广大科学工作者和工程技术人员能以较低的价格购买，对于推动我国信息技术领域的科研与教学是十分有益的事。

此次科学出版社在广泛征求专家意见的基础上，经过反复论证、仔细遴选，共引进了接近30本外版书，大体上可以分为两类，第一类是基础理论著作，第二类是工程应用方面的著作。所有的著作都涉及信息领域的最新成果，大多数是2005年后出版的，力求“层次高、内

容新、参考性强”。在内容和形式上都体现了科学出版社一贯奉行的严谨作风。

当然，这批书只能涵盖信息科学技术的一部分，所以这项工作还应该继续下去。对于一些读者面较广、观点新颖、国内缺乏的好书还应该翻译成中文出版，这有利于知识更好更快地传播。同时，我也希望广大读者提出好的建议，以改进和完善丛书的出版工作。

总之，我对科学出版社引进外版书这一举措表示热烈的支持，并盼望这一工作取得更大的成绩。

中国科学院院士

中国工程院院士

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Preface

This book presents the perspective of the ADRIATIC project for the design of reconfigurable systems-on-chip, as perceived in the course of the research during 2001 - 2004. The project provided: (a) a high-level hardware/software co-design and co-verification methodology and tools for reconfigurable systems-on-chip, supplemented with back-end design tools for the implementation of the reconfigurable logic blocks of the chip, (b) the definition of the technological requirements for reconfigurable processors for wireless terminals and (c) the implementation of MPEG-4, WCDMA and WLAN design cases to validate the methodology and tools.

Reconfigurability is becoming an important part of System-on-Chip (SoC) design to cope with the increasing demands for simultaneous flexibility and computational power. Current hardware/software co-design methodologies provide little support for dealing with the additional design dimension introduced. Further support at the system-level is needed for the identification and modelling of dynamically re-configurable function blocks, for efficient design space exploration, partitioning and mapping, and for performance evaluation. The overhead effects, e.g. context switching and configuration data, should be included in the modelling already at the system-level in order to produce credible information for decision-making.

This book focuses on hardware/software co-design applied for reconfigurable SoCs. We discuss exploration of additional requirements due to reconfigurability, report extensions to two C++ based languages/methodologies, SystemC and OCAPI-XL, to support those requirements, and present results of three case studies in the wireless and multimedia communication domain that were used for the validation of the approaches.

The book includes nine chapters, divided in three parts: Part A contains Chapters 1 – 3 and provides an introduction to reconfigurable systems-on-chip; Part B contains Chapters 4 – 6 and describes in detail the proposed system level design methodology and the associated tools; Part C, which contains Chapters 7 – 9, provides the details of applying the proposed methodology in practice.

Acknowledgments

The research work that provided the material for this book was carried out during 2001 – 2004 mainly in the ADRIATIC Project (Advanced Methodology for Designing Reconflgurable SoC and Application-Targeted IP-entities in wireless Communications) supported partially by the European Commission under the contract IST-2000-30049. Guidance and comments of Mr Ronan Burgess, Dr Lech Jozwiak and Dr Mark Hellyar on research direction are highly appreciated.

In addition to the authors, the contributions of the following project members and partners' personnel are gratefully acknowledged: Antti Anttonen, Spyros Blionas, Kristof Denolf, Klaus Kronlöf, Tarja Leinonen, Dimitris Metafas, Robert Pasko, Antti Pelkonen, Konstantinos Potamianos, Tapio Rautio, Geert Vanmeerbeeck, Serge Vernalde, Peter Vos, Erik Watzeels, Matti Weisssenfelt and Yan Zhang.

Of them, the editors express their special thanks to Antti Pelkonen and Yan Zhang for their valuable contributions to Chapter 5 and Chapter 9, Robert Pasko and Geert Vanmeerbeeck for their valuable contributions to Chapter 6, Kristof Denolf and Peter Vos for their substantial contributions to Chapter 7 and Serge Vernalde and Erik Watzeels for management related issues.

PART A

RECONFIGURABLE SYSTEMS

Chapter 1

INTRODUCTION TO RECONFIGURABLE HARDWARE

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Abstract: This chapter introduces the reader to main concepts of reconfigurable computing and reconfigurable hardware. Different types of reconfiguration are discussed. A detailed classification of reconfigurable architectures with respect to the granularity of their building blocks, the reconfiguration scheme and the system level coupling is also presented.

Key words: Reconfigurable hardware, reconfigurable architectures, reconfiguration, reconfigurable computing

1. RECONFIGURABLE COMPUTING AND RECONFIGURABLE HARDWARE

Reconfigurable computing refers to systems incorporating some form of hardware programmability–customizing how the hardware is used using a number of physical control points [2]. These control points can then be changed periodically in order to execute different applications using the same hardware. Reconfigurable hardware offers a good balance between implementation efficiency and flexibility as shown in Figure 1-1. This is because reconfigurable hardware combines post-fabrication programmability with the spatial (parallel) computation style [2] of application specific integrated circuits (ASICs), which is more efficient in comparison to the temporal (sequential) computation style of instruction set processors.

Due to the increasing flexibility requirements (e.g. for adaptation to different evolving standards and operating conditions) that are imposed by computationally intensive applications such as wireless communications,

N.S. Voros and K. Masselos (eds.), System Level Design of Reconfigurable Systems-on-Chips, 15-26.

devices need to be highly adaptable to the running applications. On the other hand, efficient realizations of such applications are required, especially in the resources they use during deployment, where power consumption must be traded against perceived quality of the application. The contradictory requirements for flexibility and implementation efficiency cannot be satisfied by conventional instruction set processors and ASICs. Reconfigurable hardware forms an interesting implementation option in such cases.

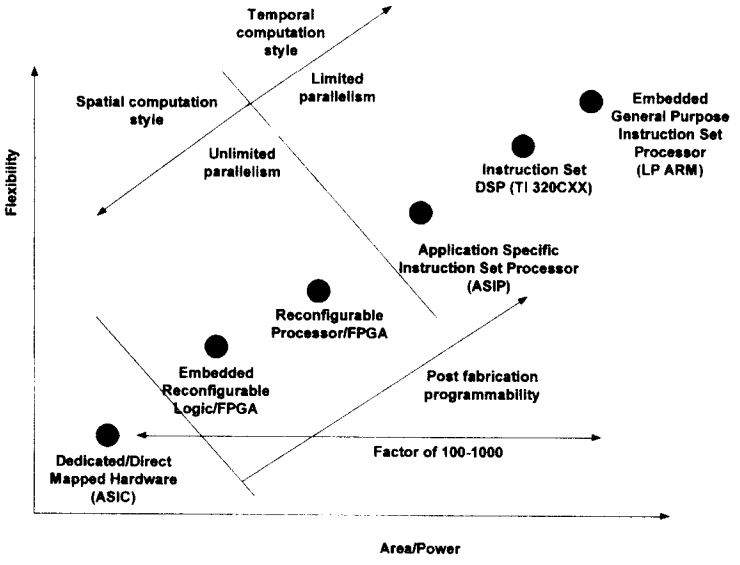

Figure 1-1. Positioning of reconfigurable hardware

There are also other reasons why to use reconfigurable resources in system-on-chip (SoC) design. The increasing non-recurring engineering (NRE) costs push designers to use same SoC in several applications and products for achieving low cost per chip. The presence of reconfigurable resources allows the fine tuning of the chip for different products or product variations. Also, the increasing complexity in the future designs adds the possibility of including design flows, which can require costly and slow redesign of the chip. Reconfigurable elements are often homogenous arrays, which can be pre-verified to minimize the possibility of having design errors. Also the post-manufacturing programmability allows correction or circumvention of problems later than with fixed hardware.