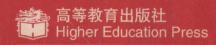
Richard Chi-Hsi Li

KEY ISSUES in RF/RFIC CIRCUIT DESIGN

射频电路和射频集成电路 设计中的关键课题



### 图书在版编目(CIP)数据

射频电路和射频集成电路设计中的关键课题 / KEY ISSUES in RF/RFIC CIRCUIT DESIGN/ Richard Chi-Hsi Li

一北京: 高等教育出版社、2005.2

ISBN 7-04-015958-9

I. 射 ... Ⅱ. R ... III. ①射频电路 - 研究 - 英文

②射频 - 集成电路 - 电路设计 - 研究 - 英文

IV. TN710

中国版本图书馆 CIP 数据核字 (2004) 第 126338 号

北京蓝色畅想图书发行有限公司

策划编辑 张培东 责任编辑 封面设计 刘晓翔 欧阳舟 责任绘图 朱静 版式设计 王尝 责任校对 康晓燕 责任印制 陈伟光

出版发行 高等教育出版社 址 北京市西城区德外大街 4 号 社 邮政编码 100011.

总 机 010-58581000

EIJ 刷 涿州市京南印刷厂

本 787 × 960 1/16 开

张 26 数 490 000 字

经

印

购书热线 010-58581118 免费咨询 800-810-0598

网 址 http://www.hep.edu.cn

http://www.hep.com.cn

网上订购 http://www.landraco.com http://www.landraco.com.cn

次 2005年2月第1次印刷 印

价 40.10 元

次 2005年2月第1版

版

定

本书如有缺页、倒页、脱页等质量问题,请到所购图书销售部门联系调换。

版权所有 侵权必究

物料号: 15958-00

# **Preface**

#### My motivation to write this book

Today, many books about RF (Radio Frequency) circuit design are available for students, researchers, and designers. In these books, the operating principles and circuit topologies are well explained and presented. In addition to offer training of the use of simulation tools, they enable a student who has just graduated from university to start RF circuit designing in his/her new job.

Generally, there are 3 phases of an RF circuit design:

- o Simulation.
- Layout or tape-out.
- And finally, the testing for the prototype module or RFIC (Radio Frequency Integrated Circuit).

Simulation is just the first phase of the design; the heavier jobs would be the second and third phases: layout and testing for a circuitry.

A new RF engineer might be somewhat frustrated from a lack of knowledge that the professors in the university did not teach him/her or he/she did not bother to learn from professors, such as

- The best way to match input and output impedance.
- How to ascertain the criteria for a good layout.
- o How to do RF grounding for a test PCB (Printed Circuit Board).
- o The consequences of tests conducted under an unmatched condition.
- The tolerance to be considered in the design phase.
- The jeopardy of the current RFIC design.
- And so on.

These topics are very important to the 3 design phases mentioned above.

The operating principles and topologies that students learn from university are just the basics of RF circuitry. This knowledge only is not enough to satisfactorily design RF circuits. New RF engineers need engineering knowledge and practical design schemes for a real product design. A book which tries to introduce these objectives might be welcome.

I have been working for a total of 20 years in the Wireless Communication System for Motorola from 1979 to 1984, and then from 1987 to 2001. My job has covered a wide range, from acoustics to RF, and from software to hardware. However, most of those years were spent on the RF and RFIC design. I have been invited to lecture about the above topics in universities and companies since 1991; my lectures seem

to be quite positive and very often I was encouraged to publish my presentation material by my audiences and professors. This is my motivation to write this book.

In this book I try to summarize my engineering experiences—both successes and failures—and some special design schemes in the RF module and RFIC design.

#### Special features of this book

The topics most published in RF books are about the main RF blocks such as the LNA, Mixer, PA, VCO, and Synthesizer... The configuration of those books could be categorized as "longitudinal."

Instead of individual RF blocks' description and discussion, the general features and the key issues of the RF circuit design will be emphasized in this book, such as impedance matching, RF grounding, the basic RF parameters, from single end to differential, jeopardy in RFIC design... Therefore, the configuration of this book could be categorized as "transversal." This is one of the special features of this book.

Another special feature of this book is that the original data in many sections is based on my design reports. This might also introduce my own imperfect understanding or prejudices: I will highly appreciate any comment from readers. On the other hand, there are not too many references that I listed: readers might easily go to the Internet for hundreds and thousands of articles, papers, and books about RF circuit design.

#### Outline of this book

### Chapter 1: Importance of impedance matching

- A digital circuit is designed for the transportation and manipulation of a digital signal's "status", "0" or "1", while an RF circuit is designed for the transportation and manipulation of an RF signal's "power." In the digital circuit design for low data rates, the main objective of concern is the speed of the circuit response while in the RF circuit design the main objective of concern is impedance matching. However, when the data rate is enhanced to or over the RF frequency range, the difference between the two design philosophies disappears. Thus, impedance matching becomes the principally concerned objective of both digital and RF circuit designs.
- O Unmatched impedance results in power loss, additional distortion, additional noise, incorrect readings in power measurement, failure to obtain enough voltage swing, and at the extreme end, damage to transistors or parts.

O Very often in many books or papers, impedance matching is described as the means for maximum power transportation or transformation. This is an incomplete explanation. Another purpose of impedance matching for an RF circuit is to approach a zero phase-shift of voltage or current when power is transported from the source to the load.

#### Chapter 2: Impedance matching

- O Before working for the impedance matching, one must understand how to measure a DUT's impedance first. In laboratory, the impedance of a DUT is usually measured by an impedance meter or network analyzer. The measurement is conducted by means of a small signal. Therefore, it is effective only for situations where the DUT is operated with a small signal. Should the DUT be operated with a large signal, the impedance of DUT must be measured with the assistance of a circulator, a vector voltmeter or a directional coupler.
- Most matching networks are implemented with passive parts: capacitors and inductors. The original impedance is changed step by step as each part is added to the matching network one by one, and eventually the final desired impedance is reached. By means of the assistance of the Smith Chart, the values of these parts can be easily found.
- O The Smith Chart is a powerful tool in the impedance matching technology. It can be divided to 4 regions; the topology of a matching network is directly related to the region where the original impedance is located. A matching network implemented with one, two, and three parts is discussed in somewhat detailed in this chapter. Additionally, two special types of 3 parts matching network, the T and Π types, are compared, showing their advantages and disadvantages.
- O Also, some useful schemes for impedance matching work are introduced.

# Chapter 3: RF grounding

- RF grounding is one of the most important topics of RF circuit designs. An imperfect RF grounding significantly degrades performance of RF blocks or systems.
- The usual way to ground a point on a circuit board is to connect this point to another well-grounded point by a metallic runner or a piece of metal sheet with a high conductivity, such as a copper runner with gold-plating on a PCB or a gold runner on the integrated circuit. This is a unanimous means of grounding

when the circuit is operating in the low frequency range because the metallic runner is equipotential. However, it might be unfeasible when the circuit is operating in the RF range: essentially, a metallic runner with a high conductivity either on the IC substrate or on the PCB in the RF range is a micro strip line. Therefore, it is not an equipotantial connector unless its length is much less than a quarter wavelength or equal to the mutiple of half wavelength.

- o In the RF frequency range, RF grounding could be well done by means of a "zero" capacitor, a micro-strip line and an RF cable of an appropriate length.
- A capacitor has a character of self-resonance in series. At SRF (Self-Resonant Frequency) the chip capacitor is called a "zero" capacitor because its impedance approaches zero. It becomes a good by-pass part when the operating frequency is equal to its SRF. Therefore, a "zero" capacitor is sometimes called by-pass capacitor. In RF testing laboratories, the chip capacitor is chosen as a "zero" or by-pass capacitor in most cases, because its SRF is mostly located in an RF frequency range and, on the other hand, its assets include small size, cheapness, and a reliable performance.
- A good RF grounding is crucial to a test PCB design for either RF module or RFIC die. It must be noted that the technique of designing a test PCB is quite different when its size is changed from small to large. This will be discussed more detailed in this chapter.
- o Finally, some special technical schemes related to RF grounding are introduced, such as compulsory RF grounding by a quarter-wavelength micro strip line, the calibration for network analyzer, and the special consideration of RF grounding to avoid or reduce the return current coupling.

# Chapter 4: Equivalent circuits of passive chip parts

- O Besides the active parts, such as transistors and diodes, the passive chip parts are basic components in the implementation of an RF module today. On the other hand, the "zero" capacitor is usually chosen among chip capacitors, which are indispensable parts for a test PCB with a good RF grounding. It does not matter that the test PCB is for testing of RF modules or RFIC dies. In other words, the study of chip parts' characteristics is important to not only for RF modules but also for RFIC designers.
- O Primarily, for RF grounding purposes, our preferences in the study of passive chip parts is how to characterize a chip capacitor and how to chose a "zero" capacitor among all the chip capacitors. The features of two other chip parts, the chip inductor and chip resistor, are also important topics to be understood in RF circuit design. Instead of self-resonance in series, a chip inductor at its SRF

frequency is in self resonance in parallel. The impedance of a chip inductor at its SRF frequency approaches infinity ideally and is therefore called an "infinitive" inductor. Sometimes it is also called an RF "choke." In the RF frequency range, the resistance of a chip resistor is quite sensitive to the operating frequency. At RF frequencies, the actual value of its resistance could be 10 times more or less than the manufacturer's specified value at low frequencies. The other features of chip resistor are also presented.

#### Chapter 5: From single-ended to differential

- o In recent years, the topology of RF circuits have shifted from single-ended stages to differential pairs. This is due to the configurational change of a communication system from a dual conversion to a direct conversion system since 1980's.
- A communication system with direct conversion brings about a lot of advantage in the reduction of material cost: many expensive filters are unnecessary. However, it also brings about technical jeopardy and DC offset problem if the topologies of RF circuits remained as single-ended stages.
- The need of differential configuration is due to its advantage of low DC offset output current and high CMRR (Common Mode Rejection Ratio). Theoretically, the DC offset due to the non-linearity of transistors in an ideal differential pair is zero and the CMRR is infinitive, though such an ideal differential pair does not exist in reality.
- It should be noted that there are two DC offset sources. One is due to the non-linearity of transistors and the asymmetry of the layout in the differential pair itself; another source is due to interference from outside the differential pair. Therefore, DC offset still exists in the entire communication system even though the DC offset due to the non-linearity of transistors can be reduced by the differential pair. An effort to reduce or eliminate DC offset is necessary though the circuit configuration has been shifted from single-ended stages to differential pairs. In the up-to-date direct conversion communication systems, there are three technologies to reduce DC offset. They are: DC offset reduction by "chopping", DC offset elimination by calibration, and DC offset cancellation by hardware.

### Chapter 6: Baluns

O Baluns are used in the transformation between differential pairs and singleended stages. A variety of baluns have been developed in the past decades; only

- some of them are introduced. They are the coaxial cable balun, the ring micro strip line balun, the transformer balun, and the LC balun.
- o LC baluns are discussed rather meticulously here: in contrast with other baluns, it has favorable assets of a small size, low cost, and easy implementation.

#### Chapter 7: Tolerance analysis

- Tolerance analysis is extremely important in both RF and digital circuit designs for a massive production line. Any circuit design without tolerance analysis might result in a very poor yield rate of the products, and thus the bankruptcy of a company.
- O The most advanced tolerance control, the so-called " $6\sigma$ " program, is the design goal for every design engineer, by which the yield rate in a massive production line is 99.74%, a little bit less than 100%.
- O Design goals sometimes depend on the tolerance analysis. If so, tolerance analysis must be conducted before or at the same time as circuit design.
- O As an example, tolerance analysis of a tunable filter design is presented.

# Chapter 8: Prospect of RFIC design

- The possibility of the implementation of an RFIC mainly depends on the isolation between RF blocks, which moved forward a great step since 1990's. Guard rings, grounding separations and DC power supply separations are the key segments to isolation improvement between RF blocks. In order to realize the SOC (System On Chip) goal, the study of isolation must be continued, including isolation between digital blocks and the isolation between RF and digital blocks.
- Layouts for runners, vias, pads, bonding wires and so on directly impact an RFIC design's performance. A designer must be familiar with these items with a specific processing and try to achieve best performance by controlling their size, shape, and the distance from adjacent parts.
- o In order to reduce the number of tape-outs for an RFIC design, the parts should be as variable as possible. This not only reduces cost but also saves time.
- O The main barrier in the developing of RFIC is the poor performance of a spiral IC inductor: the Q value of a spiral IC inductor is too low. Since the 1980's, many scientists and engineers have put a lot of effort on the implementation of

an inductor with a high Q value on the RFIC chip. Unfortunately, progress is quite limited. The most prospective technology to build a high-Q IC inductor might be the use of negative-resistance compensation technology.

#### Chapter 9: Noise, gain, and sensitivity of a receiver

- O The main RF parameters include the noise figure, gain, and non-linearity.
- O There are different noises induced form both active and passive parts. Shot noise in parts is directly related to the current flowing through it. In the micro world, the current is fluctuated around its average value at any instant. The fluctuation is a random, stochastic process and represents a kind of noise called "shot" noise. Thermal noise is essentially the fluctuation of the resistance in the parts or devices and is directly related to the temperature. Besides these two types of noise, a variety of other noises existed in parts, such as flicker noise, popcorn noise and so on.
- The additional noise of a circuit block can be described by its noise figure, which is defined as a ratio of the input SNR (Ratio of Signal to Noise) to the output SNR. The noise figure of a circuit block is related to the source impedance. It can be proved that there is an optimum value of the source impedance for a two port block, by which the noise figure of a two port block reaches a minimum.
- The noise figure of a system is contributed by the noise figures from all the individual blocks. However, the noise figure of 1<sup>st</sup> block is the main contributor to the system noise figure if its power gain is greater than 1. If the 1<sup>st</sup> block is an LNA (Low Noise Amplifier), then to design an LNA with low noise figure and high power gain is the top priority to the sensitivity of an analog communication system, since the sensitivity mainly depends on the system noise figure. The system noise figure can be calculated by cascading all of the noises from all of the blocks.

# Chapter 10: Non-linearity and spurious products

The spurious products in a block or system come from a non-linearity of active devices. It is well known that the non-linearity of active devices consists of numerous non-linear elements with different orders. Consequently, the spurious products in a block or a system are rather complicated. Generally, the remarkable spurious products, of course, result from the 2<sup>nd</sup> and 3<sup>rd</sup> orders of non-linearity because the non-linearity coefficients of 2<sup>nd</sup> and 3<sup>rd</sup> order non-linearity are usually dominant over or much greater than that of other orders' non-linearity.

- O IP (Intercept Point) is an intermediate concept. In terms of intercept points, the IMR (InterModulation Rejection) can be obtained through some simple calculations. The  $2^{nd}$  and  $3^{rd}$  orders of the intercept points,  $IP_2$  and  $IP_3$ , will be discussed thoroughly since they represent the main terms of non-linearity. The value  $IP_3$  is widely applied in the measurement of the non-linearity of a block or system.
- O However, the measurement of  $IP_3$  in the laboratory is somewhat complicated. Very often, people replace the specification of  $IP_3$  with a 1 dB compression point. As a matter of fact, both of them can characterize the non-linearity of a block or a system, but a 1 dB compression point seems to be more intuitive.
- Finally, it should be noted that all spurious products appear as the distortion of signals in a block or a system: unlike noise, they can be categorized as interference.

#### Chapter 11: Cascaded equations and system analysis

In order to carry out system analysis, the cascaded equations for the power gains, noise figures and intercept points are derived and an example of system analysis is demonstrated in this chapter.

## Chapter 12: From analog to digital communication system

- An RF circuit designer must understand the digital circuit portion of a system so that he/she can achieve better designing on the RF circuit portion and cooperate better with the digital circuit designer. This is the purpose of this chapter.
- There are two main differences between analog and digital communication systems: A/D-D/A conversion and encoding/decoding. There are no A/D-D/A or encoding/decoding blocks in an analog communication system. In the transmitter of an analog communication system, the signal, such as the video or voice, directly modulates the RF carrier using its special modulation mode, such as AM, FM, and PM. In the receiver of an analog communication system, the modulated RF carrier is demodulated with a corresponding modulation mode, and the signal is recovered. In the transmitter of a digital communication system, there are 3 procedures to be done. First, the signal must be digitalized, in which a signal waveform is converted into a digital sequence via A/D conversion. Next, the digital sequence is taken to an encoder for channel arrangement and partially for error correction. Lastly, the encoded digital signal modulates RF carrier with various modulation schemes, such as FSK, BPSK, QPSK, MSK, and so on. In the receiver of a digital communication system, the first task is to demodulate the RF carrier with a corresponding modulation mode.

Next, the demodulated digital sequence is taken to the decoder for channel arrangement and error correction. Lastly, the decoded digital sequence is converted into an analog waveform so that the signal, such as video or voice, is recovered.

 Bit error rate, instead of sensitivity, is the main concern of a digital communication system. Some basic encoding and decoding technologies and error correction schemes are outlined in this chapter.

#### Readers of this book

- o RF and RFIC designers
- O Students, teachers and Professors for their RF/RFIC design course in universities.

# **Acknowledgements**

With my heart and soul I am always very thankful to my mother-schools who cultivated me from primary- to high- education, and to the company which I have been working for 20 years. They are

- O QiaoGuang middle school, NanAn, Fujian, China;
- O YongChun First high school, YongChun, Fujian, China;
- o FuDan University, Shanghai, China;
- o Pennsylvania State University, State College, Pennsylvania, USA.
- Communication division, Motorola, Fort Lauderdale/Phoenix/Fort Worth, USA.

Thanks to Professor Zhi-Gong Wang in SEU (SouthEast University), Nanjing, China, who encouraged and recommended this book to the publisher. Professor Wang examined all the contents of this book. Also, thanks to Mr. Pei-Dong Zhang, Ms. Zhou Ouyang, and the team in Higher Education Press, Beijing, China, who have been working hard for all the publication affairs. Finally, my deepest appreciation to my lovely son, Bruno Sie Li, who is just 12 years old but checked and corrected my English writing for this book.

Richard Chi-Hsi Li September, 2004

# **About Author**

**Richard Chi-Hsi Li,** male, was born in NanAn, QuanZhou, Fujian, China. He graduated in the Physics Department of FuDan University, Shanghai, China in 1958. From 1958 to 1973, he had been working for the Institute of Geophysics, Chinese academy, and the University of China Science and Technology, Beijing, China.

From 1977 to 1980, he studied in the Electrical Engineering Department of Pennsylvania State University in Pennsylvania, USA for the PhD degree. He had been working totally 20 years in the Wireless Communication System for Motorola from 1979 to 1984, and from 1987 to 2001. From 1985 to 1987 he had been working for Texas Instruments, Dallas, Texas, and for RCA in Princeton, New Jersey, for the Communication Satellite Design.

His job covers a wide range, from acoustic to RF, and from software to hardware. Most of years in Motorola he spent on the RF and RFIC design in RFTC (RF Technology Center) and WITC (Wireless Integrated Technology Center). Richard has pioneered the development of innovative RF/RFIC circuits including: Tunable filter, LNA, PA, Mixer, VCO, and the RFIC for portable radio or cellular radio front end. He developed on-chip 1 watt to 2 watts power amplifier by CMOS, the outstanding tunable filter, the dual-line and toroidal balun. Not only in the RF and RFIC design, Richard had been working for the acoustic, digital software design for years also.

From 1985 to 1986, Richard was the technical leader of the DBS (Direct Broadcast Satellite) team with 25 engineers working for the DBS system in Texas Instruments, Dallas, Texas. From 1986 to 1987 working for RCA, he had been involving in 4 Communication Satellite designs.

Richard had been invited as a technical consultant in CCL, ITRI, in Taiwan from 1991 to 2000. Richard holds 3 US patents. He wrote tens of high technology internal reports. Also, he is the co-author of the book titled "The Upper Atmosphere", published in Beijing, 1963.

# **Contents**

Chapter 1 Importance of Impedance Matching					
1.1	Difference between RF and Digital Circuit Design				
•	1.1.1	Case 1: Digital Circuits at Low Data Rate			
	1.1.2	Case 2: Digital Circuits at High Data Rate	(		
1.2	Sign	Significance of Impedance Matching			
	1.2.1	Power Transportation from a Source to a Load			
	1.2.2	Maximizing of Power Transportation without Phase Shift			
	1.2.3				
	1.2.4	Impedance Matching Network			
1.3	Problems due to Unmatched Status of Impedance				
	1.3.1	General Expression of Power Transportation	16		
	1.3.2	Power Instability and Additional Power Loss	18		
	1.3.3	Additional Distortion and Quasi-Noise			
	1.3.4				
	1.3.5	Power Transportation and Voltage Transportation	26		
	1.3.6	Burning of a Transistor	30		
Ref	erences	3	31		
Chapter	2 Im	pedance Matching	32		
2.1	Impedance Measured by Small Signal				
	2.1.1	Impedance Measured by S Parameter Measurement	32		
	2.1.2	Smith Chart: Impedance and Admittance Coordination	34		
	2.1.3	Accuracy of Smith Chart			
	2.1.4	Relationship between the Impedance in Series and in Parallel	39		
2.2	Impe	dance Measured by Large Signal	······ <b>4</b> 0		
2.3	Impe	Impedance Matching4			
	2.3.1	One Part Matching Network	44		
	2.3.2	Recognition of Regions in a Smith Chart	·····45		
	2.3.3	Two Parts Matching Network			
	2.3.4	Two Parts Upward and Downward Impedance Transformer	58		
	2.3.5	Three Parts Matching Network and Impedance Transformer	62		
		2.3.5.1 Topology Limitation of Two Parts Matching Network	62		
		2.3.5.2 II Type Matching Network	64		
		2.3.5.3 T Type Matching Network ·····	71		
2.4	Some	Useful Schemes for Impedance Matching	····· 76		

		2.4.1 Designs and T	ests when $Z_L$ is not 50 $\Omega$	.76			
		2.4.2 Conversion be	tween T and Π Type Matching Network······	-77			
			hing Network				
		2.4.4 Impedance Ma	tching between Power Transportation Units	.80			
			tching for a Mixer				
1	Refer	ences ·····		·83			
Chapt	ter 3	RF Grounding	g	·85			
3	.1	A True Story		85			
3	.2	Three Component	s for RF Grounding	87			
		3.2.1 "Zero" Capacit	ors	-88			
		3.2.2 Micro Strip Lit	ıe	92			
		3.2.3 RF Cables ······		98			
3	.3	Evamples of RE C	rounding1	۸۸			
3		3.3.1 Test PCB	]	.00			
			Test PCB ······				
		3.3.1					
		3.3.1	1.2 RF Grounding with a Rectangular Metallic				
			Frame·····l				
		3.3.1		07			
		_	: Test PCB1				
		3.3.1		12			
		3.3.1.		10			
		2.2 7 1.4 1.4	Quarter Wavelength1				
		.3.2 Isolation betwe	en Input and Output in a Mixer or an Up-converter ········· 1 Network Analyzer ······ 1	17			
3.	.4	RF Grounding for Reduction of Return Current Coupling					
		.4.1 A Circuit Built	by Discrete Parts on a PCB1	19			
		.4.2 RFICs		21			
R	efer	nces·····	1	27			
			the CD of CD of CD				
Chapte			cuits of Passive Chip Parts1				
4.	1	Aodeling of Passiv	e Chip Parts1	29			
4.	2	Characterization o	f a Chip Part by Network Analyzer	30			
4.	3	extraction from th	e Measurement by Network Analyzer1	32			
		.3.1 Extraction for C	hip Capacitors 1	33			
		3.2 Extraction for C	hip Inductors 1	38			
			hip Resistors 1				
4.	4	ummary	1	<b>4</b> 5			
-			1	47			

6.5	LC Balun220						
References 2							
Chapter	7 Tolerance Analysis	232					
7.1	Importance of Tolerance Analysis						
7.2	Fundamentals of Tolerance Analysis						
1.2	7.2.1 Tolerance and Normal Distribution	234					
	7.2.2 $6\sigma$ , $C_p$ , and $C_{pk}$	238					
	7.2.3 Yield Rate and DPU	243					
	7.2.4 Poisson Distribution						
7.3	An Approach to 6σ Design and Production	247					
7.4	An Example: A Tunable Filter Design						
	7.4.1 Description of the Tunable Filter Design	253					
	7.4.2 Monte-Carlo Analysis	255					
7.5	Appendix: Table of the Normal Distribution	261					
	erences						
Reie	rences	200					
Chapter	8 Prospect of RFIC Design	264					
8.1	History of RFIC Development	264					
8.2	Isolation between Blocks in an RFIC						
	8.2.1 Definition and Measurement of Isolation	268					
	8.2.2 Isolation Technology						
8.3	Low Q Value of Spiral Inductor	283					
	8.3.1 Skin Effect	·············· 285					
	8.3.2 Attenuation due to Substrate ·····	287					
	8.3.3 Flux Leakage ····	287					
	8.3.4 Flux Cancellation						
	8.3.5 A Possible Solution—Negative Resistance Compensation	292					
	8.3.5.1 Negative Resistance Generator with a FET	293					
	8.3.5.2 Negative Resistance Generator with Transformer						
8.4	Layout ·····	295					
	8.4.1 Runners····	295					
	8.4.2 Parts	302					
	8.4.3 Variable Parts in RFIC	304					
	8.4.4 Symmetry	305					
		30b					
8.5	Two Challenges in an RFIC or SOC Design	308					
	8.5.1 Isolation						