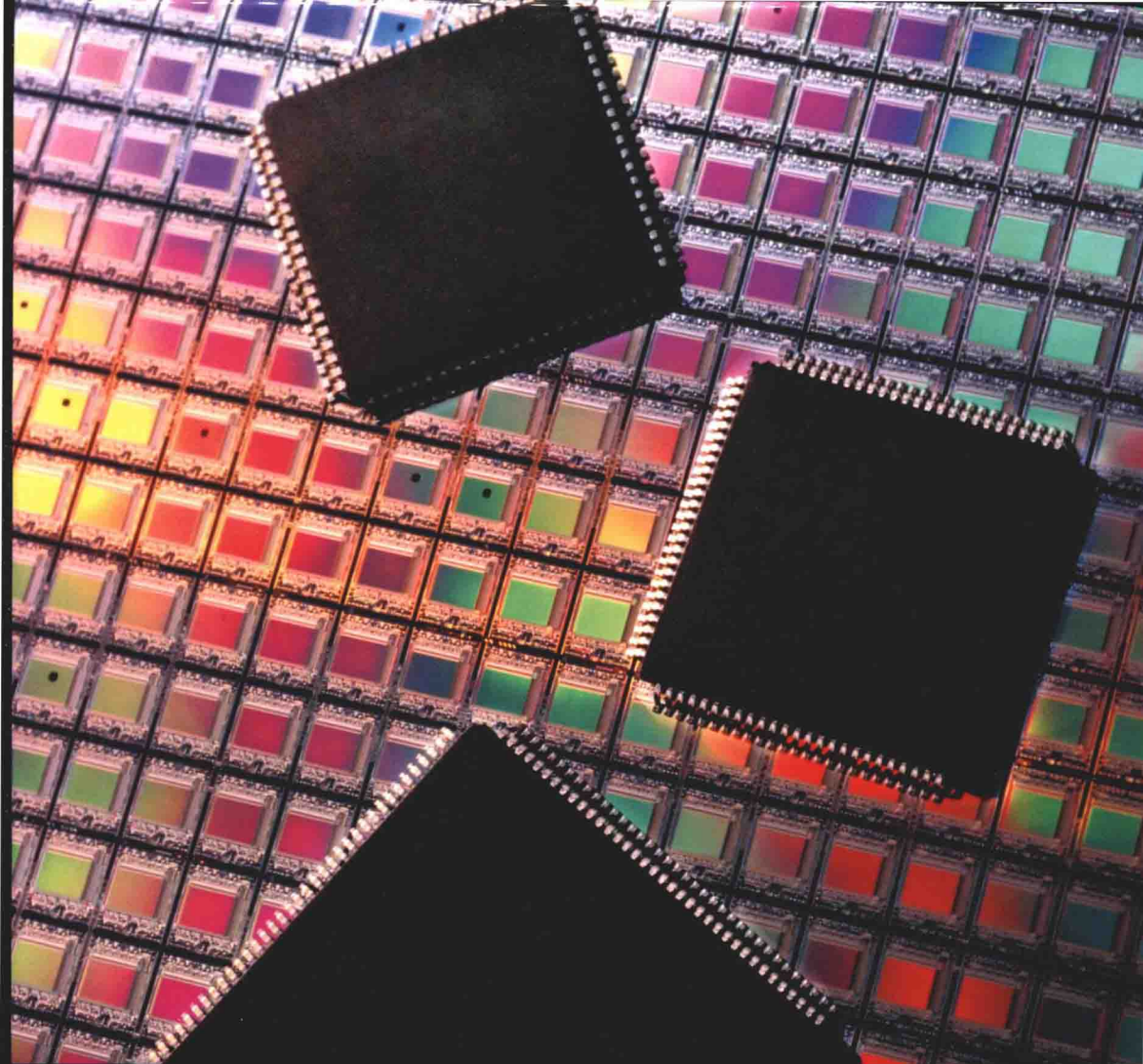

Through Silicon Vias

Materials, Models, Design, and Performance

Brajesh Kumar Kaushik • Vobulapuram Ramesh Kumar
Manoj Kumar Majumder • Arsalan Alam

CRC Press
Taylor & Francis Group

Through Silicon Vias

Materials, Models, Design, and Performance

Brajesh Kumar Kaushik • Vobulapuram Ramesh Kumar
Manoj Kumar Majumder • Arsalan Alam

CRC Press
Taylor & Francis Group
Boca Raton London New York

CRC Press is an imprint of the
Taylor & Francis Group, an **Informa** business

CRC Press
Taylor & Francis Group
6000 Broken Sound Parkway NW, Suite 300
Boca Raton, FL 33487-2742

Printed on acid-free paper
Version Date: 20160624

International Standard Book Number-13: 978-1-4987-4552-9 (Hardback)

Visit the Taylor & Francis Web site at
http://www.taylorandfrancis.com

and the CRC Press Web site at
http://www.crcpress.com

Through Silicon Vias

Materials, Models, Design, and Performance

Preface

The conventional two-dimensional integrated circuit (2D IC) packaging technique has almost reached its maximum profitable limit and is no longer useful for future IC integration. With the advancement in technology, the density of dies keeps increasing, and, therefore, the number of input/output (I/O) pins increases exponentially according to Rent's rule, and the interconnect length also increases to communicate between the dies. Therefore, due to the limited number of I/O pins and longer interconnects between dies, 2D IC integration offers lower bandwidth and thus degrades system performance. Recent advances in semiconductor technology offer vertical interconnect access (via) that extends through silicon, known as through silicon via (TSV). Compared to the conventional wire bond, TSVs offer higher bandwidth and density with low latency, and power dissipation, thereby enabling higher integration density and superior system performance. The use of TSVs is the only way to overcome the difficulties of 2D packaging issues while extending the momentum of Moore's law for future very-large-scale integration (VLSI) technology by using the advanced packaging chips named as three-dimensional (3D) chips.

Development of a reliable 3D integrated system is largely dependent on the choice of filler materials used in TSVs. Although several researchers demonstrated that copper (Cu) is a suitable filler material, but recently graphene-based nano-interconnects have rapidly gained interest to replace Cu. Graphene-based nano-interconnects can exhibit unique electrical, thermal, mechanical, and chemical properties. The sp^2 bonding in graphene is stronger than the sp^3 bonding in diamonds. The higher current-carrying capability, long ballistic transport length, higher thermal conductivity, and mechanical strength are responsible for their exciting prospects in the area of advanced packaging techniques.

This book provides a comprehensive review of theory behind TSVs, covering the most recent advancements in materials, models, and design. Furthermore, depending on the geometry and physical configurations, different electrical equivalent models for Cu-, carbon nanotube (CNT)-, and graphene nanoribbon (GNR)-based TSVs are presented. Based on the electrical equivalent models, the performance comparison among the Cu-, CNT-, and GNR-based TSVs is also discussed. The organization of the book is as follows: Chapter 1 introduces the current research scenario in 3D technology and packaging techniques. Chapter 2 discusses the structure, properties, fabrication techniques, and different filler materials of TSVs. Chapter 3 presents the scalable electrical equivalent model of Cu-based TSVs. Additionally, a novel approach is discussed to extract the parasitic parameters of Cu-based TSVs. Chapter 4 provides a brief review of CNTs and the performance

comparison of Cu- and CNT-based TSVs. Chapters 5 and 6 discuss the mixed CNT bundled TSVs and GNR-based TSVs, respectively, along with the performance comparison of Cu- and CNT-based TSVs. Chapter 7 is dedicated to TSV liner materials and their impact on performance. Finally, Chapter 8 introduces the modeling of TSVs using the finite-difference time-domain technique.

Brajesh Kumar Kaushik
Vobulapuram Ramesh Kumar
Manoj Kumar Majumder
Arsalan Alam

Authors

Brajesh Kumar Kaushik received his BE degree in Electronics and Communication Engineering from the Deenbandhu Chhotu Ram University of Science and Technology (formerly *Chhotu Ram State College of Engineering*), Murthal, Haryana, in 1994; his M.Tech degree in Engineering Systems from Dayalbagh Educational Institute, Agra, Uttar Pradesh, in 1997; and his PhD degree under the All India Council for Technical Education-Quality Improvement Programme (AICTE-QIP) scheme from the Indian Institute of Technology Roorkee, Roorkee, Uttarakhand, India, in 2007. He served at Vinytics Peripherals Pvt. Ltd., Delhi, from 1997 to 1998 as the Research and Development Engineer for microprocessor-, microcontroller-, and DSP processor-based systems.

Dr. Kaushik joined the Department of Electronics and Communication Engineering, Govind Ballabh Pant Engineering College, Pauri Garhwal, Uttarakhand, India, as a Lecturer in July 1998, where he also served as an Assistant Professor from May 2005 to May 2006 and as an Associate Professor from May 2006 to December 2009. He is currently serving as an Associate Professor in the Department of Electronics and Communication Engineering, Indian Institute of Technology Roorkee. His research interests include high-speed interconnects, low-power very-large-scale integration (VLSI) design, CNT-based designs, organic thin-film transistor design and modeling, and spintronics-based devices and circuits. He has published extensively in several national and international journals and conferences of repute. Dr. Kaushik is a reviewer of many international journals belonging to various publication houses such the Institute of Electrical and Electronics Engineers (IEEE), the Institution of Engineering and Technology (IET), Elsevier, Springer, Emerald, and Taylor & Francis. He has delivered many keynote addresses in reputed international and national conferences. He holds the position of Editor and Editor-in-Chief of various journals in the field of VLSI and Microelectronics. He is a senior member of IEEE and has received many awards and recognitions from the International Biographical Center, Cambridge, England. His name has been listed in *Marquis Who's Who in Science and Engineering®* (10th Anniversary, 2008–2009 Edition) and *Marquis Who's Who in the World®* (26th Edition, 2009).

Vobulapuram Ramesh Kumar received his B.Tech in Electronics and Communication Engineering from Acharya Nagarjuna University, Guntur, Andhra Pradesh, in 2007, M.Tech degree in VLSI design from the National Institute of Technology, Hamirpur, Himachal Pradesh, India, in 2010, and PhD degree from the Indian Institute of Technology Roorkee, Roorkee, Uttarakhand, India, in 2015. He has authored/coauthored over 20 publications in reputed journals and conferences. He has coauthored a book titled *Crosstalk in Modern On-Chip Interconnects-A FDTD Approach* (Singapore, Springer, 2016).

Dr. Kumar worked as an Assistant Professor in the Department of Electronics and Communication Engineering at Gandhi Institute of Technology and Management (GITAM) University, Hyderabad Campus, Andhra Pradesh, from June 2010 to December 2011. He is currently working as an Associate Professor in the Department of Electronics and Communication Engineering at KL University (officially the Koneru Lakshmaiah Education Foundation), Guntur, Andhra Pradesh, India. His current research interests include time-domain numerical methods to approach fast transients characterization techniques, modeling of VLSI on-chip interconnects, graphene-based nano-interconnects, and through silicon vias.

Manoj Kumar Majumder received his B.Tech and M.Tech degrees from West Bengal University of Technology, Bidhan Nagar, West Bengal, India, and Indian Institute of Engineering Science and Technology (IIEST), Shibpur, West Bengal, India, in 2007 and 2009, respectively. He was awarded his PhD degree from the Department of Electronics and Communication Engineering, Indian Institute of Technology Roorkee, Roorkee, Uttarakhand, India, in 2015. He was a Lecturer in the Durgapur Institute of Advanced Technology and Management, Durgapur, West Bengal, India, from July 2009 to July 2010. He is currently associated with the academic activities in Electronics and Communication Engineering Department, Techno India University, Kolkata, West Bengal, India.

He has authored over 20 papers in peer-reviewed international journals and over 30 papers in international conferences. He has coauthored a book titled *Carbon Nanotube Based VLSI Interconnects: Analysis and Design* (New York: Springer, 2014) and also a book chapter entitled "Fabrication and modelling of copper and carbon nanotube based through-silicon via" in *Design of 3D Integrated Circuits and Systems* (Boca Raton, FL: CRC Press,

2014). His current research interests include the area of carbon nanotube and graphene nanoribbon-based VLSI interconnects and vias. His name has been listed in *Marquis Who's Who in the World* (33rd Edition, 2016).

Arsalan Alam received his B.Tech degree from Zakir Hussain College of Engineering and Technology, Aligarh Muslim University, Aligarh, Uttar Pradesh, India, in 2011 and his M.Tech degree in Microelectronics and VLSI from Indian Institute of Technology Roorkee, Roorkee, Uttarakhand, India, 2015. He is currently working as a Research Associate in King Abdullah University of Science & Technology, Thuwal, Saudi Arabia. His research areas are time-domain numerical methods for analyzing the performance of VLSI on-chip interconnects and modeling of through silicon vias.

Contents