



Through Silicon Vias

Materials, Models, Design, and Performance

Brajesh Kumar Kaushik • Vobulapuram Ramesh Kumar
Manoj Kumar Majumder • Arsalan Alam



CRC Press
Taylor & Francis Group

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Boca Raton London New York

CRC Press is an imprint of the
Taylor & Francis Group, an **Informa** business

CRC Press
Taylor & Francis Group
6000 Broken Sound Parkway NW, Suite 300
Boca Raton, FL 33487-2742

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CRC Press is an imprint of Taylor & Francis Group, an Informa business

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Printed on acid-free paper
Version Date: 20160624

International Standard Book Number-13: 978-1-4987-4552-9 (Hardback)

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Preface

The conventional two-dimensional integrated circuit (2D IC) packaging technique has almost reached its maximum profitable limit and is no longer useful for future IC integration. With the advancement in technology, the density of dies keeps increasing, and, therefore, the number of input/output (I/O) pins increases exponentially according to Rent's rule, and the interconnect length also increases to communicate between the dies. Therefore, due to the limited number of I/O pins and longer interconnects between dies, 2D IC integration offers lower bandwidth and thus degrades system performance. Recent advances in semiconductor technology offer vertical interconnect access (via) that extends through silicon, known as through silicon via (TSV). Compared to the conventional wire bond, TSVs offer higher bandwidth and density with low latency, and power dissipation, thereby enabling higher integration density and superior system performance. The use of TSVs is the only way to overcome the difficulties of 2D packaging issues while extending the momentum of Moore's law for future very-large-scale integration (VLSI) technology by using the advanced packaging chips named as three-dimensional (3D) chips.

Development of a reliable 3D integrated system is largely dependent on the choice of filler materials used in TSVs. Although several researchers demonstrated that copper (Cu) is a suitable filler material, but recently graphene-based nano-interconnects have rapidly gained interest to replace Cu. Graphene-based nano-interconnects can exhibit unique electrical, thermal, mechanical, and chemical properties. The sp^2 bonding in graphene is stronger than the sp^3 bonding in diamonds. The higher current-carrying capability, long ballistic transport length, higher thermal conductivity, and mechanical strength are responsible for their exciting prospects in the area of advanced packaging techniques.

This book provides a comprehensive review of theory behind TSVs, covering the most recent advancements in materials, models, and design. Furthermore, depending on the geometry and physical configurations, different electrical equivalent models for Cu-, carbon nanotube (CNT)-, and graphene nanoribbon (GNR)-based TSVs are presented. Based on the electrical equivalent models, the performance comparison among the Cu-, CNT-, and GNR-based TSVs is also discussed. The organization of the book is as follows: Chapter 1 introduces the current research scenario in 3D technology and packaging techniques. Chapter 2 discusses the structure, properties, fabrication techniques, and different filler materials of TSVs. Chapter 3 presents the scalable electrical equivalent model of Cu-based TSVs. Additionally, a novel approach is discussed to extract the parasitic parameters of Cu-based TSVs. Chapter 4 provides a brief review of CNTs and the performance

comparison of Cu- and CNT-based TSVs. Chapters 5 and 6 discuss the mixed CNT bundled TSVs and GNR-based TSVs, respectively, along with the performance comparison of Cu- and CNT-based TSVs. Chapter 7 is dedicated to TSV liner materials and their impact on performance. Finally, Chapter 8 introduces the modeling of TSVs using the finite-difference time-domain technique.

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Dr. Kaushik joined the Department of Electronics and Communication Engineering, Govind Ballabh Pant Engineering College, Pauri Garhwal, Uttarakhand, India, as a Lecturer in July 1998, where he also served as an Assistant Professor from May 2005 to May 2006 and as an Associate Professor from May 2006 to December 2009. He is currently serving as an Associate Professor in the Department of Electronics and Communication Engineering, Indian Institute of Technology Roorkee. His research interests include high-speed interconnects, low-power very-large-scale integration (VLSI) design, CNT-based designs, organic thin-film transistor design and modeling, and spintronics-based devices and circuits. He has published extensively in several national and international journals and conferences of repute. Dr. Kaushik is a reviewer of many international journals belonging to various publication houses such as the Institute of Electrical and Electronics Engineers (IEEE), the Institution of Engineering and Technology (IET), Elsevier, Springer, Emerald, and Taylor & Francis. He has delivered many keynote addresses in reputed international and national conferences. He holds the position of Editor and Editor-in-Chief of various journals in the field of VLSI and Microelectronics. He is a senior member of IEEE and has received many awards and recognitions from the International Biographical Center, Cambridge, England. His name has been listed in *Marquis Who's Who in Science and Engineering*® (10th Anniversary, 2008–2009 Edition) and *Marquis Who's Who in the World*® (26th Edition, 2009).



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Manoj Kumar Majumder received his B.Tech and M.Tech degrees from West Bengal University of Technology, Bidhan Nagar, West Bengal, India, and Indian Institute of Engineering Science and Technology (IIST), Shibpur, West Bengal, India, in 2007 and 2009, respectively. He was awarded his PhD degree from the Department of Electronics and Communication Engineering, Indian Institute of Technology Roorkee, Roorkee, Uttarakhand, India, in 2015. He was a Lecturer in the Durgapur Institute of Advanced Technology

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Contents

| | |
|---|-----------|
| Preface..... | xi |
| Authors | xiii |
| | |
| 1. Three-Dimensional Technology and Packaging Techniques | 1 |
| 1.1 Introduction | 1 |
| 1.1.1 Conventional Packaging Techniques | 1 |
| 1.1.2 Limitations | 4 |
| 1.1.3 Recent Advances in Packaging Technology | 4 |
| 1.2 Packaging Techniques of Future ICs | 5 |
| 1.2.1 Silicon Interposer Technology | 7 |
| 1.2.2 Through Silicon Vias | 8 |
| 1.2.3 Hybrid Packaging Technique | 9 |
| 1.2.4 Silicon-Less Interconnect Technology | 10 |
| 1.2.5 Comparison of Different Packaging Techniques | 11 |
| 1.3 3D Integrated Architectures | 14 |
| 1.3.1 3D Integrated Microprocessor | 14 |
| 1.3.2 SRAM Array Integration | 14 |
| 1.3.3 Network-on-Chip Architecture | 15 |
| 1.3.4 Wireless Sensor Network Architecture | 16 |
| 1.4 Summary | 17 |
| Multiple Choice Questions | 18 |
| Short Questions | 19 |
| Long Questions | 20 |
| References | 20 |
| | |
| 2. Through Silicon Vias: Materials, Properties, and Fabrication..... | 23 |
| 2.1 Introduction | 23 |
| 2.2 History of Graphene | 24 |
| 2.3 Carbon Nanotubes | 25 |
| 2.3.1 Basic Structure of CNT | 26 |
| 2.3.1.1 Basic Structure of Single-Walled CNT | 26 |
| 2.3.1.2 Basic Structure of Multiwalled CNT | 29 |
| 2.3.2 Semiconducting and Metallic CNTs | 31 |
| 2.3.3 Properties and Characteristics | 33 |
| 2.3.3.1 Strength and Elasticity | 33 |
| 2.3.3.2 Thermal Conductivity and Expansion | 33 |
| 2.3.3.3 Field Emission | 34 |
| 2.3.3.4 Aspect Ratio | 34 |
| 2.3.3.5 Absorbent | 34 |
| 2.3.3.6 Conductivity | 34 |

| | | |
|-----------|---|-----------|
| 2.4 | Graphene Nanoribbons | 37 |
| 2.4.1 | Basic Structure of GNR | 37 |
| 2.4.2 | Semiconducting and Metallic GNRs..... | 39 |
| 2.4.3 | Properties and Characteristics | 40 |
| 2.4.3.1 | MFP of GNR..... | 40 |
| 2.5 | Properties of TSVs..... | 42 |
| 2.5.1 | Electrical Properties..... | 42 |
| 2.5.2 | Thermal Transport..... | 45 |
| 2.5.3 | Mechanical Performance | 48 |
| 2.5.4 | Thermomechanical Properties..... | 54 |
| 2.6 | Fabrication of TSVs..... | 57 |
| 2.6.1 | Via-First TSV..... | 58 |
| 2.6.2 | Via-Middle TSV..... | 58 |
| 2.6.3 | Via-Last TSV | 59 |
| 2.6.4 | Etching..... | 59 |
| 2.6.5 | Deposition of Oxide..... | 60 |
| 2.6.6 | Barrier Layer or Seed Layer..... | 60 |
| 2.6.7 | Via Filling/Plating..... | 61 |
| 2.6.8 | Chemical Mechanical Polishing | 62 |
| 2.6.9 | Wafer Thinning..... | 62 |
| 2.7 | Challenges for TSV Implementation | 63 |
| 2.7.1 | Cost | 63 |
| 2.7.2 | Design..... | 64 |
| 2.7.3 | Testing | 65 |
| 2.7.4 | Warpage Occurrence..... | 65 |
| 2.7.5 | Manufacturing | 66 |
| 2.8 | Summary | 66 |
| | Multiple Choice Questions..... | 67 |
| | Short Questions | 69 |
| | Long Questions | 70 |
| | References | 70 |
| 3. | Copper-Based Through Silicon Vias | 75 |
| 3.1 | Introduction | 75 |
| 3.2 | Physical Configuration..... | 76 |
| 3.3 | Modeling of Cu-Based TSVs | 78 |
| 3.3.1 | Scalable Electrical Equivalent Model of Coupled TSVs with Bumps..... | 79 |
| 3.3.2 | Modeling of Multicoupled TSVs..... | 82 |
| 3.3.3 | Modeling of Coupled TSVs with MES Ground Structure | 83 |
| 3.3.4 | Modeling of TSVs with Ohmic Contact in Silicon Interposer..... | 83 |
| 3.4 | Performance Analysis of Cu-Based TSVs | 86 |
| 3.4.1 | Propagation Delay and Power Dissipation | 86 |

| | | |
|-------|--|----|
| 3.4.2 | Crosstalk-Induced Delay..... | 87 |
| 3.4.3 | Frequency Response and Bandwidth Analysis..... | 89 |
| 3.5 | Summary..... | 92 |
| | Multiple Choice Questions..... | 93 |
| | Short Questions..... | 94 |
| | Long Questions..... | 95 |
| | References..... | 95 |

4. Modeling and Performance Analysis of CNT-Based

| | | |
|-------|---|-----|
| | Through Silicon Vias..... | 97 |
| 4.1 | Introduction..... | 97 |
| 4.2 | Physical Configuration..... | 99 |
| 4.3 | Real Possibilities of CNT-Based TSVs..... | 100 |
| 4.3.1 | Imperfect Metal–Nanotube Contact Resistance..... | 100 |
| 4.3.2 | Densely Packed CNT Bundles..... | 100 |
| 4.3.3 | Chirality Control..... | 100 |
| 4.3.4 | Defect-Free CNTs..... | 100 |
| 4.3.5 | Higher Growth Temperature of CNTs..... | 101 |
| 4.4 | Modeling..... | 101 |
| 4.4.1 | Compact AC Model of SWCNT Bundled TSVs..... | 101 |
| 4.4.2 | Simplified Transmission Line Model of a TSV Pair..... | 106 |
| 4.4.3 | Modeling of MWCNT-Based TSV..... | 110 |
| 4.5 | Performance Analysis..... | 113 |
| 4.5.1 | Propagation Delay and Power Dissipation Analysis..... | 113 |
| 4.5.2 | Crosstalk Analysis..... | 115 |
| 4.5.3 | Frequency Response and Bandwidth Analysis..... | 116 |
| 4.6 | Conclusion..... | 118 |
| | Multiple Choice Questions..... | 120 |
| | Short Questions..... | 121 |
| | Long Questions..... | 122 |
| | References..... | 122 |

5. Mixed CNT Bundled Through Silicon Vias.....

| | | |
|-------|--|-----|
| 5.1 | Introduction..... | 125 |
| 5.2 | Configurations of Mixed CNT Bundled TSVs..... | 126 |
| 5.2.1 | Physical Configuration of a TSV Pair..... | 126 |
| 5.2.2 | Mixed CNT Bundled TSVs..... | 127 |
| 5.3 | Modeling of MCB-Based TSVs..... | 129 |
| 5.4 | Signal Integrity Analysis of MCB-Based TSVs..... | 131 |
| 5.4.1 | Worst-Case Crosstalk-Induced Delay for Different TSV Pitches..... | 132 |
| 5.4.2 | In-Phase and Propagation Delay for Different TSV Heights..... | 134 |
| 5.4.3 | Noise Peak Voltage for Different TSV Heights..... | 136 |

| | | |
|-----------|---|------------|
| 5.5 | Summary | 139 |
| | Multiple Choice Questions | 139 |
| | Short Questions | 141 |
| | Long Questions | 141 |
| | References | 142 |
| 6. | Graphene Nanoribbon-Based Through Silicon Vias | 145 |
| 6.1 | Introduction | 145 |
| 6.2 | Configurations of GNR-Based TSVs | 146 |
| 6.3 | Fabrication Challenges and Limitations | 147 |
| 6.4 | Modeling of GNR-Based TSVs with Smooth Edges | 149 |
| 6.5 | Modeling of GNR-Based TSVs with Rough Edges | 153 |
| 6.6 | Signal Integrity Analysis of GNR-Based TSVs | 154 |
| 6.6.1 | Propagation Delay for Cu-, SWCNT-, MWCNT-, MCB-, and GNR-Based TSVs | 155 |
| 6.6.2 | Crosstalk-Induced Delay for Cu-, SWCNT-, MWCNT-, MCB-, and GNR-Based TSVs | 156 |
| 6.7 | Summary | 157 |
| | Multiple Choice Questions | 157 |
| | Short Questions | 159 |
| | Long Questions | 159 |
| | References | 160 |
| 7. | Liners in Through Silicon Vias | 163 |
| 7.1 | Introduction | 163 |
| 7.2 | Types of Liners | 164 |
| 7.3 | Fabrication of TSVs with Polymer Liner | 165 |
| 7.3.1 | Polymer Deep Trench Filling | 166 |
| 7.4 | Modeling of CNT Bundled TSV with SiO ₂ Liner | 167 |
| 7.5 | Impact of Polymer Liners on Delay | 171 |
| 7.6 | Summary | 174 |
| | Multiple Choice Questions | 174 |
| | Short Questions | 176 |
| | Long Questions | 176 |
| | References | 177 |
| 8. | Modeling of Through Silicon Vias Using Finite-Difference Time-Domain Technique | 179 |
| 8.1 | Introduction to Finite-Difference Time-Domain Technique | 179 |
| 8.1.1 | Working with the FDTD Method | 179 |
| 8.1.2 | Stability Criterion for FDTD | 180 |
| 8.1.3 | Central Difference Approximation | 180 |

- 8.2 FDTD Model 181
 - 8.2.1 TSV Line Equation 182
 - 8.2.2 Discretization in Space and Time 182
 - 8.2.3 Leapfrog Time Stepping 185
 - 8.2.4 Incorporation of Boundary Conditions 185
 - 8.2.4.1 Boundary Matching at the Source End 186
 - 8.2.4.2 Boundary Matching at the Load End 187
 - 8.2.5 FDTD Model for TSV Terminated by a Resistive Load 187
 - 8.2.6 FDTD Model for TSV Terminated by a Capacitive Load 188
 - 8.2.7 FDTD Model for TSV Driven by a Resistive Driver 189
 - 8.2.8 FDTD Model for CMOS Gate-Driven TSV 191
 - 8.2.9 FDTD Model for Coupled Transmission Line 194
- 8.3 Performance Analysis of TSVs 195
 - 8.3.1 Crosstalk Noise 195
 - 8.3.1.1 Functional Crosstalk 196
 - 8.3.1.2 Dynamic Crosstalk 196
 - 8.3.2 Effect of TSV Length Variation 198
- 8.4 Summary 200
- Multiple Choice Questions 201
- Short Questions 202
- Long Questions 203
- References 203
- Answers to Multiple Choice Questions 205
- Index 207

