国外电子信息精品著作(影印版)

# ΣΔ A/D 转换技术在信号调理中的应用

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## 内 容 简 介

本书讲述了连续时间 ΣΔ 模数转换器在无线通信中的应用，尤其重点讲述了 ΣΔ 模数转换器数字化无线通信信道的优点，从能耗的角度分析了 ΣΔ 模数转换器在信号调理中的应用。提出把部分的信号调理集成到 ΣΔ A/D 转换器中的方法，本方法改善了整个信道的功耗和性能的平衡。本书给出了采用这种方法的两个实例，包括电路图、模拟和测试结果，也对基于 ΣΔ 调节的信道和通常解决方法做了比较，采用了理论和实践结合的方法对所提出的方法进行了阐述。



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# 《国外电子信息精品著作》序

20世纪90年代以来，信息科学技术成为世界经济的中坚力量。随着经济全球化的进一步发展，以微电子、计算机、通信和网络技术为代表的信息技术，成为人类社会进步过程中发展最快、渗透性最强、应用面最广的关键技术。信息技术的发展带动了微电子、计算机、通信、网络、超导等产业的发展，促进了生命科学、新材料、能源、航空航天等高新技术产业的成长。信息产业的发展水平不仅是社会物质生产、文化进步的基本要素和必备条件，也是衡量一个国家的综合国力、国际竞争力和发展水平的重要标志。在中国，信息产业在国民经济发展中占有举足轻重的地位，成为国民经济重要支柱产业。然而，中国的信息科学支持技术发展的力度不够，信息技术还处于比较落后的水平，因此，快速发展信息科学技术成为我国迫在眉睫的大事。

要使我国的信息技术更好地发展起来，需要科学工作者和工程技术人员付出艰辛的努力。此外，我们要从客观上为科学工作者和工程技术人员创造更有利于发展的环境，加强对信息技术的支持与投资力度，其中也包括与信息技术相关的图书出版工作。

从出版的角度考虑，除了较好较快地出版具有自主知识产权的成果外，引进国外的优秀出版物是大有裨益的。洋为中用，将国外的优秀著作引进到国内，促进最新的科技成就迅速转化为我们自己的智力成果，无疑是值得高度重视的。科学出版社引进一批国外知名出版社的优秀著作，使我国从事信息技术的广大科学工作者和工程技术人员能以较低的价格购买，对于推动我国信息技术领域的科研与教学是十分有益的事。

此次科学出版社在广泛征求专家意见的基础上，经过反复论证、仔细遴选，共引进了接近30本外版书，大体上可以分为两类，第一类是基础理论著作，第二类是工程应用方面的著作。所有的著作都涉及信息领域的最新成果，大多数是2005年后出版的，力求“层次高、内

容新、参考性强”。在内容和形式上都体现了科学出版社一贯奉行的严谨作风。

当然，这批书只能涵盖信息科学技术的一部分，所以这项工作还应该继续下去。对于一些读者面较广、观点新颖、国内缺乏的好书还应该翻译成中文出版，这有利于知识更好更快地传播。同时，我也希望广大读者提出好的建议，以改进和完善丛书的出版工作。

总之，我对科学出版社引进外版书这一举措表示热烈的支持，并盼望这一工作取得更大的成绩。

中国科学院院士
中国工程院院士
2006 年 12 月

# List of symbols and abbreviations

| Symbol | Description | Unit |
|---|---|---|
| $BW$ | bandwidth of the wanted signal | Hz |
| $C$ | capacitance | F |
| $c$ | linearized quantizer gain for a $\Sigma\Delta$ ADC | |
| $C_0(t)$ | matched filter | |
| CCh | conditioning channel | |
| $d$ | linearized DAC gain for a $\Sigma\Delta$ ADC | |
| $dB_{FS}$ | ratio (in decibels) of the signal power compared to the full-scale power of a digital data format | $dB_{FS}$ |
| $DR$ | dynamic range; i.e. ratio of the maximum signal power to the minimum detectable signal power in the same bandwidth | |
| $DR_{dB}$ | DR expressed in decibels | dB |
| DSP | Digital Signal Processing | |
| $F$ | implementation factor, i.e. the ratio of $FOM(ADC)$ over $FOM(reference\ ADC)$ | |
| $f_a$ | transition frequency from a high-order to a first-order slope of a transfer function | Hz |
| FFB-ADC | filtering-feedback $\Sigma\Delta$ ADC | |
| $f_{ug}$ | unity-gain bandwidth | Hz |
| $f_s$ | Nyquist sample rate | |
| $f_{sw}$ | average switching frequency; i.e. the inverse of the average number of $0-1$ transitions in a digital data sequence | Hz |
| $IM_3$ | ratio of the amplitude of the third-order intermodulation component, to the amplitude of the fundamental signals. The fundamental signals both are applied at half of the full-scale level. | |
| $IM_{3,dB}$ | $IM_3$ expressed in decibels | $dB_c$ |
| $k$ | Boltzmann's constant equaling $1.38 \times 10^{-23} J/K$ | J/K |
| $L$ | order of the loop filter of a $\Sigma\Delta$ ADC | |
| $m$ | over-sampling factor | |
| MASH | multi-stage noise shaping | |
| $N$ | number of bits of a quantizer | |

| Symbol | Description | Unit |
|---|---|---|
| NTF | noise transfer function | |
| $p$ | ratio between the bandwidth of the entire signal (including the wanted and interferer channels) and the bandwidth of the wanted signal only | |
| $P$ | power consumption | W |
| $q$ | ratio of the amplitude of an overall signal, consisting of both wanted and interferer components, to that of the wanted signal only | |
| $SINAD$ | signal/noise-and-distortion ratio; i.e. ratio of the power of the wanted signal to the sum of the noise power and the distortion power. All are integrated over the channel bandwidth and are present simultaneously | |
| $SINAD_{dB}$ | SINAD expressed in decibels | dB |
| $SNR$ | signal/noise ratio; i.e. ratio of the power of the wanted signal to the noise power. Both are integrated over the channel bandwidth and are present simultaneously | |
| $SNR_{dB}$ | SNR expressed in decibels | dB |
| STF | signal transfer function | |
| $T$ | absolute temperature | K |
| $\hat{v}_{IN}$ | instantaneous amplitude of a wanted signal | V |
| $\hat{v}_{MIN}$ | minimum amplitude of a wanted signal | V |
| $\hat{v}_{MAX}$ | maximum amplitude of a wanted signal | V |
| $v_n$ | short-hand notation for the rms value of an input-referred, equivalent noise source, measured over the wanted channel only | V |
| $V_{DD}$ | positive supply voltage | V |
| $V_{SS}$ | negative supply voltage | V |

# Contents

# Chapter 1

# Introduction

## 1.1 Background

Moore's Law predicts a decrease by a factor of two in the feature size of CMOS technology every three years and has been valid for years. It implies a doubling of the operation speed and a four times higher transistor count per unit of area, every three years. The combination leads to an eight times higher processing capability per unit of area. This on-going miniaturization allows the integration of complex electronic systems with millions of transistors (Very-Large-Scale-Integration) and enables the integration of electronic systems.

### An electronic system

A generic picture of an integrated electronic system is shown in fig. 1.1. The heart of the system is the signal processing core. This core supports a wide variety of functions, such as customization and programmability of multiple applications, channel coding, the definition of the user interface, etc. These functions are enabled by DSP, a controller CPU and various blocks of memory. In advanced ICs these blocks provide (almost) all signal processing and usually dominate in the overall power and area consumption of integrated systems. The huge data rates involved, require high-speed busses for communication between these blocks. A power-management unit fuels the system by providing the appropriate supply voltages and currents.

Communication with the physical world is realized by a chain of mixed-signal, analog and RF-circuitry. This chain acts as a "signal-conditioning channel". It translates physical signals into binary representations or vice versa. This channel also comprises amplification, filtering and possibly frequency translation. It is the challenge of present day mixed-signal and RF design to integrate the signal-conditioning channel at a low power consumption and a high performance level.

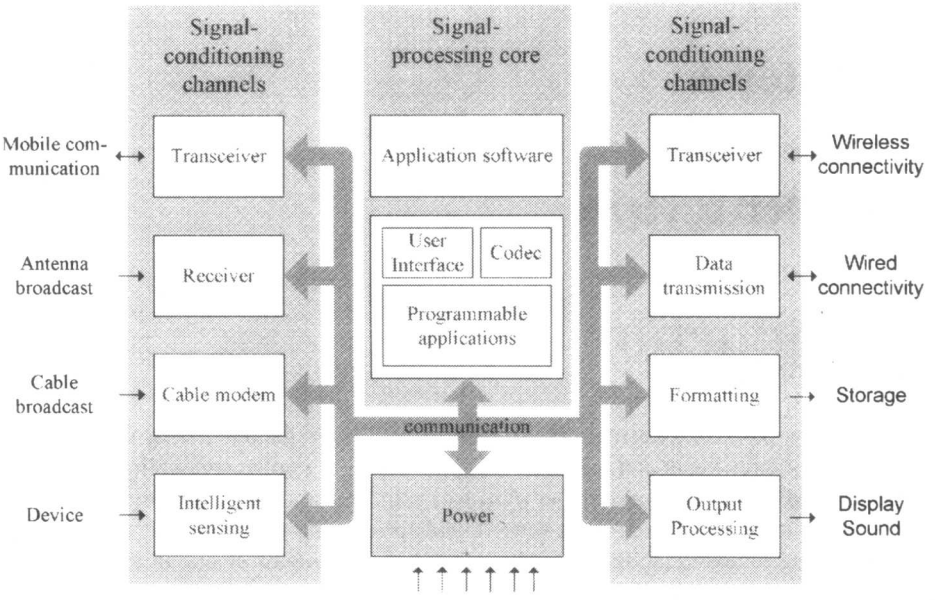


**Figure 1.1:** *Electronic system including "signal-processing" units and some example "signal-conditioning" channels for communication to the physical world [1]*

### Digital signal processing

More and more digital systems and standards have been conceived: DECT has replaced analog cordless systems, CD has overtaken the market of analog audio and digital cameras are conquering conventional photography. These new standards offer higher quality and more features thanks to the digital signal processing. The digital solution is moreover easily scalable to new technologies and changing systems.

Clearly, *in the signal-processing arena "full-digital" is becoming a fact for the majority of systems. A similar evolution is happening to the signal-conditioning channels shown in fig. 1.1 although the feasibility and economics of "highly-digitized signal conditioning" have not yet been proven.*

### Digitization of signal conditioning

Fig. 1.2 depicts a conventional (i.e. dominantly analog) implementation of an A/D and a D/A type of signal-conditioning channel. In fact, this could be the block diagram detailing any of the signal-conditioning channels introduced in fig. 1.1. These channels select the wanted signal in the time and the frequency domain, amplify the wanted signal, suppress interferer signals and noise, perform A/D or D/A conversion and de- or encoding of the signal.

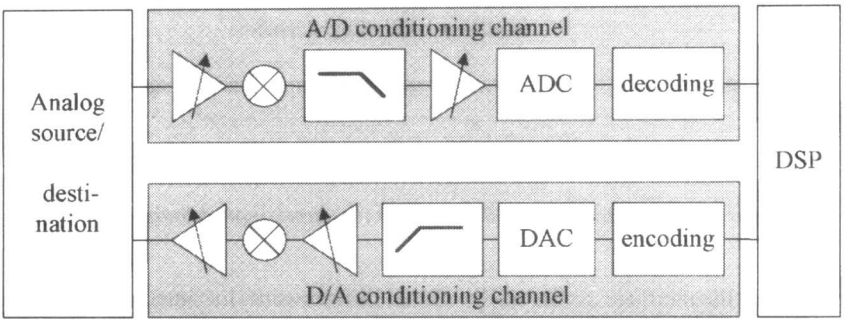


**Figure 1.2:** *Block schematic of conventional A/D and D/A conditioning channel*

The signal conditioning happens in either the analog or the digital domain[1]. Predominant analog signal conditioning relaxes the bandwidth and the dynamic range requirements of all the following blocks. Predominant digital conditioning reduces the number of analog blocks needed, while the implementation of the digital blocks benefits from Moore's Law. The requirements imposed on the data converters, however, become substantially stricter. As the ADC and DAC move towards the antenna a much higher sample rate and significantly higher resolution and linearity are required (see example on page 15).

While digital processing seems to come for free in advanced CMOS technologies, any performance increase of analog circuitry leads to higher power consumption. Moreover, migration of an analog circuit to a new technology generation may imply a power increase, even at constant performance requirements [3], [4]. Although some transistor parameters have improved in advanced technologies, the negative effect of the decreasing supply voltage has over-compensated this for generations beyond 0.25$\mu$m-CMOS [5]. Therefore, new circuit techniques need to be developed in order to bridge this performance gap. Evolution in analog circuit techniques is, however, very slow in comparison with the revolution that has taken place in the complexity of digital processing and algorithms.

Obviously, *digitization of the signal-conditioning channel in an advanced CMOS technology, imposes a substantial burden on the analog circuits and on the data converters especially. All-digital signal conditioning is therefore not necessarily the best option in view of the overall optimization of the signal-conditioning channel.*

### Digitization of inter-die interfaces

The signal-conditioning channel can be integrated on a single die or often it extends over multiple dies (in order to take advantage of a dedicated technology or for reasons of standardization of the interface). In the latter case, digitization of the channel may lead to a

[1] In this book, it is assumed that de- and encoding of the signal occurs in the digital domain. This is obvious for digital communication schemes but is also becoming the de-facto implementation for analog systems. A good example are FM radio receivers in which analog demodulation -although adequate and low-cost- is substituted by digital demodulation [2] featuring all the previously mentioned advantages.

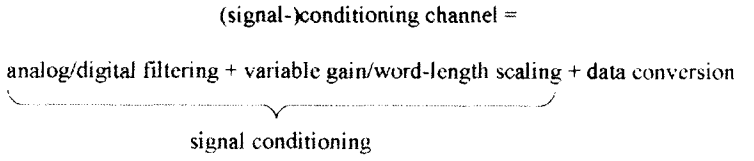


**Figure 1.3:** *Nomenclature with respect to the signal-conditioning channel*

new inter-die interface: as the ADC or DAC shifts towards the antenna a previously analog interface may be replaced by a digital interface. Hence, the cost of an inter-die interface will strongly depend on the degree of digitization of the signal-conditioning channel, and must be included in the overall optimization of the cost/performance ratio of the channel.

## 1.2 Scope

This book studies the digitization of the signal-conditioning channel. In particular, it focuses on the consequences of digitization on the power consumption of the channel in relation to the performance target. The target "performance" is evaluated in terms of noise, distortion and bandwidth. In generic terms, the aim of this book is to *improve the power/performance relation of the conditioning channel by balancing analog and digital signal conditioning*. This is pursued while striving for a highly-digitized solution. Some limitations on the scope of the text are briefly motivated next.

### Baseband A/D conditioning channels

The text focuses on signal conditioning in an A/D type of channel, operating at baseband. The key circuits in the analysis are filters, variable-gain amplifiers and data converters. At present, digitization of this (part of the) signal-conditioning channel -though very challenging still- is becoming feasible for various systems. On the contrary, power-efficient digitization at the IF or RF frequency can be considered as a next -but further-off- step. In addition, the de- and encoding of the signal are left out because the digitization of these blocks has become a reality already.

The nomenclature as defined in fig. 1.3 will be used. "Conditioning channel" is used as a shorthand notation for "signal-conditioning channel". As explained above, it only refers to the conditioning actions identified in fig. 1.3. Moreover, the term "signal conditioning" only refers to filtering and variable gain or word-length scaling, without the data conversion. In chapter 6, this functionality is integrated into a $\Sigma\Delta$ ADC. Then, the terminology of "a conditioning $\Sigma\Delta$ ADC" is used.

### Continuous-time single-bit sigma-delta conversion

The choice for sigma-delta data conversion is motivated by the evolution of CMOS technology and the system need for low power data conversion (see chapters 2 and 3) and by

the potential of sigma-delta converters for digitizing the conditioning channel in a power efficient way. The latter argument is demonstrated throughout the book.

This choice does limit the analysis to channels with a "narrow" bandwidth. At present, $\Sigma\Delta$ ADCs with a signal bandwidth up to 40MHz have been reported [6] in CMOS. For this range of bandwidths $\Sigma\Delta$ converters enable low-power, high-performance conditioning channels.

This is especially true in case a continuous-time loop filter is used as this alleviates the requirements on preceding anti-aliasing filtering. In addition, most continuous-time implementations have a better power/performance ratio than their switched-capacitor counterparts often due to lower bandwidth requirements on the filter stages [7].

Single-bit quantization provides high-linearity. This is a major specification on the ADC in case analog conditioning -limiting bandwidth and *DR* of the input signal- is traded for digital conditioning.

Motivated by the above promise of an attractive cost/performance ratio the text concentrates on continuous-time, single-bit $\Sigma\Delta$ -ADCs (see also 3.2.1).

### CMOS technology

The choice for a baseband mixed-signal channel justifies a further narrowing of the scope to CMOS technology only. While CMOS is gaining ground in many application areas, it is certainly doing so in the field of analog and mixed-signal baseband design. This follows from the number of scientific publications in this area.

### Power consumption as cost parameter

The optimization of the signal-conditioning channel is performed in a single cost dimension, being power consumption. This is certainly a viable choice for portable applications aiming at long stand-by times and small and light-weight battery packs. In general, low power consumption can be an important asset in view of limited heat sinking capabilities of packages, in view of area required by fans, etc.

The analysis aims at calculating the relation between the current consumption and the performance requirements. The maximum supply voltage is assumed to be dictated by the technology choice.

### Performance parameters

In view of the comparison of various architectures for the conditioning channel a limited set of performance parameters needs to be identified. These parameters need to represent a fundamental specification on a generic signal-conditioning channel, influence the balancing of analog and digital conditioning and influence the power consumption. Based on Shannon's theory on the capacity of a generic communication channel a meaningful set of parameters is derived in section 2.2. These parameters relate to signal bandwidth, signal amplitude, noise power and distortion. The associated nomenclature is discussed in section 2.5.

For now it is mentioned that only (white) thermal circuit noise is taken into account. Other noise sources like flicker noise and shot noise only occur in a limited frequency band and therefore are less generic.

Only differential circuits are considered such that third-order distortion dominates. Differential operation is preferable in a mixed-signal environment anyway. Furthermore it is assumed that all circuits operate under weakly non-linear conditions which implies that the response at the $n^{th}$ harmonic is only determined by the $n^{th}$ order non-linearity.

## 1.3 Outline

The book starts with a study of a generic signal-conditioning channel in chapter 2. Applying Shannon's theory, the choice of the performance parameters is further motivated. It is explained how system evolution and technology advances affect the conditioning channel and digitization is identified as a key challenge. In addition, some nomenclature is introduced.

Chapter 3 presents an overview of state-of-the-art in $\Sigma\Delta$ A/D converter design and motivates the assets of $\Sigma\Delta$ converters for digitization of the conditioning channel. For completeness, we briefly touch upon limitations on the application of $\Sigma\Delta$ converters.

In chapter 4, power/performance relations for the building blocks of the conditioning channel -i.e. for a major class of analog circuits, for the $\Sigma\Delta$ ADC and for the decimation filter- are derived. This leads to conclusions on how to proceed in view of power-efficient digitization. Further on, these results are used to compare conditioning channels, with a varying degree of digitization, in terms of their power/performance balance.

In chapter 5, we study a full-analog and a full-digital conditioning channel. These represent the two extremes in terms of digitization and are compared with respect to power consumption.

Chapter 6 introduces the concept of "conditioning $\Sigma\Delta$ ADCs". Instead of having analog conditioning, in front of the ADC, or performing the conditioning in the digital domain, it is integrated into the $\Sigma\Delta$ loop. This concept is enabled by the fact that $\Sigma\Delta$ ADCs are largely immune to interferers. The analysis of the interferer immunity and of the limitations thereon, is a key topic of this chapter. In addition, various $\Sigma\Delta$ topologies are evaluated in this perspective and a "filtering-feedback $\Sigma\Delta$ ADC" -explicitly designed for interferer immunity- is presented. Again, the power/performance balance of the various solutions is assessed as well.

Often, the signal-conditioning channel extends over multiple dies. In that case, digitization of the conditioning channel, may lead to digitization of the inter-die interface as well. This is the topic of chapter 7.

Chapters 8 and 9, present design examples as an illustration of the theory of chapters 5 and 6 respectively. A dual-mode receiver for FM/AM radio is considered in chapter 8. In FM mode, the signal conditioning is highly analog. In AM mode, it is highly digitized using multi-channel A/D conversion. In chapter 9, three implementations of a "conditioning $\Sigma\Delta$ ADC" for use in a Bluetooth receiver are discussed. The first design is attractive for systems requiring a high *SNR* for the digital processing. The other two designs enable