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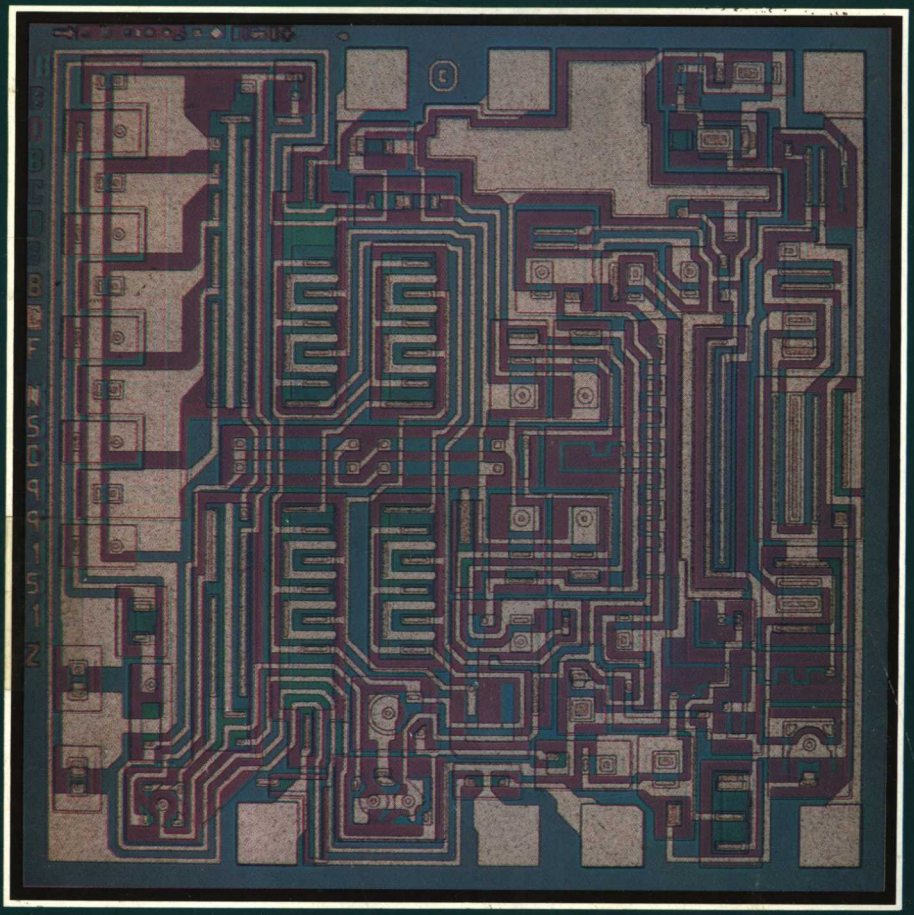
THE

# LINEAR IC HANDBOOK

MICHAEL S. MORLEY



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# Introduction

THE PURPOSE OF THIS BOOK IS TO PROVIDE BOTH TUTORIAL information and technical data to aid electronics circuit designers in the selection of standard linear integrated circuits. This book was written for engineers, technicians, and hobbyists—in short, anyone who designs electronics circuits for any purpose.

During the course of a design assignment, the circuit designer must answer the following questions:

(1) What are the requirements?
(2) What are the alternative circuit design approaches?
(3) What components are available to do the job?
(4) How do I apply these components to my design to assure high yield and reliability?

The number one job is to understand the requirements. If this is done poorly, then the design will have to be redone (assuming there is some means in place for determining whether your design meets the requirements, i.e., design reviews and product assurance reviews). After you understand the design requirements, then you will answer questions 2-4 for each "paper design" you think of. The answer to these questions usually drives the design to one or two good design alternatives. The rest of the time, or a big percentage of it, is spent doing component trade studies. For that, you

need specific technical information. You are looking for the "right" IC for the job—the least expensive IC that will do the job with some (but not too much) design margin. What do you do? You wade through a dozen or more IC books, looking up this or that IC, comparing the IC specifications with your requirements. And you look up the prices, or call the local sales representative to get a budgetary price.

The purpose of this book is to reduce the amount of time that you spend looking for a particular linear IC. Suppose, for example, that you need a low-noise op amp. The selection guides in Table 4-22 through 4-24 list low-noise op amps for the commercial, industrial, and military temperature ranges by part number, manufacturer, input noise voltage, input noise current, and price. From there you can go to Appendix A and get some more data—bandwidth, slew rate, input offset voltage, power supply current, and other data. Beyond this you will have to go to the manufacturer's data sheet or databook.

There are no pinouts in this book. No curves. It is not the purpose of this book to replace the databooks of a dozen or more linear IC manufacturers. (1) This book isn't big enough. (2) It's not, and never will be, an official databook. (3) Although I have tried to carefully copy (and in some cases, interpret) the manufacturers' data, I am sure that in a book this size that there are at least a few errors. The point is this: use this book to quickly locate an IC, but do not base any designs on the data in this book alone.

Also, there is price information in this book, but you should not consider this book an official price book for two reasons: (1) The price data in this book is out of date. It was out of date when I got it (fall of 1984). In fact, the only up-to-date prices are those you get when you formally ask a supplier for a quotation. (2) The price of any particular IC in this book is the lowest price for that IC. For example, if there is more than one package available for a given part type, I have listed the unit price for the lowest cost package version, probably plastic.

Then why has the price been given? Because IC cost is a big factor in circuit design. The prices in this book are old, but they are important because they tell you the *relative* price you must pay to get a certain performance. The name of the game is to get the most performance for your money. Never select a more expensive part than you need to do the job (with some performance margin for worst case conditions). (For me, learning the prices of the ICs listed in this book was one of the more interesting aspects of writing this book. I quickly found out which manufacturers generally produce the more expensive parts. And not all of these parts had the best performance!)

The structure of this book is as follows:

Part I is about linear IC fundamentals: fabrication (Chapter 1), components (Chapter 2), and design techniques (Chapter 3). This is background information for linear IC users, not a course for linear IC designers. Advanced IC design techniques are beyond the scope of this book.

Part II provides a basic tutorial section and a set of selection guides for seven major linear IC types: op amps (Chapter 4), comparators (Chapter 5), voltage references (Chapter 6), voltage regulators (Chapter 7), D/A converters (Chapter 8), A/D converters (Chapter 9), and sample-and-hold amplifiers (Chapter 10). The largest chapter is on op amps for two reasons: (1) There are more op amp types available than any other linear IC. (2) The design techniques used in op amps are fundamental to all other linear ICs. A thorough understanding of op amp design techniques will help you understand other linear IC types more quickly. The tutorials in the other chapters assume you understand the op amp material. This is true in general: the later chapters are based on the ideas presented in earlier chapters.

Part III is devoted to other linear ICs: special-purpose amplifiers (Chapter 11), analog math blocks (Chapter 12), timers and oscillators (Chapter 13), and transistor, amplifier, and diode arrays (Chapter 14). Each of these chapters presents tutorial and selection guides for four or five types of linear ICs that have similar or related functions. None of these categories have a large number of available part types. Nevertheless, the linear IC types presented in these chapters perform standard functions and have broad applications. Every circuit designer should be aware of these parts, how they work, and about how much they cost.

The Appendices are a set of specification summary tables by IC type and then by manufacturer. The data in the Appendices was compiled first, before the text sections were written and before the selection guide tables were created. I used a database program to enter the raw data into my computer and then used a sorting/report program to create the selection guides given in Part II.

The Appendices are purposely incomplete. For example, Texas Instruments makes the following op amps: μA709, LM108, SE5534, MC1558, and the OP-07. None of these op amps are included in the Texas Instruments section of Appendix A. However, you can find the μA709 under Fairchild, the LM108 under National, the SE5534 under Signetics, the MC1558 under Motorola, and the OP-07 under Precision Monolithics Incorporated (PMI) because these manufacturers are the original sources for these ICs. (In general, the prefix tells you the original source—μA for Fairchild, LM for National, and so forth.) Therefore, any part that has exactly the same prefix as the original part is not listed in Appendix A. Since the specifications are the same, the only thing lost is the

price data, which should be approximately the same.

This does not mean that all alternate sourced parts are not included. For example, National makes the LM709, an alternate source to the Fairchild μA709. Both parts are in the Appendix. The rule I used for including parts in the Appendix (and also the selection guides) is this: If manufacturer A made a part with the same prefix (and number) as manufacturer B (the original manufacturer), then the part made by manufacturer A was not included. If manufacturer A made a part with the same number but a different prefix than manufacturer B, then both parts were included. These conditions correspond to two cases. In the first case (same prefix), the IC appears to be a straight copy, probably a mask exchange and licensing agreement. In the second case, it appears that a new IC has been designed to previously published specifications. The schematic is different, and probably there is no licensing agreement. Also, the redesigned part may not have exactly the same specifications. It's your responsibility (not your purchasing agent's) to make sure that alternate sourced ICs will meet your application's requirements.

# Contents

# Chapter 1

# Linear IC Fabrication

A PHOTOGRAPH OF A SIMPLE LINEAR INTEGRATED CIRCUIT is shown in Fig. 1-1. Understanding how this particular chip and linear ICs in general are made is the purpose of this chapter. This is important because the performance of linear ICs is directly related to how the circuit components are fabricated.

## MASK GENERATION

The chip shown in Fig. 1-1 was made using a set of masks, analogous in some ways to the artwork used in the generation of a multilayered printed circuit, or PC, board. In the simplest linear IC process, there are at least seven masks. These masks are listed in Table 1-1, on page 16. Figures 1-2 through 1-8 show simplified artwork drawings for the seven masks used to fabricate the chip shown in Fig. 1-1. The process steps associated with these masks will be explained later in this chapter.

As in the case of a PC board, the artwork for these masks is drawn at a much larger scale than the final product. IC mask artwork, in fact, is generally drawn several hundred times (as high as 1000 times) actual size.

The artwork generally is drawn on gridded mylar and then digitized. Digitization is the process whereby the artwork is entered into a computer. To the computer, each layer of the artwork is a

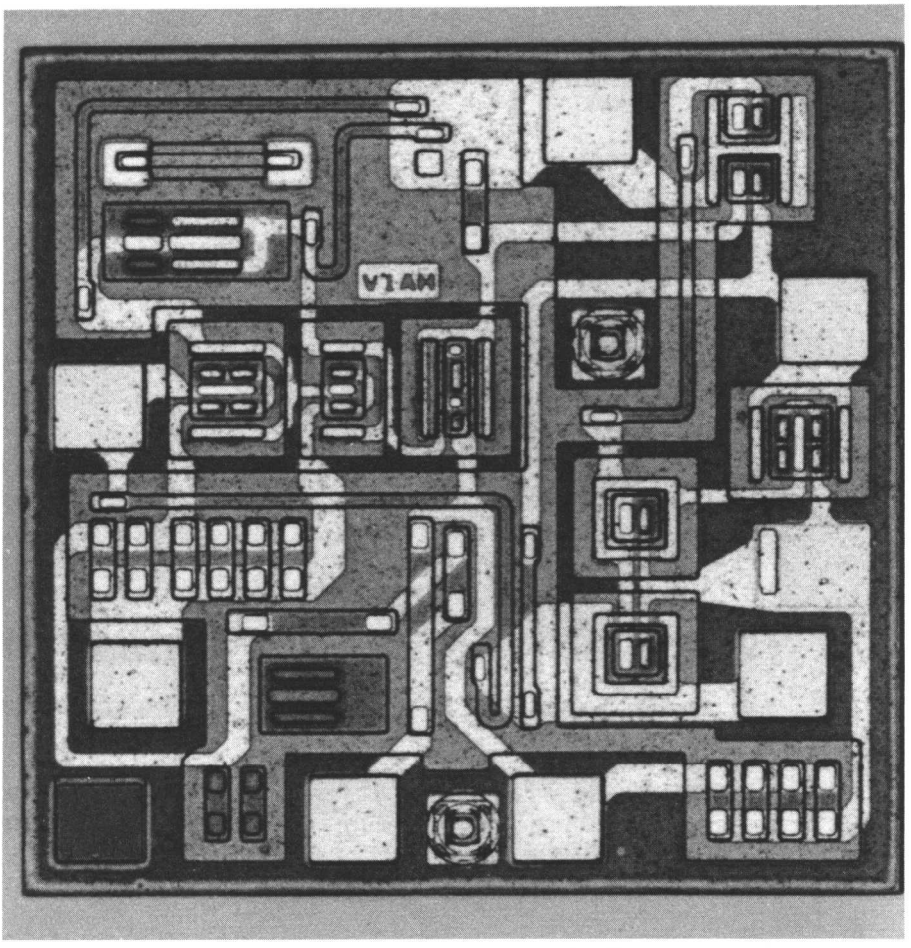

Fig. 1-1. Photograph of a linear IC (courtesy Motorola Semiconductor).

set of geometries defined by sets of coordinates connected by line segments. With the advent of computer-aided design (CAD) workstations, many IC designs today are drawn directly on the terminal screen, thus eliminating the tedious process of drawing and digitizing the artwork.

The physical design, or layout, of the IC is governed by a set of mask design rules, such as minimum rectangle size, minimum width, minimum spacing to another geometry of the same layer or other layer. Some of these rules are the result of the limitation of the photolithography technology used in mask generation. Other rules are defined in order to assure certain electrical performance criteria. For example, base-to-collector breakdown voltage for an NPN transistor is directly related to the spacing between the isolation diffusion (mask 2) and the base diffusion (mask 3).

Next, a 10× (10 times actual size) plate, called a reticle, for each layer is generated from the layout database. The reticle is used to photographically step and repeat a 1× image of a single layer in rows and columns on a square glass plate large enough to cover a 3-inch, 4-inch, or possibly even a 5-inch diameter wafer. (Wafer diameter size historically has been increasing with improved processing methods.)

The plates made from the reticles are called masters. From these are generated a set of masks, called working plates, which are used to fabricate the IC. A simplified drawing of a finished wafer is shown in Fig. 1-9. This figure shows only the chip boundaries and is not to scale. The darkened areas indicate the location of test patterns, which are used to monitor the electrical performance of test transistors and resistors during and after wafer fabrication.

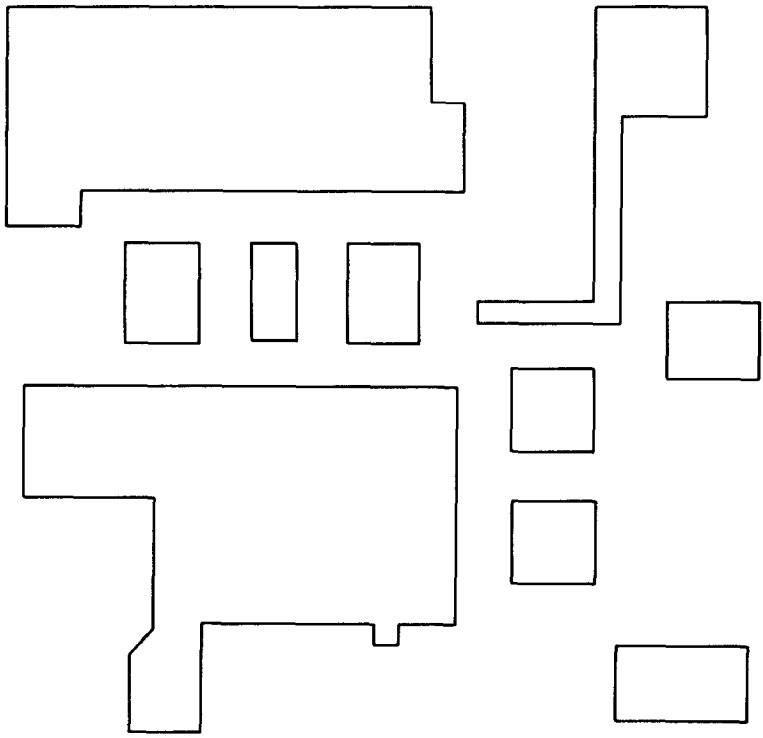

Fig. 1-2. Line drawing of buried layer diffusion artwork (mask 1).

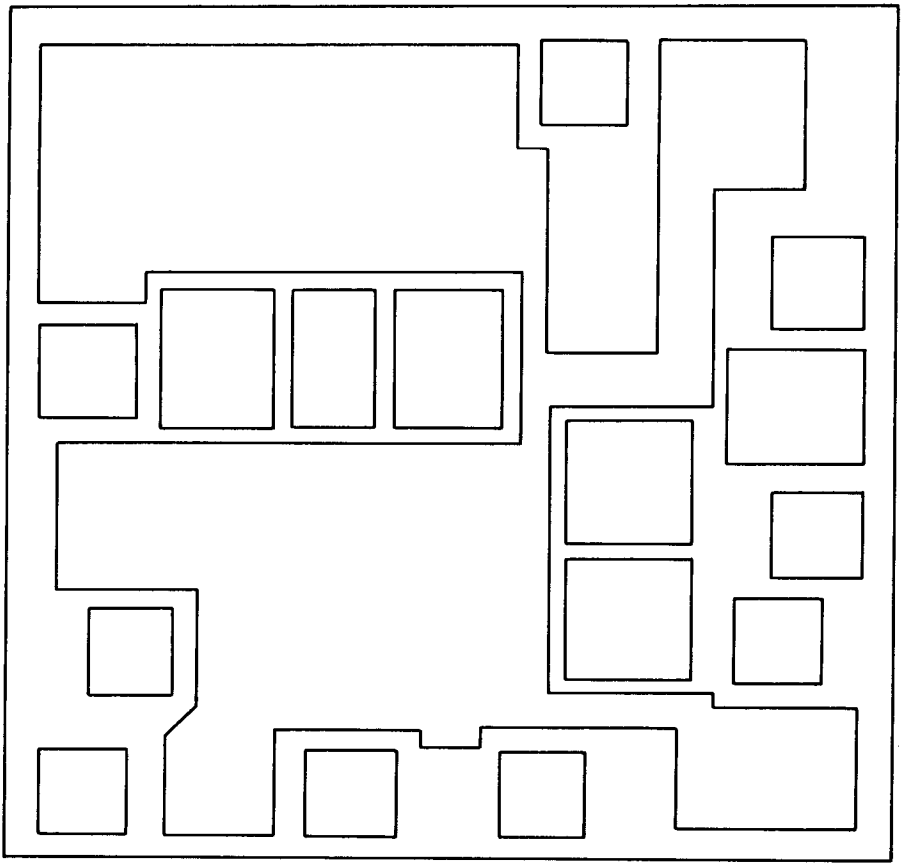

Fig. 1-3. Line drawing of isolation diffusion artwork (mask 2).

## WAFER FABRICATION

A small portion of an IC chip, or die, is shown in Fig. 1-10. This figure shows the top view and side view of a hypothetical, small NPN transistor. The side view is the view seen if you could make a horizontal slice through the middle of the top view of the transistor. Dashed lines are used to indicate that only a portion of the chip is shown.

The top view is approximately to scale with the collector region measuring 95 microns long by 67 microns wide, or 0.00374 inches by 0.00264 inches (25.4 microns equals 0.001 inch, or 1 mil). The side view is not to scale. The diffusions and layers are deeper or thicker (as in the case of the epitaxial layer) than the scale of the top view would indicate. This liberty has been taken in order to be able to clearly show the various transistor regions.

Now, let's see how each of these regions is formed.

### Buried Layer Diffusion

The formation of the buried layer is shown in Fig. 1-11. The starting material is a P-type silicon wafer approximately 15 to 20 mils thick (Fig. 1-11A). P-type silicon is made by introducing atoms with three electrons in their outer shells. Because silicon has four electrons in its outer shell, vacancies, or holes, are formed when the covalent bonds are formed (two electrons per covalent bond, eight electrons to completely fill the outer shell). Because holes have a positive charge, the material is called P-type. (N-type material is made by introducing atoms with five electrons in their outer shells. When the covalent bonds are formed, one free electron is generated for each dopant atom. Since electrons are negatively charged, the material is called N-type.)

**Step 1.** A thin layer of silicon dioxide is grown on the surface (Fig. 1-11B). The silicon dioxide is a form of glass and acts as a

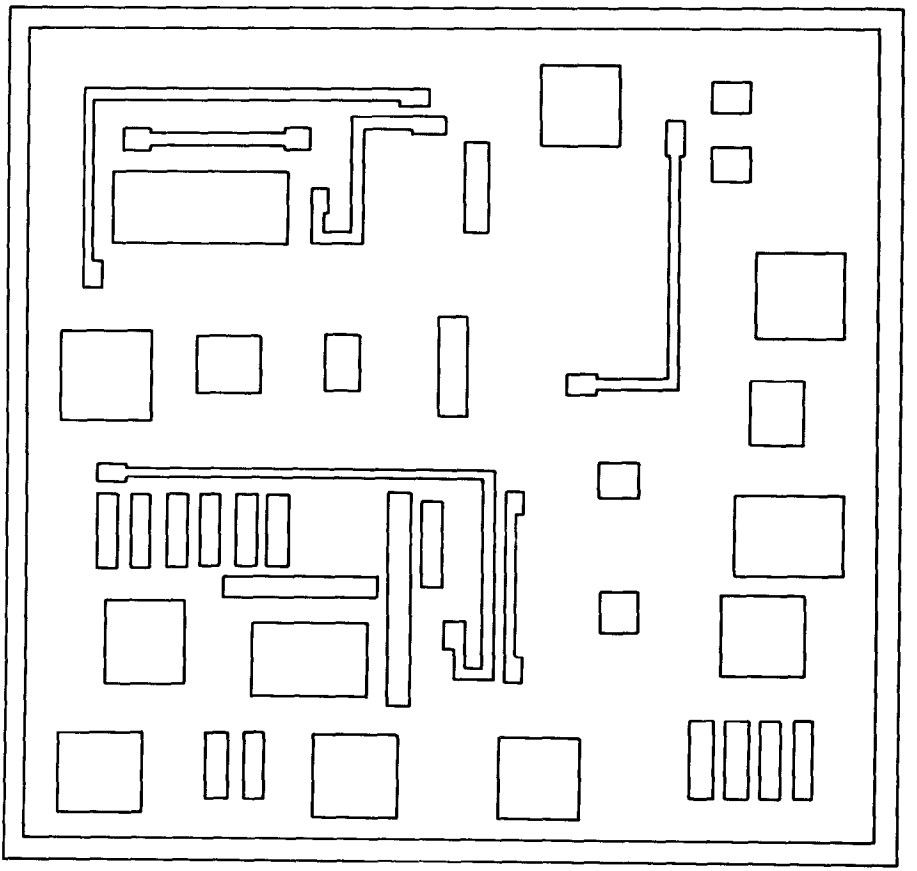

Fig. 1-4. Line drawing of base diffusion artwork (mask 3).

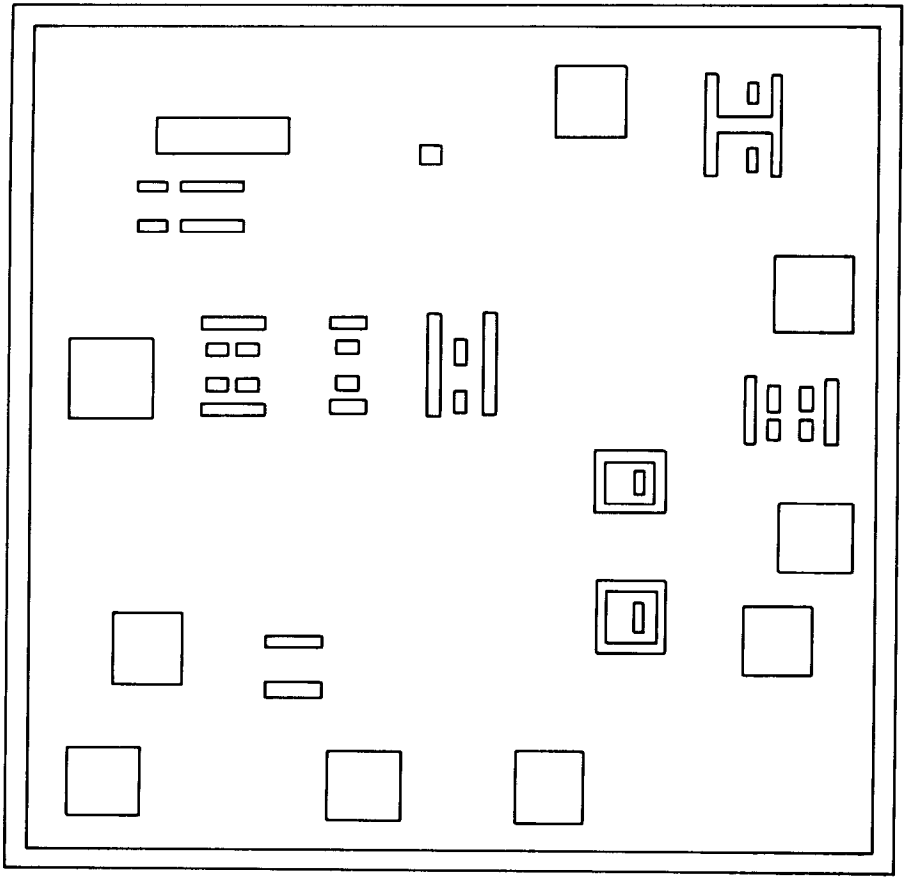

Fig. 1-5. Line drawing of emitter/collector diffusion artwork (mask 4).

barrier, preventing unwanted impurities from diffusing into the silicon.

**Step 2.** A layer of photoresist is deposited on top of the silicon dioxide (Fig. 1-11C).

**Step 3.** The glass mask with the buried layer pattern on it is placed on the wafer and is exposed to ultraviolet light (Fig. 1-11D). The photoresist is hardened in all areas except those areas covered by the mask pattern.

**Step 4.** The unexposed photoresist is washed away (Fig. 1-11E).

**Step 5.** The silicon dioxide not covered by the photoresist is chemically etched away (Fig. 1-11F).

**Step 6.** The remaining photoresist is removed (Fig. 1-11G).

**Step 7.** Impurity atoms with five electrons in their outer shells are diffused into the silicon through the oxide windows formed in steps 1-6 (Fig. 1-11H). The silicon just below the exposed surface

becomes N-type. The buried layer is called "N+" because the number of free electrons is higher in this region than in the so-called epitaxial N-type layer formed in the next step. The depth and impurity concentration of the buried layer diffusion is a function of oven temperature and exposure time. The purpose of the buried layer is to reduce the collector resistance of the NPN transistors.

### Epitaxial Layer

The oxide remaining from the formation of the buried layer is removed and N-type silicon is grown on the surface of the wafer (Fig. 1-12). This is the epitaxial layer. The thickness and impurity concentration of the epitaxial layer directly affect transistor breakdown voltage and collector resistance. For a medium voltage linear IC process, the epitaxial layer thickness may be in the range

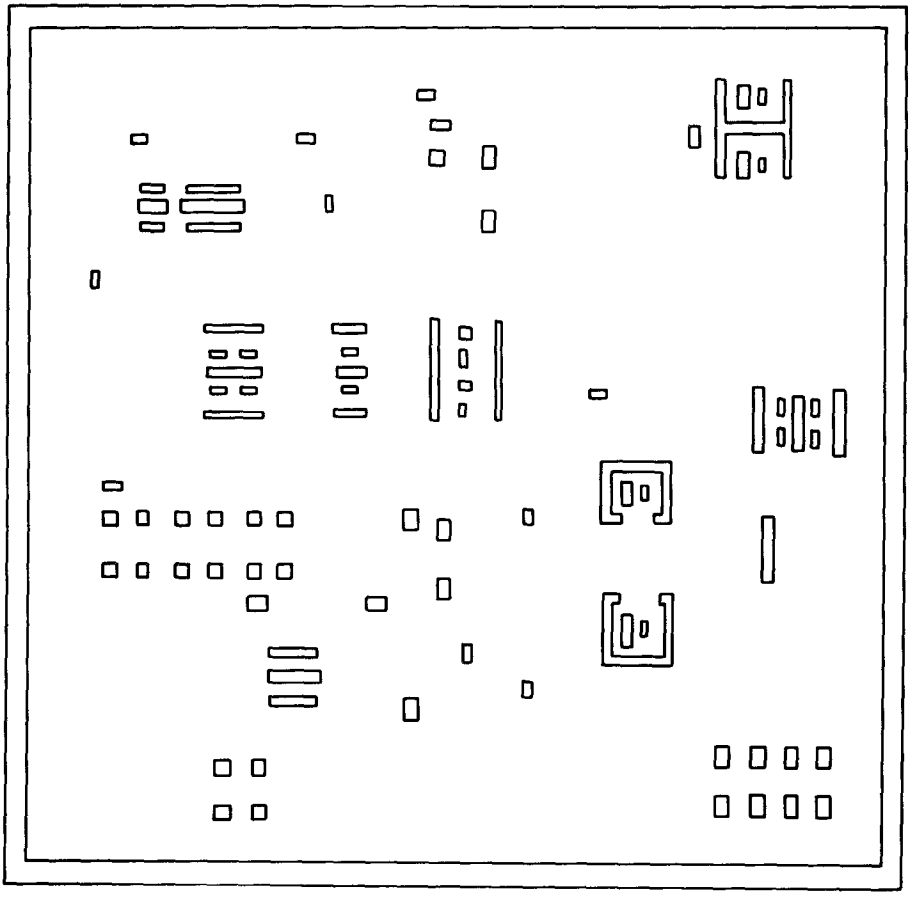

Fig. 1-6. Line drawing of contact oxide opening artwork (mask 5).

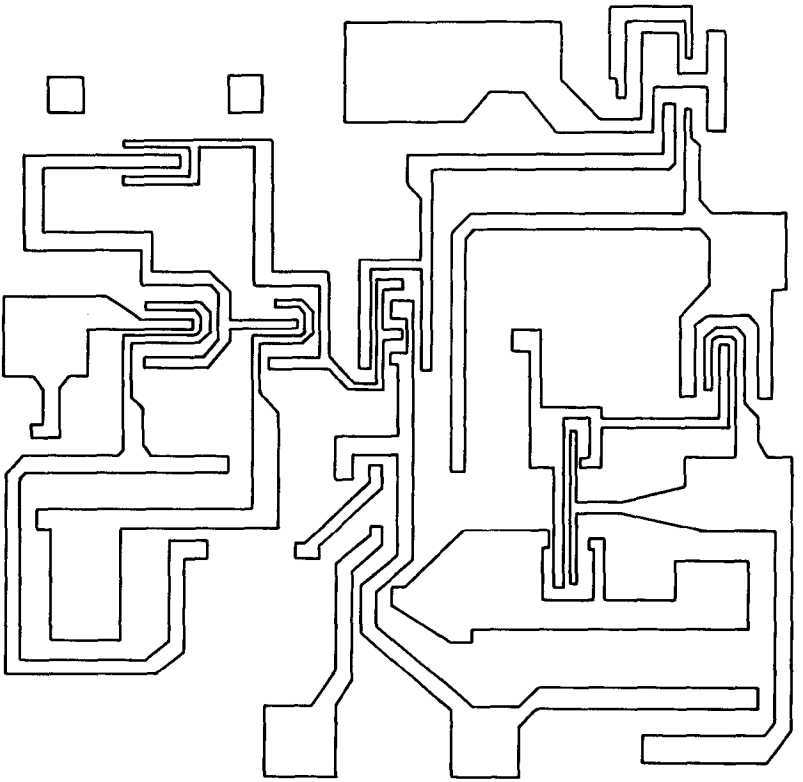

Fig. 1-7. Line drawing of metalization artwork (mask 6).

of 10-15 microns. This is very thin when compared to the thickness of the substrate, which, as stated earlier, is in the range of 15 to 20 mils (381 to 508 microns).

### Isolation, Base, and Emitter Diffusions

The same process steps shown in Fig. 1-11A through 1-11H is repeated for the isolation, base, and emitter diffusions. The P+ isolation diffusion (Fig. 1-13), as its name implies, isolates one epitaxial island, or tub, from another. The isolation diffusion extends all the way to the P-substrate to insure isolation which is achieved by connecting the substrate to the most negative potential (ground or V–), thus backbiasing the PN junction formed by the P-substrate and the N-epitaxial layer.

An epitaxial island formed by the isolation diffusion may be the collector of an NPN transistor (as shown in Fig. 1-10), the base