Gordon Shaw III · Barton C. Prorok LaVern Starman · Cosme Furlong *Editors*

MEMS and Nanotechnology, Volume 5

Proceedings of the 2013 Annual Conference on Experimental and Applied Mechanics





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Preface

MEMS and Nanotechnology, Volume 5: Proceedings of the 2013 Annual Conference on Experimental and Applied Mechanics represents one of eight volumes of technical papers presented at the SEM 2013 Annual Conference & Exposition on Experimental and Applied Mechanics organized by the Society for Experimental Mechanics and held in Lombard, IL, June 3–5, 2013. The complete Proceedings also includes volumes on: Dynamic Behavior of Materials; Challenges in Mechanics of Time-Dependent Materials and Processes in Conventional and Multifunctional Materials; Advancement of Optical Methods in Experimental Mechanics; Mechanics of Biological Systems and Materials; Experimental Mechanics of Composite, Hybrid, and Multifunctional Materials; Fracture and Fatigue; Residual Stress, Thermomechanics & Infrared Imaging, Hybrid Techniques and Inverse Problems.

Each collection presents early findings from experimental and computational investigations on an important area within Experimental Mechanics, MEMS and Nanotechnology being one of these areas.

Microelectromechanical systems (MEMS) and nanotechnology are revolutionary enabling technologies (ET). These technologies merge the functions of sensing, actuation, and controls with computation and communication to affect the way people and machines interact with the physical world. This is done by integrating advances in various multidisciplinary fields to produce very small devices that use very low power and operate in many different environments. Today, developments in MEMS and nanotechnology are being made at an unprecedented rate, driven by both technology and user requirements. These developments depend on micromechanical and nanomechanical analyses, and characterization of structures comprising nanophase materials.

To provide a forum for an up-to-date account of the advances in the field of MEMS and nanotechnology and to promote an alliance of governmental, industrial, and academic practitioners of ET, SEM initiated a *Symposium Series on MEMS and Nanotechnology*.

The 2013 Symposium is the fourteenth in the series and addresses pertinent issues relating to design, analysis, fabrication, testing, optimization, and applications of MEMS and nanotechnology, especially as these issues relate to experimental mechanics of microscale and nanoscale structures.

It is with deep gratitude that we thank the Organizing Committee, Session Chairs, Authors and Keynote Speakers, Participants, and SEM Staff for making the 13th-ISMAN a valuable and unforgettable experience.

Gaithersburg, MD, USA Auburn, AL, USA Wright-Patterson AFB, OH, USA Worcester, MA, USA Gordon Shaw III Barton C. Prorok LaVern Starman Cosme Furlong

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Chapter 1

Warpage Measurement of Simulated Electronic Packaging Assembly

Ningning Du, George F. Raiser, and W. Carter Ralph

Abstract Digital image correlation is an attractive displacement measurement method for thermo-mechanical characterization and simulation of electronic assemblies, but faces a number of challenges to implementation. In this paper, a batch reflow oven with a large window was used to allow for optical measurements of an assembly under simulated production reflow conditions, and the results were compared to those from a finite element model. The testing and modeling methods are described, and their results are compared.

Keywords Digital image correlation • Reflow • Electronic packaging • Assembly • Thermo-mechanical stress

1.1 Introduction

Failures associated with thermal-mechanical stress are common in electronics assemblies. Digital image correlation (DIC) is an attractive displacement measurement technique for addressing these issues, but it cannot be used inside of production reflow ovens or thermal cycling chambers due to space and temperature constraints of the hardware. One solution is to acquire images in a windowed thermal chamber that is able to replicate the thermal conditions of reflow and thermal cycling. Such a solution presents many challenges to the ability to replicate the rapid temperature changes of reflow while collecting sufficiently high quality images of the assemblies.

Digital image correlation is an optical displacement measurement technique that is attractive for a number of reasons. In particular, it is a full-field, non-contact, two- or three-dimensional measurement method with good spatial sensitivity. The full-field nature can reveal high-strain regions that are sometimes unanticipated and might be missed by strain gages. The non-contact nature of DIC reduces setup time and decreases the chance of measurement interference with specimen behavior. The three dimensional capability yields more data than most other displacement techniques, and is especially attractive for both electronic assembly manufacturing and thermal cycling, since problems are often due to multiple thermal expansion mismatches resulting in complex displacements and warpage. The data lends itself well to qualitative and quantitative comparisons to finite element analysis for model validation [1, 2], and may also be used for traditional engineering analyses.

DIC has been used extensively with thermal chambers to measure strains resulting from thermal expansion mismatches, but published work is primarily on the sub-component level or under isothermal conditions [3–8]. Measurement of entire assemblies requires a relatively large thermal chamber, and heating and cooling capacities must be sufficiently large to match the temperature ramp rates of typical reflow ovens. Furthermore, the chamber must have an optical port that allows images to be taken with low enough optical distortion that three-dimensional displacements can be calculated over the entire assembly throughout the range of thermal conditions.

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This paper presents a series of tests used to verify and test an electronics assembly under under simulated reflow conditions. A commercially-available batch reflow oven was modified to provide a more uniform temperature distribution and to reduce optical distortions, and test methods were developed to further improve thermal and optical performance. An electronic assembly was run through a temperature profile in three configurations, and a finite element model of one of the configurations was constructed. Two parts of an electronic assembly were then run through a simulated reflow profile in the batch oven in order to measure the warpage of the solder pads during assembly.

1.2 Test Hardware and Test Methods

The tests were performed using a thermal chamber and a commercial DIC system. The thermal chamber was a modified Bokar X-Reflow 306 LF batch reflow oven, shown in Fig. 1.1. The DIC system was an Aramis 5 M (5 megapixel) system with 50 mm lenses. The thermal chamber was modified to improve temperature uniformity by replacing the supply air vents at either end of the sample stage with ducts that distribute the heated air more evenly across the stage in both the horizontal and vertical directions, and by adding side frames along the stage to conduct the heated air across the sample stage to return vents in the middle of the stage. Thermally-induced optical distortions between the window panes were effectively eliminated by decreasing the spacing between the panes, which prevented convective air circulation from setting up. The oven lid guide was also replaced with one that allowed the lid to be opened to 90° in order to allow the DIC system to be calibrated through the window. Circular polarizing filters were used on both the lenses and lights on the DIC system to reduce reflections and glare [9].

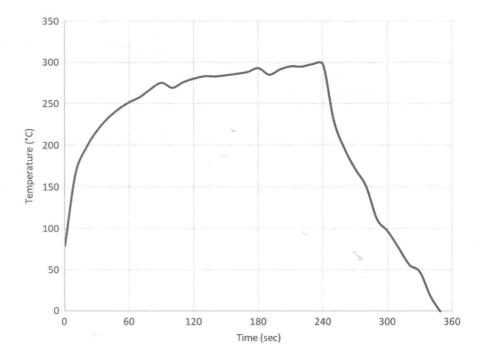
In addition to the hardware modifications, several test methods were employed. Continuous supply air circulation was used to induce constant turbulent air flow across the sample stage, breaking up thermally-induced optical distortions. Likewise, an external fan was used to induce turbulent air flow across the outside of the window in order to break up thermally-induced distortions arising from the outside of the heated glass. Specimens were suspended vertically at the mid-plane of the specimen stage to allow the supply air to flow evenly across the top and bottom surfaces.

The hardware provides heating rates that can replicate typical production reflow ovens. An example heating and cooling profile is shown in Fig. 1.2, showing heating of the specimen stage from room temperature to 300 °C in 5 min. In a typical scenario, the specimen would be heated to the solder reflow temperature in several stages over about 5 min.



Fig. 1.1 Bokar X-Reflow 306 LF batch reflow oven and DIC system

Fig. 1.2 Example heating and cooling profile



1.3 Low Rate Tests

In the first series of tests, warpage measurements were made during multiple temperature cycles on three specimen configurations. The purpose of the tests was to characterize the warpage of the specimens as a function of temperature. The first test configuration was a single overmolded package cycled to 220 °C five times. In the second configuration, the same overmolded package design was mounted to a daughter board, and two specimens were each cycled to 200 °C three times. The third configuration was similar to the second, except that the packages were underfilled, and two specimens were each cycled to 200 °C two times since no difference was observed between the second and third cycles in the first two configurations.

The specimens were speckled in the areas of interest, and were suspended above an aluminum holder with spring clips, as shown in Fig. 1.3. A thermocouple was attached to the underside of each specimen. For each test run the specimen was placed in the oven, the oven was heated to 5 °C above the target temperature, the specimen was heated until the thermocouple reached the target temperature, and then the heaters were turned off and the specimen was allowed to cool back down to room temperature (Fig. 1.4). The heating portion of each test required approximately 30 min, and each entire temperature cycle lasted about 2 h. DIC images were captured every 60 s during the tests. The coordinate system was set such that the x-y plane was coincident with three corners of the package. Rigid body motion was corrected for each image pair with a translation of a 6 degree of freedom best fit plane to that of the reference image at initial room temperature.

Warpage was defined as the displacement of the package center relative to the reference plane. In all tests the package warped downward when viewed from the overmolded side, so that the package center was lower than the corners as shown in Fig. 1.5. The warpage showed a difference between the heating and cooling legs as shown in Fig. 1.6. The difference between heating and cooling is most likely due to a temperature gradient in the package, and the response during the cooling phase is should more closely represent the isothermal behavior. The warpage of the package was -0.06 mm at initial and final room temperature, reached a maximum of -0.11 mm at 135 °C, and reached a minimum of -0.02 mm at 220 °C. The initial warpage before temperature cycling was -0.04 mm, which was different than the room temperature warpage after the first test and on subsequent tests, indicating that the difference is due to hysteresis in the materials that settles out after the first temperature cycle. An exception to this is that one of the non-underfilled specimens was cycled for third time approximately 3 days after the second cycle, and its warpage matched that of the first cycle.

The test results also showed significant part-to-part bias. When this bias was adjusted, the data yielded good repeatability. The warpage data for the non-underfilled tests are shown in the left-hand graph in Fig. 1.7, which shows significant scatter to the graph. When the final room temperature warpage is subtracted from the data and only the cool-down data are plotted, as in the right-hand graph of Fig. 1.7, the trends converge.

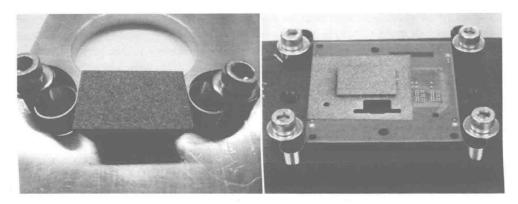


Fig. 1.3 Standalone (left) and mounted (right) test configurations

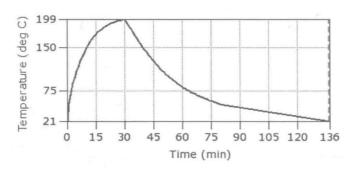


Fig. 1.4 Representative thermal cycle

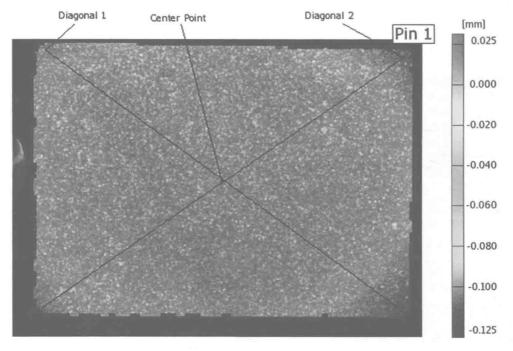


Fig. 1.5 Package warpage contour plot

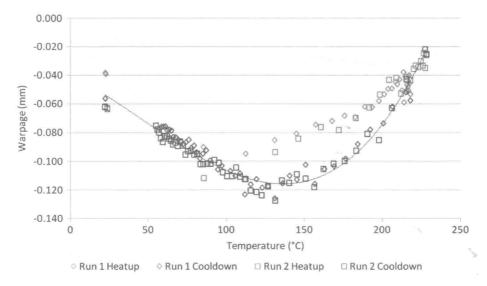


Fig. 1.6 Warpage of stand-alone package for first two cycles

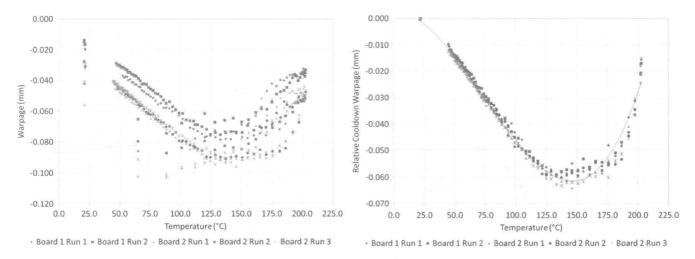


Fig. 1.7 Complete (left) and adjusted (right) warpage for non-underfilled tests

1.4 FEA Model Calibration and Validation

A FEA model was built to calculate the stresses within the package due to thermal-mechanical loading under its manufacturing and use conditions, and to optimize the design for reliability. The first step was to construct a model of the stand-alone module and validate it against the experimental measurements. This section describes the model and the method used for model calibration and validation with DIC data.

Figure 1.8 shows the mesh of the standalone module with and without the mold cap. Quadratic cubic and tetrahedral elements were used in order to avoid shear lock and accurately calculate the deformation. Since the temperature range of interest encompasses the glass transition temperature of the overmold epoxy, it is important to capture the time and temperature dependence of this material in the model. Viscoelastic material properties of the overmold epoxy was measured with DMA (Dynamic Mechanical Analysis) and used in the model. The cure shrinkage of the overmold epoxy was also included in the material model in order to capture the cross-linkage of the polymer at the cure temperature (175 C) of the epoxy. Typically the printed circuit board (PWB) can also exhibit some viscoelastic behaviors. However due to its relatively higher glass transition temperature, in this model the PWB is modeled as a transversely isotropic elastic material. The material properties that were used are listed in Table 1.1 and plotted in Fig. 1.9.

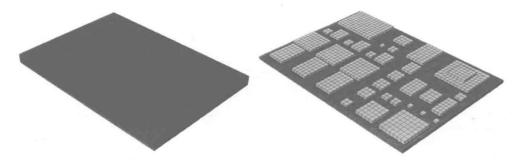


Fig. 1.8 Finite element mesh of the module package with and without the mold cap

Table 1.1 Material properties used in the FEA model

Material	Constitutive model
PWB	Transversely isotropic linear elastic
	In plane: $E = 30 \text{ GPa}$, $CTE = 11-14 \text{ ppm/}^{\circ}C$
Die Attach	Temperature dependent linear elastic
	Tg = 83 °C
	Above Tg, CTE = 151 ppm/°C
	Below Tg, CTE = 65 ppm/°C
Overmold epoxy	Viscoelastic, master curve see Fig. 1.5
	$Tg = 135 ^{\circ}C$
	Above Tg, CTE = 31 ppm/°C
	Below Tg, CTE = 7 ppm/°C
	Cure shrinkage, ~0.16 %
Die	Linear elastic, E = 131 GPa, CTE = 2.6 ppm/°C

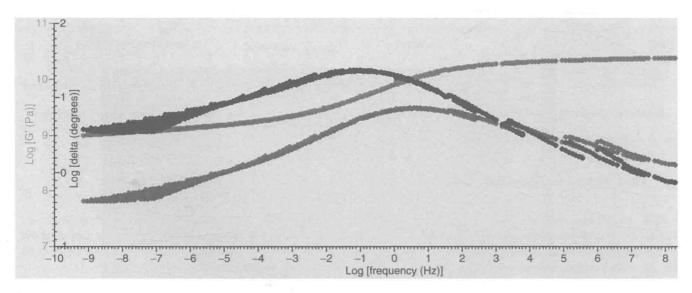


Fig. 1.9 Master curves of the overmold epoxy viscoelastic properties

In order to capture the initial warpage of the lab samples at room temperature prior to the DIC measurements, the thermal history of the manufacturing processes was considered in the model. Here the model assumes that at the time of overmolding of the package, the warpage of the module and all of its components is zero. Overmold epoxy cure and the subsequent cooling process were modeled to calculate the initial room temperature warpage. A subsequent step that used the same temperature history as the DIC tests was also included. Figure 1.10 shows the entire temperature history modeled.

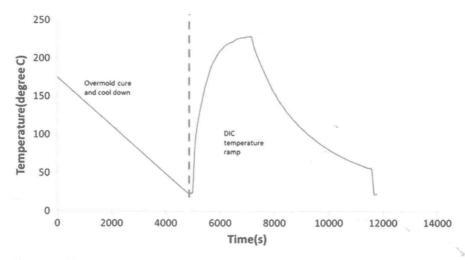


Fig. 1.10 Temperature history used in the FEA model

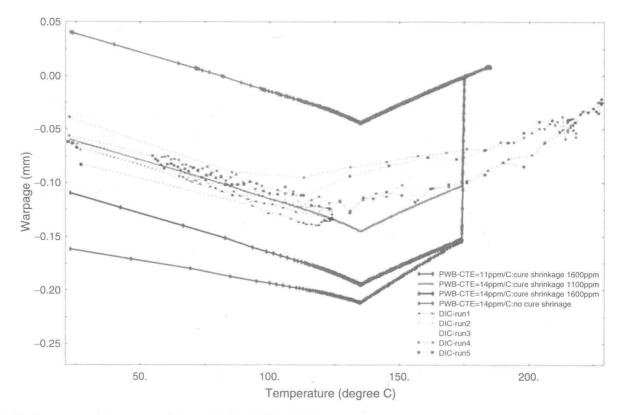


Fig. 1.11 Comparison of the warpage of the module from DIC and FEA

Several simulations with variations in the CTE of PWB and overmold cure shrinkage values were conducted and the results are compared to the DIC measurements (Fig. 1.11). First, all simulations were able to capture the change of warpage trend at around 135 °C. The change in the trend of the warpage-temperature curve is mainly due to the rapid change of the overmold epoxy material properties around its glass transition temperature, and the constitutive model of the overmold epoxy was able to reflect this change. Second, the stand-alone modules at room temperature prior to any DIC measurements have a warpage value around 0.06 mm; in simulation, this value was determined by two critical parts – the cure shrinkage amount of the overmold epoxy, and the relative thermal expansion mismatch of the overmold and the PWB during the cool down. The latter also determines the slopes of the warpage-temperature curve. By comparing the DIC data and the FEA simulation results, it is evident that the cure shrinkage needed to be included in order to correctly model the deformation of the package.

A final observation is that during the entire temperature history, the warpage results from FEA showed little time history dependency. In contrast the DIC data showed some hysteresis of the samples, with this effect more pronounced in the standalone modules and non-underfilled parts. This discrepancy could be caused by the neglecting the viscoelastic effect in other polymer materials such as PWB in the package, and needs to be further investigated.

1.5 Reflow Simulation Tests

In the second set of tests, the objective was to compare the displacements of pads on a circuit board to those of corresponding pads on a surface mount component. The air temperature profile of the production reflow oven was measured, and the batch reflow oven was programmed to provide a reasonable match, as shown in Fig. 1.7, with cool-down accelerated by opening the lid 30° and forcing ambient air across the stage. The circuit boards were composed of multiple daughter boards that were manufactured and assembled in one piece and singulated after assembly, and both bare and over-molded board configurations were tested. Each daughter board was speckled in the area of interest, a thermocouple was adhered to the board near the location of the surface mount component, and the boards were placed in their reflow carrier trays for testing. Three components were similarly prepared, except that they were placed upside down on a quartz stand so that the surface mount pads were facing the cameras. The DIC system was calibrated through the window. The specimens were run through the reflow profile and images were acquired at 10 s intervals during heating and 20 s intervals during cooling (Fig. 1.12).

Rigid body motion was corrected post-test, and out-of-plane displacement data were reduced for specific points on each pad. Example contour plots of the data are shown in Fig. 1.13. The test data yielded good part-to-part and test-to-test consistency. The warpage was modeled for the bare board configuration and the finite element and experimental results showed matching behavior.

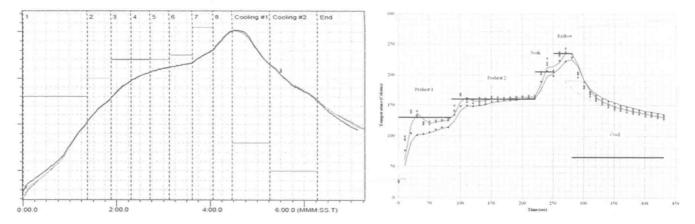


Fig. 1.12 Comparison of production (left) and test (right) temperature profiles

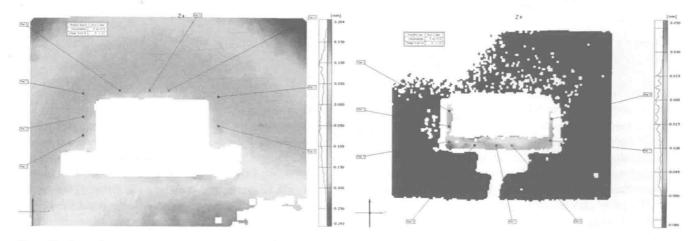


Fig. 1.13 Example contour plots of daughter board (left) and component (right)

1.6 Conclusions

A series of low heating rate tests was conducted on parts with three configurations. The results appear to show a heating rate effect, part-to-part variability, and a hysteresis between the first and second heating cycles. When adjusted for part-to-part bias and hysteresis, the results showed good repeatability.

A finite element model of the stand-alone configuration was constructed and compared to the experimental results. The model included the entire thermal history of assembly, cure shrinkage of the overmold epoxy, and the thermal expansion mismatches of the overmold and substrate. The model reflected the experimental results, including the warpage peak at about 140 °C, but did not show the hysteresis between the first and second temperature cycles.

A second series of tests was performed on a daughter board and a surface mount component under simulated reflow conditions. The test hardware was able to provide a reasonable match to the production reflow profile. The response of the thin daughter board matched modeled behavior. The test was used to quantify the warpage difference between board and component solder pads under simulated manufacturing conditions.

Acknowledgements Thanks to Wade Hezeltine at Intel Corporation's SMTD laboratory in Hillsboro, Oregon, for his idea to decrease the spacing of the window panes to reduce optical distortions.

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Chapter 2 Nanomechanical Characterization of Lead Free Solder Joints

Md Hasnine, Muhannad Mustafa, Jeffrey C. Suhling, Barton C. Prorok, Michael J. Bozack, and Pradeep Lall

Abstract The mechanical properties of a lead free solder are strongly influenced by its microstructure, which is controlled by its thermal history including solidification rate and thermal aging after solidification. In our ongoing research, we are exploring aging effects in lead free solder joints, and correlating the results to measured behavior from miniature bulk tensile samples. As a part of these efforts, the mechanical properties and creep behavior of lead free solders are being characterized by nano-mechanical testing of single SAC305 solder joints extracted from PBGA assemblies. Using nanoindentation techniques, the stress–strain and creep behavior of the SAC solder materials have been explored at the joint scale. Mechanical properties characterized included the elastic modulus, hardness, and yield stress. The test results show that the mechanical properties (modulus, hardness) of single grain SAC305 joints were dependent on the crystal orientation. Using a constant force at max indentation, the creep response of the solder joint materials has also been measured as a function of the applied stress level. An approach has been developed to estimate tensile creep strain rates for low stress levels using nanoindentation creep data measured at very high compressive stress levels.

Keywords Nanoindentation • Lead free solder • SAC alloy • Modulus • Hardness • Creep

2.1 Introduction

The ongoing transition to lead free soldering has been motivated by environmental concerns, legislative mandates, and market differentiation. Although no clear solution has been identified for all applications; Sn-Ag, Sn-Ag-Cu (SAC), and other alloys involving elements such as Sn, Ag, Cu, Bi, In, and Zn have been identified as potential replacements for standard 63Sn-37Pb eutectic solder. Several SAC alloys, such as 96.5Sn-3.0Ag-0.5Cu (SAC305), 95.5Sn-3.8Ag-0.7Cu (SAC387), 95.5Sn-3.9Ag-0.6Cu (SAC396) and 95.5Sn-4.0Ag-0.5Cu (SAC405), have been the proposed by various user groups and industry experts. For enhanced reliability of portable electronic devices during shock/drop loading (e.g. high strain rates), SAC alloys with low silver content have been recommended including 98.5Sn-1.0Ag-0.5Cu (SAC105). The main benefits of the various SAC alloy systems are their relatively low melting temperatures compared with the Sn-Ag binary eutectic alloy, as well as their higher strength, superior resistance to creep and thermal fatigue and solderability when compared to other lead free solders.

Solder joint fatigue is one of the predominant failure mechanisms in lead free electronic assemblies exposed to thermal cycling. Thus, accurate mechanical properties and constitutive equations for solder materials are needed for use in mechanical design, reliability assessment, and process optimization. Ma et al. [1] have reviewed the literature on the mechanical behavior of lead free solders. The mechanical properties of a lead free solder are strongly influenced by its microstructure, which is controlled by its thermal history including solidification rate and thermal aging after solidification. Due to aging phenomena, the microstructure, mechanical response, and failure behavior of lead free solder joints in electronic assemblies are constantly evolving when exposed to isothermal aging and/or thermal cycling environments.

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