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英文版

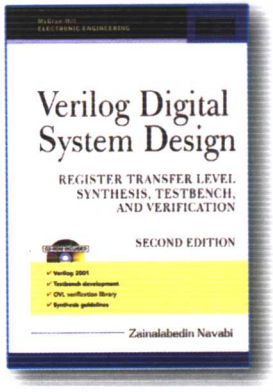
Verilog数字系统设计

——RTL综合、测试平台与验证

（第二版）

Verilog Digital System Design

Register Transfer Level Synthesis, Testbench, and Verification, Second Edition



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内容简介

本书主要讲述基于IEEE Std 1364–2001版本的Verilog硬件描述语言，着重讲述了使用Verilog进行数字系统的设计、验证及综合。根据数字集成电路设计的工程需求，本书重点关注了testbench的设计编写、验证和测试技术，深入讲述了基于Verilog HDL的开关级、门级、RTL级、行为级和系统级建模技术，从而使读者能尽快掌握硬件电路和系统的高效Verilog编程技术。书中把RTL描述、电路综合和testbench验证测试技术紧密结合，给出了多个从设计描述到验证的RTL数字电路模块和系统的设计实例。改编者在对标题、重点句子和段落进行注解时，在翻译的基础上针对较难理解的内容做了详细说明。

本书的设计与讲解由浅入深，既适合高年级本科生作为双语教学教材，也适合作为研究生第一年的双语课程教材。作为本科生和研究生数字系统设计和计算机组织结构的补充，本书也很有价值。

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序

2001年7月间，电子工业出版社的领导同志邀请各高校十几位通信领域方面的老师，商量引进国外教材问题。与会同志对出版社提出的计划十分赞同，大家认为，这对我国通信事业、特别是对高等院校通信学科的教学工作会很有好处。

教材建设是高校教学建设的主要内容之一。编写、出版一本好的教材，意味着开设了一门好的课程，甚至可能预示着一个崭新学科的诞生。20世纪40年代MIT林肯实验室出版的一套28本雷达丛书，对近代电子学科、特别是对雷达技术的推动作用，就是一个很好的例子。

我国领导部门对教材建设一直非常重视。20世纪80年代，在原教委教材编审委员会的领导下，汇集了高等院校几百位富有教学经验的专家，编写、出版了一大批教材；很多院校还根据学校的特点和需要，陆续编写了大量的讲义和参考书。这些教材对高校的教学工作发挥了极好的作用。近年来，随着教学改革不断深入和科学技术的飞速进步，有的教材内容已比较陈旧、落后，难以适应教学的要求，特别是在电子学和通信技术发展神速、可以讲是日新月异的今天，如何适应这种情况，更是一个必须认真考虑的问题。解决这个问题，除了依靠高校的老师和专家撰写新的符合要求的教科书外，引进和出版一些国外优秀电子与通信教材，尤其是有选择地引进一批英文原版教材，是会有好处的。

一年多来，电子工业出版社为此做了很多工作。他们成立了一个“国外电子与通信教材系列”项目组，选派了富有经验的业务骨干负责有关工作，收集了230余种通信教材和参考书的详细资料，调来了100余种原版教材样书，依靠由20余位专家组成的出版委员会，从中精选了40多种，内容丰富，覆盖了电路理论与应用、信号与系统、数字信号处理、微电子、通信系统、电磁场与微波等方面，既可作为通信专业本科生和研究生的教学用书，也可作为有关专业人员的参考材料。此外，这批教材，有的翻译为中文，还有部分教材直接影印出版，以供教师用英语直接授课。希望这些教材的引进和出版对高校通信教学和教材改革能起一定作用。

在这里，我还要感谢参加工作的各位教授、专家、老师与参加翻译、编辑和出版的同志们。各位专家认真负责、严谨细致、不辞辛劳、不怕琐碎和精益求精的态度，充分体现了中国教育工作者和出版工作者的良好美德。

随着我国经济建设的发展和科学技术的不断进步，对高校教学工作会不断提出新的要求和希望。我想，无论如何，要做好引进国外教材的工作，一定要联系我国的实际。教材和学术专著不同，既要注意科学性、学术性，也要重视可读性，要深入浅出，便于读者自学；引进的教材要适应高校教学改革的需要，针对目前一些教材内容较为陈旧的问题，有目的地引进一些先进的和正在发展中的交叉学科的参考书；要与国内出版的教材相配套，安排好出版英文原版教材和翻译教材的比例。我们努力使这套教材能尽量满足上述要求，希望它们能放在学生们的课桌上，发挥一定的作用。

最后，预祝“国外电子与通信教材系列”项目取得成功，为我国电子与通信教学和通信产业的发展培土施肥。也恳切希望读者能对这些书籍的不足之处、特别是翻译中存在的问题，提出意见和建议，以便再版时更正。

吴佑寿

中国工程院院士、清华大学教授

“国外电子与通信教材系列”出版委员会主任

出 版 说 明

进入21世纪以来，我国信息产业在生产和科研方面都大大加快了发展速度，并已成为国民经济发展的支柱产业之一。但是，与世界上其他信息产业发达的国家相比，我国在技术开发、教育培训等方面都还存在着较大的差距。特别是在加入WTO后的今天，我国信息产业面临着国外竞争对手的严峻挑战。

作为我国信息产业的专业科技出版社，我们始终关注着全球电子信息技术的发展方向，始终把引进国外优秀电子与通信信息技术教材和专业书籍放在我们工作的重要位置上。在2000年至2001年间，我社先后从世界著名出版公司引进出版了40余种教材，形成了一套“国外计算机科学教材系列”，在全国高校以及科研部门中受到了欢迎和好评，得到了计算机领域的广大教师与科研工作者的充分肯定。

引进和出版一些国外优秀电子与通信教材，尤其是有选择地引进一批英文原版教材，将有助于我国信息产业培养具有国际竞争能力的技术人才，也将有助于我国国内在电子与通信教学工作中掌握和跟踪国际发展水平。根据国内信息产业的现状、教育部《关于“十五”期间普通高等教育教材建设与改革的意见》的指示精神以及高等院校老师们反映的各种意见，我们决定引进“国外电子与通信教材系列”，并随后开展了大量准备工作。此次引进的国外电子与通信教材均来自国际著名出版商，其中影印教材约占一半。教材内容涉及的学科方向包括电路理论与应用、信号与系统、数字信号处理、微电子、通信系统、电磁场与微波等，其中既有本科专业课程教材，也有研究生课程教材，以适应不同院系、不同专业、不同层次的师生对教材的需求，广大师生可自由选择和自由组合使用。我们还将与国外出版商一起，陆续推出一些教材的教学支持资料，为授课教师提供帮助。

此外，“国外电子与通信教材系列”的引进和出版工作得到了教育部高等教育司的大力支持和帮助，其中的部分引进教材已通过“教育部高等学校电子信息科学与工程类专业教学指导委员会”的审核，并得到教育部高等教育司的批准，纳入了“教育部高等教育司推荐——国外优秀信息科学与技术系列教学用书”。

为做好该系列教材的翻译工作，我们聘请了清华大学、北京大学、北京邮电大学、南京邮电大学、东南大学、西安交通大学、天津大学、西安电子科技大学、电子科技大学、中山大学、哈尔滨工业大学、西南交通大学等著名高校的教授和骨干教师参与教材的翻译和审校工作。许多教授在国内电子与通信专业领域享有较高的声望，具有丰富的教学经验，他们的渊博学识从根本上保证了教材的翻译质量和专业学术方面的严格与准确。我们在此对他们的辛勤工作与贡献表示衷心的感谢。此外，对于编辑的选择，我们达到了专业对口；对于从英文原书中发现的错误，我们通过与作者联络、从网上下载勘误表等方式，逐一进行了修订；同时，我们对审校、排版、印制质量进行了严格把关。

今后，我们将进一步加强同各高校教师的密切关系，努力引进更多的国外优秀教材和教学参考书，为我国电子与通信教材达到世界先进水平而努力。由于我们对国内外电子与通信教育的发展仍存在一些认识上的不足，在选题、翻译、出版等方面的工作中还有许多需要改进的地方，恳请广大师生和读者提出批评及建议。

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Preface

This book is on the IEEE Standard Hardware Description Language based on the Verilog® Hardware Description Language (Verilog HDL), IEEE Std 1364-2001. The intended audiences are engineers involved in various aspects of digital systems design and manufacturing and students with the basic knowledge of digital system design. The emphasis of the book is on using Verilog HDL for the design, verification, and synthesis of digital systems. We will discuss Register Transfer (RT) level digital system design, and discuss how Verilog can be used in this design flow.

In the last few years RT level design of digital systems has gone through significant changes. Beyond simulation and synthesis that are now part of any RTL design process, we are looking at testbench generation and automatic verification tools. As with any book on Verilog, this book covers digital design and Verilog for simulation and synthesis. However, to ready design engineers for designing, testing, and verifying large digital system designs, the book contains material for testbench development and verification. The subjects of testbench and verification are introduced in Chapter 1. Chapter 2 onwards we concentrate on Verilog for design and synthesis. This will teach the readers efficient Verilog coding techniques for describing actual hardware components. When all of Verilog from a design point of view is presented, we turn our attention to test and verification. Chapter 6 covers testbench development techniques and use of assertion verification monitors for better analysis of a design. Toward the end of the book we put together our coding techniques for synthesis and testbench development, and present several RT level designs from design specification to verification.

Embedded in the presentation of the language, the book provides a review of digital system design and computer architecture concepts. This review is useful for relearning these concepts as demanded by new design methodologies and hardware description language based design tools. For practicing engineers the flow of the book, which starts from introductory material and advances into complex digital design concepts, provides a self-sufficient learning tool. The material is suitable for an upper division undergraduate or a first year graduate course. For a one-semester course on the Verilog HDL language and its use in a digital system design environment, the book can be used in its entirety. The book can also be used as a supplement for graduate and undergraduate digital system design and computer organization courses.

Overview of the Chapters

Chapter overviews are presented below. This material is intended to help a reader concentrate on parts of the book that he or she finds suit able to his or her needs best. Chapters 1 and 2 are introductory, and contain material with which many readers may already be familiar. It is, however, recommended that these chapters not be completely omitted, even by experienced readers. The Verilog language is

presented in Chapter 3 and includes the details of language syntax and semantics. The next two chapters (4 and 5) concentrate on Verilog for describing hardware from a design point of view. This is followed by a chapter on testing. Together, Chapters 4, 5, and 6 cover use of Verilog for design and test of digital systems. Chapter 7, which is on detailed modeling, is useful for VLSI designers. The last example in Chapter 8 is a complete processor that is modeled for synthesis and a complete testbench is developed for it.

Chapter 1 gives an overview of digital design process and the use of hardware description languages in this process. Simulation, synthesis, formal verification, and assertion verification are discussed in this chapter.

Chapter 2 shows various ways hardware components can be described in Verilog. The purpose of this chapter is to give the reader a general overview of the Verilog language.

Chapter 3 discusses the complete Verilog language structure. The focus of the chapter is more on the linguistic issues and not on modeling hardware components. A general understanding of the language is necessary before it can be used for hardware modeling. Writing Verilog for describing hardware is discussed in the chapters that follow this chapter.

Chapter 4 starts with gates and ends with high-level Verilog constructs for description of combinational circuits. Concurrency and timing will be discussed in the examples of this chapter. Except for specification of timing parameters, codes discussed in this chapter are synthesizable. A section in this chapter presents rules for writing synthesizable combinational circuits.

Chapter 5 discusses modeling and description of sequential circuits in Verilog. The chapter begins with models of memory and shows how they can be specified in Verilog. Registers, counters, and state machines are discussed in this chapter. A section in this chapter presents rules for writing synthesizable sequential circuits.

Chapter 6 is on writing testbenches in Verilog. The previous two chapters discussed Verilog from a hardware design point of view, and this chapter shows how components described as such can be tested. We talk about data generation, response analysis, and assertion verification.

Chapter 7 covers switch level modeling and detailed representation of signals in Verilog. This material is geared more for those using Verilog as a modeling language and less for designers. VLSI structures can be described by Verilog constructs discussed here.

Chapter 8 shows complete RTL design flow, from problem specification to test. We show several complete examples that take advantage of material of Chapters 4, 5, and 6 for description, simulation, verification, and synthesis of digital systems. Examples in this chapter take advantage of text IO facilities of Verilog for storing test data and circuit responses.

Appendix A contains Verilog keywords. Appendix B lists commonly used system tasks and briefly describes each task. Appendix C lists Verilog compiler directives and explains their use. Appendix D presents the standard IEEE Verilog HDL syntax. Language constructs terminals and nonterminals are presented here in a formal grammar representation. Appendix E presents the OVL assertion monitors. After a brief description of each assertion monitor its parameters and arguments are explained.

Suggested Reading Flow

The book teaches the Verilog language for RT level design, simulation, verification, and synthesis of digital systems. For a complete comprehension of these issues, or for a complete one-semester graduate course, the book is recommended in its entirety. However, for specific needs and requirements or for an undergraduate course on automated design methodologies, parts of the book can also be used. The following paragraphs present several such uses.

For a hardware designer interested in learning about synthesis, Chapters 4 and 5 are the most important ones. For such users, Chapter 3 can be used as a reference, and Chapter 6, which is on testbench development, can be studied as needed. When the designer is ready to consider complete systems, Chapter 8 is recommended.

Chapter 2 is introductory and provides an overview of the language. For a student using Verilog in a lower-level undergraduate course, this chapter is a good starting point for learning the language. More complex parts of the language can then be learned as needed.

Chapter 8 can be used for learning computer organization concepts and the use of Verilog in description of these structures. Readers familiar with Verilog can use their knowledge to learn the inter-workings of CPU structures, instruction execution, and testing large systems.

The flow of the book is such that it provides a complete knowledge of Verilog using the same flow as that used in teaching hardware design in most 4-year Computer Engineering programs. The following outlines indicate various applications of the book for beginners, undergraduate students, graduate students, designer engineers, modelers, and system designers.

1. General introduction for a lower-level undergraduate course or an entry level design engineer:
   - *Chapters 1-2.* Design flow and Verilog overview
   - *Chapters 4-5.* Combinational and sequential circuits for synthesis
2. Advanced logic design for a senior-level course or an advanced design engineer with some familiarity with design flow and Verilog syntax:
   - *Chapters 1-2.* A review of Verilog-based design
   - *Chapter 3.* Language semantics and constructs
   - *Chapters 4-5.* Combinational and sequential circuits for synthesis
   - *Chapter 6.* Test methods
3. Advanced system design for a senior-level course or an advanced system design engineer with some familiarity with design flow and Verilog syntax:
   - *Chapters 1-2.* A review of Verilog-based design
   - *Chapter 3.* Use as reference as needed
   - *Chapters 4-5.* Combinational and sequential circuits for synthesis
   - *Chapter 6.* Test methods
   - *Chapter 8.* Top-down design of systems
4. Advanced modeling and system design for a graduate-level course or an advanced VLSI design engineer:

- *Chapters 1-2.* A review of Verilog-based design
- *Chapter 3.* Use as reference as needed
- *Chapters 4-5.* Combinational and sequential circuits for synthesis
- *Chapter 6.* Test methods
- *Chapter 7.* Switch level and CMOS modeling
- *Chapter 8.* Top-down design of systems

5. Parallel with undergraduate Computer Engineering program:
   - Use Chapters 1 and 2 early in a digital logic design course
   - Use Chapters 4 and 5 in a digital logic design course in parallel with discussion of combinational and sequential circuits
   - Use Chapter 6 in a technical elective design course
   - Use Chapter 7 in the senior-level VLSI course
   - Use Chapter 8 in the Junior or Sophomore computer architecture course

Code Examples

Among many tasks involved in the preparation of the manuscript, for a book describing a language that is as example oriented as this book, selecting appropriate set of examples and presenting them to the reader are of special importance. For every design example presented in this book, a testbench is generated and the design has been tested. With every example, there is a logic design concept and there are several Verilog constructs and features that are covered. The set of examples is chosen to present the complete Verilog language for synthesis. These examples start with using simple Verilog constructs and progressively move into more complex ones. Parallel with the flow of language constructs, the book starts with using simple logic design concepts, such as using basic gates for combinational circuits, and moves into advanced logic design concepts such as queues and processors.

The CD accompanying this book includes simulation, synthesis, and device programming software tools. Verilog description of the examples of this book and their testbenches are also included on this CD. For the instructors using this book in an educational setting, solutions for the end of chapter problems and Power Point lecture slides can be obtained from the author or the publisher.

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