

VLSI Electronics Microstructure Science

Volume 9

Edited by

Norman G. Einspruch

VLSI Electronics Microstructure Science

Volume 9

Edited by

Norman G. Einspruch

**College of Engineering
University of Miami
Gables, Florida**

1985



ACADEMIC PRESS, INC.

(Harcourt Brace Jovanovich, Publishers)

**Orlando San Diego New York London
Toronto Montreal Sydney Tokyo**

COPYRIGHT © 1985, BY ACADEMIC PRESS, INC.
ALL RIGHTS RESERVED.
NO PART OF THIS PUBLICATION MAY BE REPRODUCED OR
TRANSMITTED IN ANY FORM OR BY ANY MEANS, ELECTRONIC
OR MECHANICAL, INCLUDING PHOTOCOPY, RECORDING, OR
ANY INFORMATION STORAGE AND RETRIEVAL SYSTEM, WITHOUT
PERMISSION IN WRITING FROM THE PUBLISHER.

ACADEMIC PRESS, INC.
Orlando, Florida 32887

United Kingdom Edition published by
ACADEMIC PRESS INC. (LONDON) LTD.
24-28 Oval Road, London NW1 7DX

Library of Congress Cataloging in Publication Data
(Revised for vol. 9)
Main entry under title:

VLSI electronics.

Vol. 6 has special title: Materials and process
characterization / edited by Norman G. Einspruch,
Graydon B. Larrabee.

Includes bibliographical references and indexes.

1. Integrated circuits—Very large scale integration.

I. Einspruch, Norman G.

TK7874.V56 621.381'73 81-2877

ISBN 0-12-234109-0 (v. 9 : alk. paper)

PRINTED IN THE UNITED STATES OF AMERICA

85 86 87 88

9 8 7 6 5 4 3 2 1

List of Contributors

Numbers in parentheses indicate the pages on which the authors' contributions begin.

- Gene Chao** (93), Metheus Corporation, Hillsboro, Oregon 97123
- T. P. Chow** (37), General Electric Company, Corporate Research and Development, Schenectady, New York 12345
- J. R. East** (441), Solid-State Electronics Laboratory and Department of Electrical and Computer Engineering, University of Michigan, Ann Arbor, Michigan 48104
- M. E. Elta** (441), Solid-State Electronics Laboratory and Department of Electrical and Computer Engineering, University of Michigan, Ann Arbor, Michigan 48104
- Eduardo B. Fernandez** (337), Department of Electrical and Computer Engineering, Florida Atlantic University, Boca Raton, Florida 33431
- D. K. Ferry** (421), Center for Solid State Electronics Research, Arizona State University, Tempe, Arizona 85287
- R. O. Grondin** (421), Center for Solid State Electronics, Arizona State University, Tempe, Arizona 85287
- G. I. Haddad** (441), Solid-State Electronics Laboratory and Department of Electrical and Computer Engineering, University of Michigan, Ann Arbor, Michigan 48109-1109
- K. Hess** (207), College of Engineering and Coordinated Science Laboratory, University of Illinois at Urbana-Champaign, Urbana, Illinois 61801
- J. S. T. Huang** (1), Honeywell, Inc., Corporate Solid State Laboratory, Plymouth, Minnesota 55441
- G. J. Iafrate** (207), U.S. Army Electronics Technology and Devices Laboratory, Fort Monmouth, New Jersey 07703
- Nobuo Kawamura** (385), NEC Corporation, Central Research Laboratories, Kawasaki, Japan
- Daniel E. Oates** (289), Lincoln Laboratory, Massachusetts Institute of Technology, Lexington, Massachusetts 02173

Yuji Okuto (385), NEC Corporation, Central Research Laboratories, Kawasaki, Japan

John M. Pankratz (185), Texas Instruments Incorporated, Dallas, Texas 75265

Allan Rosencwaig (227), Therma-Wave, Inc., Fremont, California 94539

Walter H. Schroen (185), Texas Instruments Incorporated, Dallas, Texas 75265

Neil C. Sher (367), Commercial Buildings Group, Honeywell, Inc., Minneapolis, Minnesota 55408

A. J. Steckl (37), Rensselaer Polytechnic Institute, Center for Integrated Electronics, Troy, New York 12181

Graham Tubbs (149), Intel Corporation, Chandler, Arizona 85224

Michiyuki Uenohara (385), NEC Corporation, Central Research Laboratories, Kawasaki, Japan

William Weir (93), Metheus Corporation, Hillsboro, Oregon 97123

Preface

Civilization has passed the threshold of the second industrial revolution. The first industrial revolution, which was based upon the steam engine, enabled man to multiply his physical capabilities to do work. The second industrial revolution, which is based upon semiconductor electronics, is enabling man to multiply his intellectual capabilities. VLSI (Very Large Scale Integration) electronics, the most advanced state of semiconductor electronics, represents a remarkable application of scientific knowledge to the requirements of technology. This treatise is published in recognition of the need for a comprehensive exposition that describes the state of this science and technology and that assesses trends for the future of VLSI electronics and the scientific base that supports its development.

These volumes are addressed to scientists and engineers who wish to become familiar with this rapidly developing field, basic researchers interested in the physics and chemistry of materials and processes, device designers concerned with the fundamental character of and limitations to device performance, systems architects who will be charged with tying VLSI circuits together, and engineers concerned with utilization of VLSI circuits in specific areas of application.

This treatise includes subjects that range from microscopic aspects of materials behavior and device performance — through the technologies that are incorporated in the fabrication of VLSI circuits — to the comprehension of VLSI in systems applications.

The volumes are organized as a coherent series of stand-alone chapters, each prepared by a recognized authority. The chapters are written so that specific topics of interest can be read and digested without regard to chapters that appear elsewhere in the sequence.

There is a general concern that the base of science that underlies integrated circuit technology has been depleted to a considerable extent and is in need of revitalization; this issue is addressed in the National Research Council

(National Academy of Sciences/National Academy of Engineering) report entitled "Microstructure Science, Engineering and Technology." It is hoped that this treatise will provide background and stimulus for further work on the physics and chemistry of structures that have dimensions that lie in the submicrometer domain and the use of these structures in serving the needs of humankind.

Contents

List of Contributors	ix
Preface	xi
Chapter 1 MOS/Bipolar Technology Trade-Offs for VLSI	
J. S. T. Huang	
I. Introduction	2
II. Fundamental Scaling Principles	3
III. Technology Comparison and Trade-Offs	9
IV. Comparison with Other Devices	22
V. Technology Issues and Trends	26
VI. Conclusions	32
Appendix. Derivation of Conventional Long-Channel MOS Theory	33
References	34
Chapter 2 A Critique of Refractory Gate Applications for MOS VLSI	
T. P. Chow and A. J. Steckl	
I. Introduction	38
II. Motivation and Requirements	39
III. Gate Structures	42
IV. Processing Issues	54
V. Devices and Circuits	77
VI. Conclusions and Future Trends	84
References	85
Chapter 3 VLSI Design Tools and Environments	
Gene Chao and William Weir	
I. Introduction	94
II. Strategies for VLSI System Design	96
III. VLSI Design Tools	110
IV. VLSI Design Environments	127
V. Trends and Emerging Issues	138
References	141

Chapter 4 VLSI Standard Part Manufacturer as a Full-Service Vendor

Graham Tubbs

I.	Introduction	150
II.	The Custom Design Arena	150
III.	The Customer-Vendor Interface	160
IV.	The Question of Testability	176
V.	Trends in the Customer-Vendor Relationship	182
	References	184

Chapter 5 VLSIC Assembly and Packaging

Walter H. Schroen and John M. Pankratz

I.	Introduction	185
II.	Chip Mounting	188
III.	Bonding	190
IV.	Packaging	192
V.	Package Mounting	202
VI.	Automation and Cost Reduction	204
	References	204

Chapter 6 High-Speed Transport in Ultrasmall Dimensions

G. J. Iafrate and K. Hess

I.	Introduction	207
II.	Semiclassical Theory of Transient Conduction and Numerical Results	212
III.	Analytical Considerations	220
IV.	Velocity Overshoot in Semiconductor Devices	223
	References	225

Chapter 7 Applications of Thermal-Wave Physics to Microelectronics

Allan Rosencwaig

I.	Introduction	227
II.	Theory	228
III.	Thermal-Wave Imaging	248
IV.	Applications	255
V.	Measurement of Thin-Film Thickness	277
VI.	Conclusions	285
	References	286

Chapter 8 Surface Acoustic Wave Devices**Daniel E. Oates**

I. Introduction	290
II. Fundamentals of SAW	292
III. Fabrication Methods for SAW Devices	306
IV. Band-Pass Filters and Resonators	309
V. Signal-Processing Devices	319
VI. Conclusions and Future Trends	333
References	334

Chapter 9 VLSI and Single-Chip Software-Oriented Computer Architecture**Eduardo B. Fernandez**

I. Introduction	338
II. Reduced Instruction Set Architectures	341
III. Extended Von Neumann Architectures	345
IV. Harvard Architectures	351
V. Ring Architectures	353
VI. Stack Architectures	355
VII. Directly Executed Language Architectures	356
VIII. Object-Oriented Architectures	357
IX. High-Level-Language Machines	359
X. Architectural Evaluation	360
XI. The Future	362
References	363

Chapter 10 Microelectronics for the Intelligent Building**Neil C. Sher**

I. Nonresidential Building Functions	368
II. Building Systems	369
III. Impact of Future Microelectronics Developments	377
IV. Overall Expectations	383

Chapter 11 The Next Generation of Integrated Circuits — What Comes after VLSI?**Michiyuki Uenohara, Nobuo Kawamura, and Yuji Okuto**

I. Social Background for VLSI Development and Beyond	386
II. Limits of VLSI Technology	389
III. Challenge to Technical Barriers	405
IV. Trend of Integrated Circuits toward and beyond the Twenty-First Century	415
References	418

Chapter 12 Transport in Submicrometer Devices**D. K. Ferry and R. O. Grondin**

I.	Introduction	421
II.	High-Field Transport	425
III.	Transient Dynamic Response	427
IV.	Velocity in Devices	431
V.	Noise and Diffusion	435
VI.	Conclusions	438
	References	439

Chapter 13 Fabrication and Performance of Very High-Frequency Devices**J. R. East, M. E. Elta, and G. I. Haddad**

I.	Introduction	441
II.	Three-Terminal Device Fabrication and Performance	442
III.	Two-Terminal Device Fabrication and Performance	451
	References	453

Index	455
--------------	------------

Contents of Other Volumes	471
----------------------------------	------------

Chapter 1

MOS/Bipolar Technology Trade-Offs for VLSI

J. S. T. HUANG

Honeywell, Inc.
Corporate Solid State Laboratory
Minneapolis, Minnesota

I.	Introduction	2
A.	Historical Background	2
B.	Scope	2
C.	Charge Control Approach	2
II.	Fundamental Scaling Principles	3
A.	Device Scaling	3
B.	Interconnect Scaling	7
III.	Technology Comparison and Trade-Offs	9
A.	Intrinsic Speed	9
B.	Intrinsic Device Model	10
C.	Circuit Delay	19
IV.	Comparison with Other Devices	22
V.	Technology Issues and Trends	26
A.	General Issues	26
B.	Bipolar Limitations	27
C.	MOS Limitations	29
D.	Application Trends	32
VI.	Conclusions	32
Appendix.	Derivation of Conventional Long-Channel MOS Theory	33
	References	34

I. INTRODUCTION

A. Historical Background

Bipolar transistors are traditionally known to have high switching speed but low integration density, chiefly because of their high power consumption. New bipolar circuit techniques such as I²L and ISL represent attempts by bipolar technologists to achieve higher integration densities. On the other hand, the metal-oxide-semiconductor (MOS) technology with its low power dissipation was intended at the outset for a high level of integration while sacrificing switching speed. Over the last decade, great strides have been made to improve the speed performance of MOS transistors by gradually shrinking the device geometry toward submicrometer dimensions. More recently, complementary MOS (CMOS) has become the more dominant MOS technology for VLSI, since its speed is comparable to *n*-channel MOS (NMOS), but dissipates much less power.

Ever since the inception of integrated circuits, the battle between bipolar and MOS technologies to gain dominance in integrated circuit applications has continued unabated. The inexorable trend toward VLSI suggests the need for continuous assessing and comparing the prospect of bipolar and MOS technologies. It is to this end that the present work is directed.

B. Scope

We shall restrict our discussion in this work to the silicon-based technology of which MOS and bipolar are the main generic technologies. Such devices as JFET, MESFET, static injection transistor (SIT) [1], and permeable base transistor (PBT) [2] are considered offshoots of either bipolar or MOS device and will be compared briefly. It turns out that the approach that we adopted can be applied equally to devices made with semiconducting materials other than Si. We are primarily concerned with device and circuit properties in terms of performance, power, and density and their impact on integrated circuit applications. Circuit fabrication techniques that give rise to the desired feature size are beyond the scope of this work.

C. Charge Control Approach

Normally, MOSFETs are considered to be voltage-controlled devices and bipolar transistors are considered to be current-controlled devices. Both can also be viewed as charge-controlled devices. Our approach is based on this

elementary charge-control concept whereby considerable physical insight into device performance can be gained at the expense of mathematical rigor. We will stress similarities as well as differences among various devices. Only through this comparison can technology trends be perceived.

According to the charge-control model, the current I is related to the charge Q by

$$I = Q/\tau, \quad (1)$$

where τ is the charge transit time between an emitting electrode and a collecting electrode. Equation (1) simply states that a charge Q is swept into a collecting electrode during each period τ . This movement of charge constitutes the current flow. The reciprocal of τ is defined as the intrinsic gain-bandwidth product f_T of the device.

The voltage buildup due to the charge flowing into a capacitor C is

$$V = Q/C. \quad (2)$$

Combining Eqs. (1) and (2) gives

$$\tau = CV/I = C/g_m, \quad (3)$$

where

$$g_m = I/V \quad (4)$$

is defined as the transconductance. Equation (3) lends itself to easy physical interpretation; that is, the delay time is the time taken to charge a capacitance C by a constant current I to the voltage level V . In general, the transconductance, the capacitance, and the transit time are indexes of performance for practically all semiconductor devices.

Equations (1)–(4) are large-signal parameters that are particularly relevant to switching circuits. Since relationships between physical quantities are often nonlinear, small-signal parameters can be defined as derivatives of large-signal quantities. Since the large-signal parameter is usually proportional to the small-signal parameter, the fact that we shall make no distinction between them will not prevent us from reaching valid conclusions.

II. FUNDAMENTAL SCALING PRINCIPLES

A. Device Scaling

Figure 1 shows the horizontal geometries of a bipolar transistor, an MOS transistor, and the cross section of an interconnect line delineating the di-

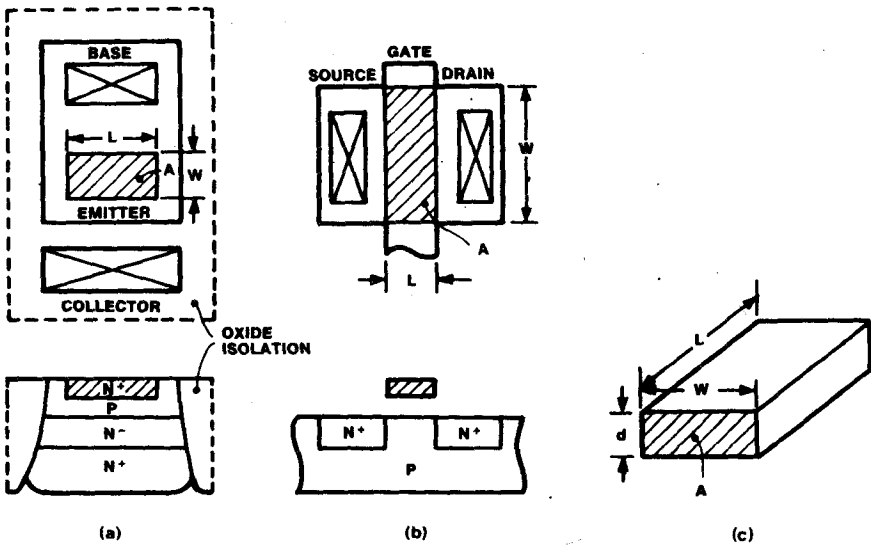


Fig. 1. (a) Top and edge views of a bipolar transistor, (b) a MOS transistor, and (c) an interconnect line.

mensions to be scaled. Table I lists one type of scaling relationship for bipolar and MOS transistors where S is a dimensionless scaling parameter greater than unity. The performance and power characteristics resulting from scaling are summarized in Table II. Not surprisingly, the speed improvement in a scaled-down MOSFET is more readily attainable than in a scaled-down bipolar transistor, since the gain and the bandwidth of a MOS device depend on the horizontal geometry, whereas those of a bipolar device depend on the vertical dimension (e.g., the basewidth, which is already near

TABLE I
Scaling Relationships

Device parameter	Bipolar ^a	MOS ^b
Device dimension L, W, d	$1/S$	$1/S$
Doping concentration N	1	S
Oxide thickness X_0	$1/S$	$1/S$
Junction depth X_j	$1/S$	$1/S$
Voltage V	1	$1/S$
Current I	$1/S^2$	$1/S$
Capacitance C	$1/S^2$	$1/S$

^a After Huang [4].

^b After Dennard *et al.* [3].

TABLE II
Speed and Power Comparison

Parameter	Bipolar	MOS
Delay time $\tau = C \Delta V / I$	1	$1/S$
Power = VI	$1/S^2$	$1/S^2$
Power density = VI/A	1	1
Speed \times power = $VI\tau$	$1/S^2$	$1/S^3$

minimum). However, with reduced voltage swing, narrower basewidth, and smaller parasitics, the delay of a bipolar transistor is decreased somewhat, but certainly not as drastically as in the MOS transistor.

Notice that for both technologies, the gate power is reduced by S^2 and the gate power density remains constant, implying that the circuit-cooling problem remains unchanged. Because of the greater speed improvement in MOS, the speed power product is decreased by S^3 as compared to only S^2 improvement for bipolar. Table III compares present and projected properties of MOS and bipolar current mode logic (CML) circuits as the minimum linewidth decreases from $3 \mu\text{m}$ toward the submicrometer region. The speed versus power is plotted in Fig. 2, showing the trend of speed power product moving toward 10^{-15}-J range.

As seen from Table III, the speed of the bipolar CML circuits is obtained at the expense of high power. The speed of NMOS and CMOS is comparable, but CMOS dissipates about one order of magnitude less power than NMOS. Hence, CMOS is increasingly being used in power-critical circuits. It should

TABLE III
Present and Projected Characteristics

Technology (min. linewidth, μm)	Gate size (mil ²)	Delay (nsec)	Power/gate (mW)
CML (high-speed bipolar)			
3.0	12.0	0.5	1.2
1.5	4.0	0.4	0.3
0.75	1.0	0.3	0.1
NMOS			
3.0	2.4	2.0	0.3
1.5	0.6	1.0	0.1
0.75	0.2	0.5	0.05
CMOS			
3.0	4.0	2.0	0.06/10 MHz
1.5	1.0	1.0	0.02/10 MHz
0.75	0.25	0.5	0.01/10 MHz

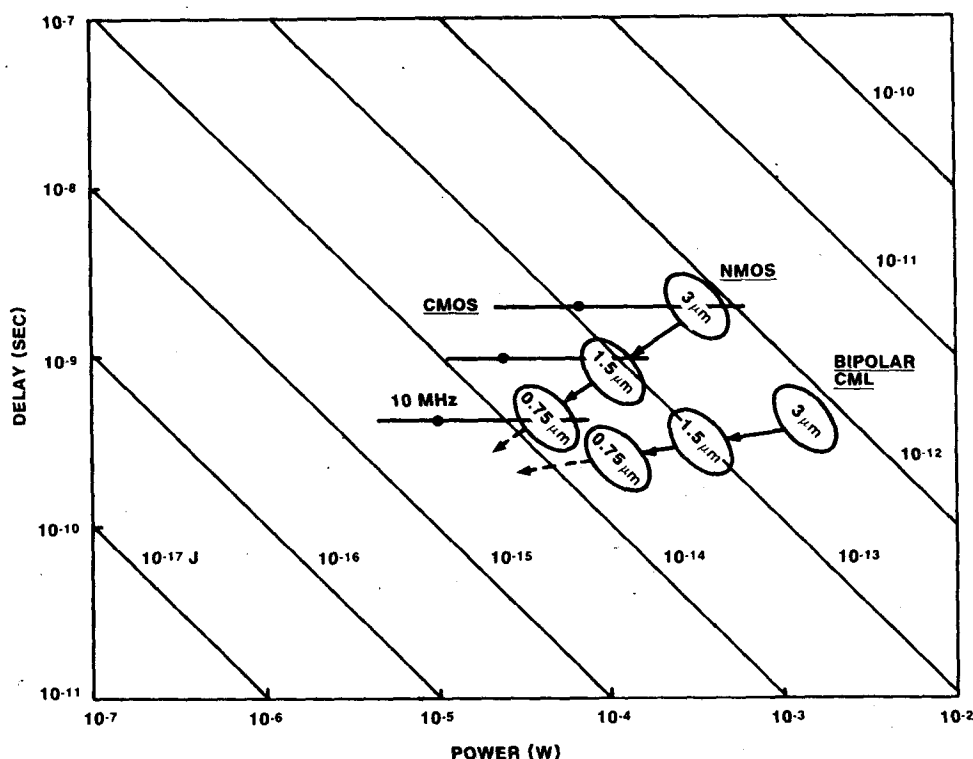


Fig. 2. Speed-versus-power plot of emerging technology.

be noted that CMOS dissipates power only during the switching period τ , when the logic state is changing. It is the average power (i.e., $\bar{P} = CV^2f$) that is given in Table III. The average power is proportional to the switching frequency f . Therefore, in the speed power plot of Fig. 2, CMOS characteristics appear as horizontal lines, indicating that for a given gate delay the power increases with frequency of operation. A more useful figure of merit for CMOS is the peak power delay product given by

$$\hat{P}\tau = \bar{P}/f = CV^2, \quad (5)$$

which is simply the energy required to switch the logic state.

Although the straightforward scaling rules given in Table I do indicate trends for future technology development, it is not the only scaling approach. In order to reduce further the basewidth for bipolar transistors, the base doping will have to be increased to avoid punchthrough and to maintain or reduce the base resistance R_B . As a result, the depletion layer capacitance C_d is decreased by less than S^2 . The depletion capacitance charging time,