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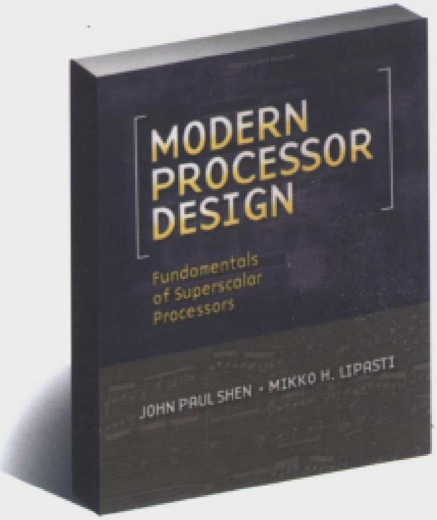
MODERN PROCESSOR DESIGN

FUNDAMENTALS OF SUPERSCALAR PROCESSORS

现代处理器设计

John P. Shen Mikko Lipasti 著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JOHN PAUL SHEN · MIKKO H. LIPASTI

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清华大学出版社

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内容简介

本书是关于处理器设计的最新、最权威教材，主要论述了：(1)处理器的设计方法和原理；(2)流水线技术；(3)主存与I/O系统；(4)超标量组织与技术；(5)PowerPC 620和Intel P6等示例；(6)超标量处理器设计；(7)先进的指令流技术、存储器数据流技术；(8)多线程技术等。

本书适合作为计算机及相关专业的“处理器设计”课程的教材，也是有关专业人员很有价值的参考用书。

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出 版 说 明

进入 21 世纪，世界各国的经济、科技以及综合国力的竞争将更加激烈。竞争的中心无疑是对人才的竞争。谁拥有大量高素质的人才，谁就能在竞争中取得优势。高等教育，作为培养高素质人才的事业，必然受到高度重视。目前我国高等教育的教材更新较慢，为了加快教材的更新频率，教育部正在大力促进我国高校采用国外原版教材。

清华大学出版社从 1996 年开始，与国外著名出版公司合作，影印出版了“大学计算机教育丛书（影印版）”等一系列引进图书，受到国内读者的欢迎和支持。跨入 21 世纪，我们本着为我国高等教育教材建设服务的初衷，在已有的基础上，进一步扩大选题内容，改变图书开本尺寸，一如既往地请有关专家挑选适用于我国高校本科及研究生计算机教育的国外经典教材或著名教材，组成本套“大学计算机教育国外著名教材系列（影印版）”，以飨读者。深切期盼读者及时将使用本系列教材的效果和意见反馈给我们。更希望国内专家、教授积极向我们推荐国外计算机教育的优秀教材，以利我们把“大学计算机教育国外著名教材系列（影印版）”做得更好，更适合高校师生的需要。

清华大学出版社

John Paul Shen

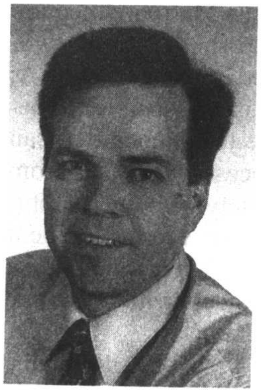
John Paul Shen is the Director of Intel's Microarchitecture Research Lab (MRL), providing leadership to about two-dozen highly skilled researchers located in Santa Clara, CA; Hillsboro, OR; and Austin, TX. MRL is responsible for developing innovative microarchitecture techniques that can potentially be used in future microprocessor products from Intel. MRL researchers collaborate closely with microarchitects from product teams in joint advanced-development efforts. MRL frequently hosts visiting faculty and Ph.D. interns and conducts joint research projects with academic research groups.

Prior to joining Intel in 2000, John was a professor in the electrical and computer engineering department of Carnegie Mellon University, where he headed up the CMU Microarchitecture Research Team (CMuART). He has supervised a total of 16 Ph.D. students during his years at CMU. Seven are currently with Intel, and five have faculty positions in academia. He won multiple teaching awards at CMU. He was an NSF Presidential Young Investigator. He is an IEEE Fellow and has served on the program committees of ISCA, MICRO, HPCA, ASPLOS, PACT, ICCD, ITC, and FTCS.

He has published over 100 research papers in diverse areas, including fault-tolerant computing, built-in self-test, process defect and fault analysis, concurrent error detection, application-specific processors, performance evaluation, compilation for instruction-level parallelism, value locality and prediction, analytical modeling of superscalar processors, systematic microarchitecture test generation, performance simulator validation, precomputation-based prefetching, database workload analysis, and user-level helper threads.

John received his M.S. and Ph.D. degrees from the University of Southern California, and his B.S. degree from the University of Michigan, all in electrical engineering. He attended Kimball High School in Royal Oak, Michigan. He is happily married and has three daughters. His family enjoys camping, road trips, and reading *The Lord of the Rings*.

Mikko Lipasti



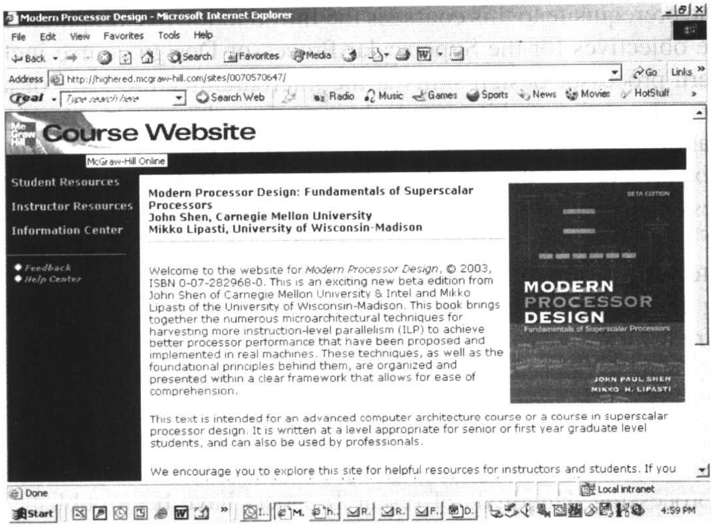
Mikko Lipasti has been an assistant professor at the University of Wisconsin-Madison since 1999, where he is actively pursuing various research topics in the realms of processor, system, and memory architecture. He has advised a total of 17 graduate students, including two completed Ph.D. theses and numerous M.S. projects, and has published more than 30 papers in top computer architecture conferences and journals. He is most well known for his seminal Ph.D. work in value prediction. His research program has received in excess of $2 million in support through multiple grants from the National Science Foundation as well as financial support and equipment donations from IBM, Intel, AMD, and Sun Microsystems.

The Eta Kappa Nu Electrical Engineering Honor Society selected Mikko as the country's Outstanding Young Electrical Engineer for 2002. He is also a member of the IEEE and the Tau Beta Pi engineering honor society. He received his B.S. in computer engineering from Valparaiso University in 1991, and M.S. (1992) and Ph.D. (1997) degrees in electrical and computer engineering from Carnegie Mellon University. Prior to beginning his academic career, he worked for IBM Corporation in both software and future processor and system performance analysis and design guidance, as well as operating system kernel implementation. While at IBM he contributed to system and microarchitectural definition of future IBM server computer systems. He has served on numerous conference and workshop program committees and is co-organizer of the annual Workshop on Duplicating, Deconstructing, and Debunking (WDDD). He has filed seven patent applications, six of which are issued U.S. patents; won the Best Paper Award at MICRO-29; and has received IBM Invention Achievement, Patent Issuance, and Technical Recognition Awards.

Mikko has been happily married since 1991 and has a nine-year-old daughter and a six-year old son. In his spare time, he enjoys regular exercise, family bike rides, reading, and volunteering his time at his local church and on campus as an English-language discussion group leader at the International Friendship Center.

Additional Resources

In addition to the comprehensive coverage within the book, a number of additional resources are available with Shen/Lipasti's MODERN PROCESSOR DESIGN through the book's website at **www.mhhe.com/shen**.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Modern Processor Design: Fundamentals of Superscalar Processors
John Shen, Carnegie Mellon University
Mikko Lipasti, University of Wisconsin-Madison

Welcome to the website for *Modern Processor Design*, © 2003, ISBN 0-07-282968-0. This is an exciting new beta edition from John Shen of Carnegie Mellon University & Intel and Mikko Lipasti of the University of Wisconsin-Madison. This book brings together the numerous microarchitectural techniques for harvesting more instruction-level parallelism (ILP) to achieve better processor performance that have been proposed and implemented in real machines. These techniques, as well as the foundational principles behind them, are organized and presented within a clear framework that allows for ease of comprehension.

This text is intended for an advanced computer architecture course or a course in superscalar processor design. It is written at a level appropriate for senior or first year graduate level students, and can also be used by professionals.

We encourage you to explore this site for helpful resources for instructors and students. If you

Instructor Resources

- **Solutions Manual**—A complete set of solutions for the chapter-ending homework problems are provided.
- **PowerPoint Slides**—Two sets of MS PowerPoint slides, from Carnegie Mellon University and the University of Wisconsin-Madison, can be downloaded to supplement your lecture presentations.
- **Figures**—A complete set of figures from the book are available in eps format. These figures can be used to create your own presentations.
- **Sample Homework Files**—A set of homework assignments with answers from Carnegie Mellon University are provided to supplement your own assignments.
- **Sample Exams**—A set of exams with answers from Carnegie Mellon University are also provided to supplement your own exams.
- **Links to www.simplescalar.com**—We provide several links to the SimpleScalar tool set, which are available free for non-commercial academic use.

Preface

This book emerged from the course *Superscalar Processor Design,* which has been taught at Carnegie Mellon University since 1995. Superscalar Processor Design is a mezzanine course targeting seniors and first-year graduate students. Quite a few of the more aggressive juniors have taken the course in the spring semester of their junior year. The prerequisite to this course is the Introduction to Computer Architecture course. The objectives for the Superscalar Processor Design course include: (1) to teach modern processor design skills at the microarchitecture level of abstraction; (2) to cover current microarchitecture techniques for achieving high performance via the exploitation of instruction-level parallelism (ILP); and (3) to impart insights and hands-on experience for the effective design of contemporary high-performance microprocessors for mobile, desktop, and server markets. In addition to covering the contents of this book, the course contains a project component that involves the microarchitectural design of a future-generation superscalar microprocessor.

During the decade of the 1990s many microarchitectural techniques for increasing clock frequency and harvesting more ILP to achieve better processor performance have been proposed and implemented in real machines. This book is an attempt to codify this large body of knowledge in a systematic way. These techniques include deep pipelining, aggressive branch prediction, dynamic register renaming, multiple instruction dispatching and issuing, out-of-order execution, and speculative load/store processing. Hundreds of research papers have been published since the early 1990s, and many of the research ideas have become reality in commercial superscalar microprocessors. In this book, the numerous techniques are organized and presented within a clear framework that facilitates ease of comprehension. The foundational principles that underlie the plethora of techniques are highlighted.

While the contents of this book would generally be viewed as graduate-level material, the book is intentionally written in a way that would be very accessible to undergraduate students. Significant effort has been spent in making seemingly complex techniques to appear as quite straightforward through appropriate abstraction and hiding of details. The priority is to convey clearly the key concepts and fundamental principles, giving just enough details to ensure understanding of implementation issues without massive dumping of information and quantitative data. The hope is that this body of knowledge can become widely possessed by not just microarchitects and processor designers but by most B.S. and M.S. students with interests in computer systems and microprocessor design.

Here is a brief summary of the chapters.

Chapter 1: Processor Design

This chapter introduces the art of processor design, the instruction set architecture (ISA) as the specification of the processor, and the microarchitecture as the implementation of the processor. The dynamic/static interface that separates compile-time software and run-time hardware is defined and discussed. The goal of this chapter is not to revisit in depth the traditional issues regarding ISA design, but to erect the proper framework for understanding modern processor design.

Chapter 2: Pipelined Processors

This chapter focuses on the concept of pipelining, discusses instruction pipeline design, and presents the performance benefits of pipelining. Pipelining is usually introduced in the first computer architecture course. Pipelining provides the foundation for modern superscalar techniques and is presented in this chapter in a fresh and unique way. We intentionally avoid the massive dumping of bar charts and graphs; instead, we focus on distilling the foundational principles of instruction pipelining.

Chapter 3: Memory and I/O Systems

This chapter provides a larger context for the remainder of the book by including a thorough grounding in the principles and mechanisms of modern memory and I/O systems. Topics covered include memory hierarchies, caching, main memory design, virtual memory architecture, common input/output devices, processor-I/O interaction, and bus design and organization.

Chapter 4: Superscalar Organization

This chapter introduces the main concepts and the overall organization of superscalar processors. It provides a "big picture" view for the reader that leads smoothly into the detailed discussions in the next chapters on specific superscalar techniques for achieving performance. This chapter highlights only the key features of superscalar processor organizations. Chapter 7 provides a detailed survey of features found in real machines.

Chapter 5: Superscalar Techniques

This chapter is the heart of this book and presents all the major microarchitecture techniques for designing contemporary superscalar processors for achieving high performance. It classifies and presents specific techniques for enhancing instruction flow, register data flow, and memory data flow. This chapter attempts to organize a plethora of techniques into a systematic framework that facilitates ease of comprehension.

Chapter 6: The PowerPC 620

This chapter presents a detailed analysis of the PowerPC 620 microarchitecture and uses it as a case study to examine many of the issues and design tradeoffs introduced in the previous chapters. This chapter contains extensive performance data of an aggressive out-of-order design.

Chapter 7: Intel's P6 Microarchitecture

This is a case study chapter on probably the most commercially successful contemporary superscalar microarchitecture. It is written by the Intel P6 design team led by Bob Colwell and presents in depth the P6 microarchitecture that facilitated the implementation of the Pentium Pro, Pentium II, and Pentium III microprocessors. This chapter offers the readers an opportunity to peek into the mindset of a top-notch design team.

Chapter 8: Survey of Superscalar Processors

This chapter, compiled by Prof. Mark Smotherman of Clemson University, provides a historical chronicle on the development of superscalar machines and a survey of existing superscalar microprocessors. The chapter was first completed in 1998 and has been continuously revised and updated since then. It contains fascinating information that can't be found elsewhere.

Chapter 9: Advanced Instruction Flow Techniques

This chapter provides a thorough overview of issues related to high-performance instruction fetching. The topics covered include historical, currently used, and proposed advanced future techniques for branch prediction, as well as high-bandwidth and high-frequency fetch architectures like trace caches. Though not all such techniques have yet been adopted in real machines, future designs are likely to incorporate at least some form of them.

Chapter 10: Advanced Register Data Flow Techniques

This chapter highlights emerging microarchitectural techniques for increasing performance by exploiting the program characteristic of *value locality*. This program characteristic was discovered recently, and techniques ranging from software memoization, instruction reuse, and various forms of value prediction are described in this chapter. Though such techniques have not yet been adopted in real machines, future designs are likely to incorporate at least some form of them.

Chapter 11: Executing Multiple Threads

This chapter provides an introduction to thread-level parallelism (TLP), and provides a basic introduction to multiprocessing, cache coherence, and high-performance implementations that guarantee either sequential or relaxed memory ordering across multiple processors. It discusses single-chip techniques like multithreading and on-chip multiprocessing that also exploit thread-level parallelism. Finally, it visits two emerging technologies—implicit multithreading and preexecution—that attempt to extract thread-level parallelism automatically from single-threaded programs.

In summary, Chapters 1 through 5 cover fundamental concepts and foundational techniques. Chapters 6 through 8 present case studies and an extensive survey of actual commercial superscalar processors. Chapter 9 provides a thorough overview of advanced instruction flow techniques, including recent developments in advanced branch predictors. Chapters 10 and 11 should be viewed as advanced topics chapters that highlight some emerging techniques and provide an introduction to multiprocessor systems.

This is the first edition of the book. An earlier beta edition was published in 2002 with the intent of collecting feedback to help shape and hone the contents and presentation of this first edition. Through the course of the development of the book, a large set of homework and exam problems have been created. A subset of these problems are included at the end of each chapter. Several problems suggest the use of the

Simplescalar simulation suite available from the Simplescalar website at **http://www.simplescalar.com**. A companion website for the book contains additional support material for the instructor, including a complete set of lecture slides (**www.mhhe.com/shen**).

Acknowledgments

Many people have generously contributed their time, energy, and support toward the completion of this book. In particular, we are grateful to Bob Colwell, who is the lead author of Chapter 7, Intel's P6 Microarchitecture. We also acknowledge his coauthors, Dave Papworth, Glenn Hinton, Mike Fetterman, and Andy Glew, who were all key members of the historic P6 team. This chapter helps ground this textbook in practical, real-world considerations. We are also grateful to Professor Mark Smotherman of Clemson University, who meticulously compiled and authored Chapter 8, Survey of Superscalar Processors. This chapter documents the rich and varied history of superscalar processor design over the last 40 years. The guest authors of these two chapters added a certain radiance to this textbook that we could not possibly have produced on our own. The PowerPC 620 case study in Chapter 6 is based on Trung Diep's Ph.D. thesis at Carnegie Mellon University. Finally, the thorough survey of advanced instruction flow techniques in Chapter 9 was authored by Gabriel Loh, largely based on his Ph.D. thesis at Yale University.

In addition, we want to thank the following professors for their detailed, insightful, and thorough review of the original manuscript. The inputs from these reviews have significantly improved the first edition of this book.

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- Ali Zaringhalam, *Stevens Institute of Technology*
- Xiaobo Zhou, *University of Colorado at Colorado Springs*

This book grew out of the course *Superscalar Processor Design* at Carnegie Mellon University. This course has been taught at CMU since 1995. Many teaching assistants of this course have left their indelible touch in the contents of this book. They include Bryan Black, Scott Cape, Yuan Chou, Alex Dean, Trung Diep, John Faistl, Andrew Huang, Deepak Limaye, Chris Nelson, Chris Newburn, Derek Noonburg, Kyle Oppenheim, Ryan Rakvic, and Bob Rychlik. Hundreds of students have taken this course at CMU; many of them provided inputs that also helped shape this book. Since 2000, Professor James Hoe at CMU has taken this course even further. We both are indebted to the nurturing we experienced while at CMU, and we hope that this book will help perpetuate CMU's historical reputation of producing some of the best computer architects and processor designers.

A draft version of this textbook has also been used at the University of Wisconsin since 2000. Some of the problems at the end of each chapter were actually contributed by students at the University of Wisconsin. We appreciate their test driving of this book.

John Paul Shen, *Director,*
Microarchitecture Research, Intel Labs, Adjunct Professor,
ECE Department, Carnegie Mellon University

Mikko H. Lipasti, *Assistant Professor,*
ECE Department, University of Wisconsin

June 2004
Soli Deo Gloria

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