国外电子信息精品著作(影印版)

模拟/射频集成电路设计的晶体管级建模

Transistor Level Modeling for Analog/RF IC Design

W.Grabinski
B.Nauwelaers
D.Schreurs

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模拟/射频集成电路设计的晶体管级建模

Transistor Level Modeling for Analog/RF IC Design

●Present a wealth of knowledge regarding the most relevant aspects in the field of MOS transistor modeling.

●Lays out the 2/3D process and device simulations as an effective tool for a better understanding of the internal behavior of semiconductor structures and this with a focus on high-voltage MOSFET devices.

●The mainstream developments of both the PSP and the EKV models are discussed in detail. These physics-based MOSFET models are compared to the measurement-based models which are frequently used in RF applications.

●The comparison includes an overview of the relevant empirical models and measurement techniques.

●Include SOI-specific aspects, modeling enhancement of small geometry MOSFET devices and a survey of quantum effects in devices and circuits.

国外电子信息精品著作（影印版）

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内 容 简 介

器件的模型一直是模拟/射频集成电路工程师关心的问题。是否能建立一个尽可能反映器件行为的模型关系到整个集成电路设计的成败。本书内容丰富，从主流模型的讨论到小尺寸器件模型和量子效应的介绍，从模型参数的提取方法到模型在硬件描述语言中的应用等方面都作了详细的论述。本书对设计工程师和器件工程师都有很好的参考价值。

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《国外电子信息精品著作》序

20世纪90年代以来，信息科学技术成为世界经济的中坚力量。随着经济全球化的进一步发展，以微电子、计算机、通信和网络技术为代表的信息技术，成为人类社会进步过程中发展最快、渗透性最强、应用面最广的关键技术。信息技术的发展带动了微电子、计算机、通信、网络、超导等产业的发展，促进了生命科学、新材料、能源、航空航天等高新技术产业的成长。信息产业的发展水平不仅是社会物质生产、文化进步的基本要素和必备条件，也是衡量一个国家的综合国力、国际竞争力和发展水平的重要标志。在中国，信息产业在国民经济发展中占有举足轻重的地位，成为国民经济重要支柱产业。然而，中国的信息科学支持技术发展的力度不够，信息技术还处于比较落后的水平，因此，快速发展信息科学技术成为我国迫在眉睫的大事。

要使我国的信息技术更好地发展起来，需要科学工作者和工程技术人员付出艰辛的努力。此外，我们要从客观上为科学工作者和工程技术人员创造更有利于发展的环境，加强对信息技术的支持与投资力度，其中也包括与信息技术相关的图书出版工作。

从出版的角度考虑，除了较好较快地出版具有自主知识产权的成果外，引进国外的优秀出版物是大有裨益的。洋为中用，将国外的优秀著作引进到国内，促进最新的科技成就迅速转化为我们自己的智力成果，无疑是值得高度重视的。科学出版社引进一批国外知名出版社的优秀著作，使我国从事信息技术的广大科学工作者和工程技术人员能以较低的价格购买，对于推动我国信息技术领域的科研与教学是十分有益的事。

此次科学出版社在广泛征求专家意见的基础上，经过反复论证、仔细遴选，共引进了接近30本外版书，大体上可以分为两类，第一类是基础理论著作，第二类是工程应用方面的著作。所有的著作都涉及信息领域的最新成果，大多数是2005年后出版的，力求“层次高、内

容新、参考性强”。在内容和形式上都体现了科学出版社一贯奉行的严谨作风。

当然，这批书只能涵盖信息科学技术的一部分，所以这项工作还应该继续下去。对于一些读者面较广、观点新颖、国内缺乏的好书还应该翻译成中文出版，这有利于知识更好更快地传播。同时，我也希望广大读者提出好的建议，以改进和完善丛书的出版工作。

总之，我对科学出版社引进外版书这一举措表示热烈的支持，并盼望这一工作取得更大的成绩。

中国科学院院士
中国工程院院士
2006 年 12 月

FOREWORD

Among many great inventions made in the 20th century, electronic circuits, which later evolved into integrated circuits, are probably the biggest, when considering their contribution to human society. Entering the 21st century, the importance of integrated circuits has increased even more. In fact, without the help of integrated circuits, recent high-technology society with the internet, cellular phone, car navigation, digital camera, and robot would never have been realized. Nowadays, integrated circuits are indispensable for almost every activity of our society.

One of the critical issues for the fabrication of integrated circuits has been the precise design of the high-speed or high-frequency operation of circuits with huge number of components. It is quite natural to predict the circuit operation by computer calculation, and there have been three waves for this, at 15-year intervals. The first wave came at the beginning of the 1970s when LSIs (Large Scale Integrated circuits) with more than 1000 components had just been introduced into the market. A mainframe computer was used for the simulation, and each semiconductor company used its own proprietary simulators and device models. However, the capability of the computer and accuracy of the model were far from satisfactory, and there are many cases of the necessity of circuit re-design after evaluation of the first chip.

The second wave hit us in the middle of 1980s, when the EWS (Engineering Work Station) was introduced for use by designers. At that time, most of the simulation tools were already provided by software vendors and standard device models for public use were being established. The simulation of circuits became considerably more accurate and the amount of re-design was significantly reduced. The third wave started to flood us at the beginning of this century, when the PC provided sufficiently high performance for circuit simulation. We are facing the front of the third wave now.

The situation for device models for circuits has changed very much during the past 20 years. Ten years ago, the model was kept in strict secrecy within each

semiconductor company, in most cases. Now the semiconductor companies adopt open public standard models or even common model parameters in order to provide a familiar design environment to their customers. Recently, very accurate and complex models have been required to cope with the need to design extremely high-speed logic circuits with ultra-small transistors – sometimes even with an SOI substrate. The characteristics of ultra-small CMOS devices are quite different from those of older larger transistors and the models become very complicated. Also, the macroscopic treatment of large number of logic devices with hardware description languages such as VHDL-AMS or Verilog-A becomes very important, with tremendous increases in integration.

Another aspect is that the market for RF integrated circuits has become very large, and there are strong demands for an accurate RF model for CMOS and HBTs. Traditionally, modeling of RF devices was very difficult, because of the accuracy required not only for the first derivative of the I-V characteristics, but also for the third derivative. In addition, an accurate three-dimensional model of the substrate is essential for precise RF simulation of active and also passive components. The substrate model is also important for noise simulation, which is a key element in RF devices. Corresponding to the accuracy and complexity of the model required, the expression of the model has wide variety; empirical expression, analytical expression, table look-up expression, and numerical expression obtained by numerical simulation.

The importance of compact modeling for circuits is becoming bigger and bigger in the third wave, and we expect to see great progress. This book includes some of the recent important advances in compact modeling. It is our hope that this book will be useful for designers and modeling scientists facing the front of the third wave.

Hiroshi Iwai
Tokyo Institute of Technology

December 1, 2005

INTRODUCTION

Wladek Grabinski, Bart Nauwelaers and Dominique Schreurs

The accuracy of the integrated circuit analysis performed in contemporary design flows is directly correlated to the quality of its fundamental components – the models. To ensure on-time delivery of these models, characterization and model generation must be rapid and precise. To be able to take full advantage of the new semiconductor technologies, the designers have to update their CAD tools regularly with precise definitions of the new device models that can be implemented into circuit simulators and design flows. The models must preferably be physics-based to account for complex dependences of the device properties on dimensions and other process variables. The model parameters are derived from measurements and characterization of the devices. For RF CMOS (bulk and SOI) and compound technologies, both modeling and characterization are challenging tasks that will be especially emphasized in this book.

This book is aimed at radio frequency (RF)/analog and mixed-signal integrated circuit (IC) designers, computer-aided design (CAD) engineers, semiconductor physics students, as well as wafer fab process engineers working on device, compact model level. We can summarize the goals of the book as follow:

- to give the reader a consistent introduction to the main steps of compact model developments, including advanced 2/3D process and device simulations, consistent and accurate MOSFET modeling founded on the physical concepts of the surface potential, charge-based modeling, empirical modeling of small and large signal device behavior, and modeling approaches that are based on linear as well as non-linear measurements;
- to illustrate the impact of device-level modeling on IC design using selected examples;

– to provide a detailed insight into modeling and design flow automation based on high-level behavioral languages, i.e. VHDL-AMS and Verilog-A.

We have structured this book to cover the key aspects of compact model developments, showing consistent flow of the implementation and dissimilation as well as its standardization tasks. Following that organization, the book is divided into ten main chapters:

In the first chapter of this book, D. Donoval *et al.* introduce 2/3D process and device simulation as an effective tool for better understanding of the internal behavior of semiconductor structures. Process simulations are used to create a virtual device with geometry and properties identical to the real structure, and such basic technology steps as ion implantation, diffusion, epitaxial growth, oxidation, deposition and etching are presented. Then numerical 2/3D device simulations are performed. The complete simulation flow is illustrated by three advanced examples: a bipolar transistor, a CMOS inverter structure and a power vertical DMOS transistor multi-cell structure. These kinds of virtual device structures created by 2/3D process and device simulations are often used as initial inputs for compact model development and validation.

Bulk CMOS models make up the main stream of the compact models. Next, two chapters discuss two concepts of the physics-based models for CMOS devices.

R. van Langevelde *et al.* present PSP: an advanced surface-potential-based MOSFET. The PSP compact model jointly developed by Philips Research and Pennsylvania State University is based on fundamental physics (the surface potential approach) over the entire MOSFET device operating regime. Such effects as gate leakage, noise, non-quasistatic (NQS) and quantum-mechanical effects, which become increasingly important with the downscaling of CMOS technology, are physically modeled within PSP and have been verified experimentally. The model also provides a better description of high-frequency behavior. The PSP model enables improved simulations of a wide class of circuits including analog/RF modules that are important in the mobile communication technology and other advanced designs. The PSP compact model is supported by professional software environments, including Verilog-A, which allow it to be directly coupled to many popular circuit simulators. The PSP model has been submitted to the Compact Model Council (CMC) as a candidate for standardization.

M. Bucher *et al.* present EKV3.0: an advanced charge-based MOSFET transistor model which is design-oriented towards next-generation CMOS technologies and IC designs. Historically, the development of the EKV model is driven by the needs of analog IC designers. This chapter presents the physical foundation of the EKV charge model, which is itself based on a surface-potential analysis. The basic charge modeling approach allows not only

physically consistent and accurate modeling of current, terminal charges and noise, but also offers a unique set of suitable expressions for hand-calculation of analog/RF circuits. The fully-featured EKV3.0 compact MOST model for circuit simulation is presented and validated using advanced RF application examples down to sub-100 nm CMOS technologies. Finally, the parameter extraction procedure and implementation in the Verilog-A language are briefly discussed.

The next two chapters describe empirical models, and also include information on measurement techniques used for model extraction or creation.

Reliable measurements are a prerequisite for any sensible device modeling work, in particular for RF applications where the silicon or III–V compound material-based device models are required to predict their subtlest behavior. D. Schreurs focuses on MOSFET modeling using direct high-frequency measurements. After explaining the theoretical background of two high-frequency modeling approaches, the author discusses the main characterization steps, i.e. linear and non-linear vector measurements and the importance of de-embedding, as well as equivalent circuit and behavioral modeling. Both linear and non-linear measurement-based modeling approaches are explained and their different implementations are illustrated by examples.

I. Angelov discusses empirical FET models. Experimental static current, S-parameter and capacitance characteristics are linked with small and consistent large signal equivalent circuit modeling, leading to an empirical FET model. This creates a basis for reviewing Standard and Extended Curtice Models, the Materka-Kacprzak Model, the Triquint Model, the EESOF Model, and the Chalmers FET Model. The author also shows an extended empirical model to incorporate physical phenomena such as thermal effects and dispersion.

The following three chapters bring some specific physical aspects into the modelling arena: SOI with its special substrate build-up, effects of very small dimension MOSFETs, and quantum effects that are observable in some circuits.

Silicon-on-insulator (SOI) CMOS technologies offer exceptional advantages not only for digital designs but also for RF, low-GHz telecommunication and microwave IC designs. B. Parvais and A. Siligaris present an empirical approach to modeling the SOI MOSFET nonlinearities. The analytical model is introduced to describe the nonlinear behavior of the SOI device from DC to RF coherently, and to account for the dispersive character of some physical phenomena, such as floating body (FB) effects in the SOI device. The simulations of a new model were validated by measurements and explained by a simple analytical model, based on the Volterra series approach.

Some of the models might not properly describe some physical effects presented in aggressively down-scaled CMOS technologies. As the MOSFET models are critical for reliable RF designs, new physical effects must be incorporated and alternative modeling techniques must be proposed. N. Itoh focuses on and describes some insufficiently modeled phenomena in the recent small

geometry MOSFETs, i.e. mobility degradation due to STI stress and channel noise enhancement due to hot carrier effects. His model accounts for physical effects associated with STI stress, scalable parasitic components and channel thermal noise allowing the reduction of both the cost and design period of advanced RF/analog IC design.

F. Felgenhauer *et al.* discuss incorporation of parasitic quantum effects in classical circuit simulations. The performance of a state-of-art CMOS device is influenced by an increasing number of parasitic effects associated with recent down-scaling of integrated semiconductor devices. Beside semi-classical parasitic effects and leakage currents such as sub-threshold current, DIBL and GIBL, further parasitic effects of quantum mechanical origin must be included in device modeling. The discussion covers the physics and the simulation of coherent charge transport with a successful attempt to include quantum effects in high-level circuit simulations such as SPICE. The simulation model developments are illustrated by three different circuit examples, which explicitly exhibit the influence of quantum effects on circuit functionality.

The two final chapters provide detailed insight into how modeling and design flow automation can be supported and enhanced by analog hardware description languages (AHDLs) such as VHDL-AMS and Verilog-A.

C. Lallement *et al.* present the capabilities of the VHDL-AMS hardware description language for compact model development. The chapter is a case study and shows that VHDL-AMS can be successful used for implementation of such models as EKV 2.6 and MM11 MOSFETs. The authors also show that the basic models can be easily enhanced to include major physical effects like self-heating, extrinsic aspects and quantum effects, since the VHDL-AMS language naturally supports multi-domain. VHDL-AMS is not limited to single device compact modelling but also can be used to describe innovative integrated devices, like Micro-Opto-Electro-Mechanical Systems (MOEMS) integrating different application-field parts on the very same chip (e.g. mechanical, electrical, thermal, and fluidic parts). Similarly to Verilog-A, discussed in the next chapter, application of VHDL-AMS to compact modeling is an attempt to standardize the compact modeling development environment.

B. Troyanovsky *et al.* present Verilog-A, a behavioral language for compact modeling of MOSFET developments, as a platform-independent software tool. The authors introduce Verilog-A, a general-purpose modeling language, by examples guiding the reader through language elements, operators, functions and structure, with particular emphasis on the constructs important to the compact model developer. The recent Verilog-A release of the language standard has added several features of interest to compact model developers. The main language extensions are discussed in the chapter. It is important to note that several academic and industrial model development groups, i.e. PSP and EKV teams, now use Verilog-A as a main and a platform-independent language of their development methodology.

From this summary of the contents of the book, the reader can see that a broad overview of modelling techniques in the MOS arena is described by a select group of authors. Very fine contributions regarding the best compact models are complemented with equally good work regarding measurement-based modeling. Additionally a number of specific topics on SOI, small devices, quantum effects and hardware description languages (VHDL-AMS, Verilog-A) further increase the usefulness of this book.

Bringing together such a notable group of authors is a very visible result of the ongoing effort of the MOS-AK group, behind which one of the editors, W. Grabinski, is a driving force, to bring all European researchers in the advanced MOS field together and to keep them talking about their mutual research interests, and more specifically about the modeling aspects of MOS devices and circuits.

It was just after the MOS-AK workshop organized in September 2004 at the University of Leuven that the co-operation between the publisher and the editors to create this book was initiated. The editors would like to thank the authors of the various chapters and the publishers' staff for bringing this project to a successful conclusion.

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Chapter 1

2/3-D PROCESS AND DEVICE SIMULATION

An effective tool for better understanding of internal behavior of semiconductor structures

Daniel Donoval[1], Andrej Vrbicky[1], Ales Chvala[1], and Peter Beno[2]
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Abstract: 2/3-D numerical process and device simulation is presented as an extremely useful tool for the analysis and characterization of fabrication processes and corresponding electro-thermal behavior of semiconductor structures and devices standing alone and/or coupled in integrated circuits. In the introductory part of this chapter, a brief description is given of the basic features, processes, and structures implemented in the numerical process and device simulation. Visualization of the internal properties (electrical, thermal, optical, magnetic, and mechanical) allows comprehensive analysis of the critical regions and weak points of the analyzed structures. The presented examples illustrate the potential, power and beauty of numerical simulation of processes and devices for the identification and analysis of the behavior of parasitic devices that exist as inevitable parts of active devices and which degrade the normal operation and reliability of integrated circuits. Commercially available TCAD process and device simulators with verified calibrated complex electro-physical models, advanced numerical solvers securing stable calculations, and user friendly interactive environment provide a unique insight into the internal operation of the analyzed structure. They can be efficiently used for comprehensive physical interpretation of experimentally obtained results and/or particularly for prediction of the properties and behavior of new semiconductor structures and devices as well as for further development and optimization of new technologies and fabrication steps.

W. Grabinski, B. Nauwelaers and D. Schreurs (eds.),
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