Gallium Nitride Power Devices

edited by Hongyu Yu | Tianli Duan

Gallium Nitride Power Devices

edited by

Hongyu Yu
Tianli Duan

Pan Stanford Publishing

Published by

Pan Stanford Publishing Pte. Ltd.
Penthouse Level, Suntec Tower 3
8 Temasek Boulevard
Singapore 038988

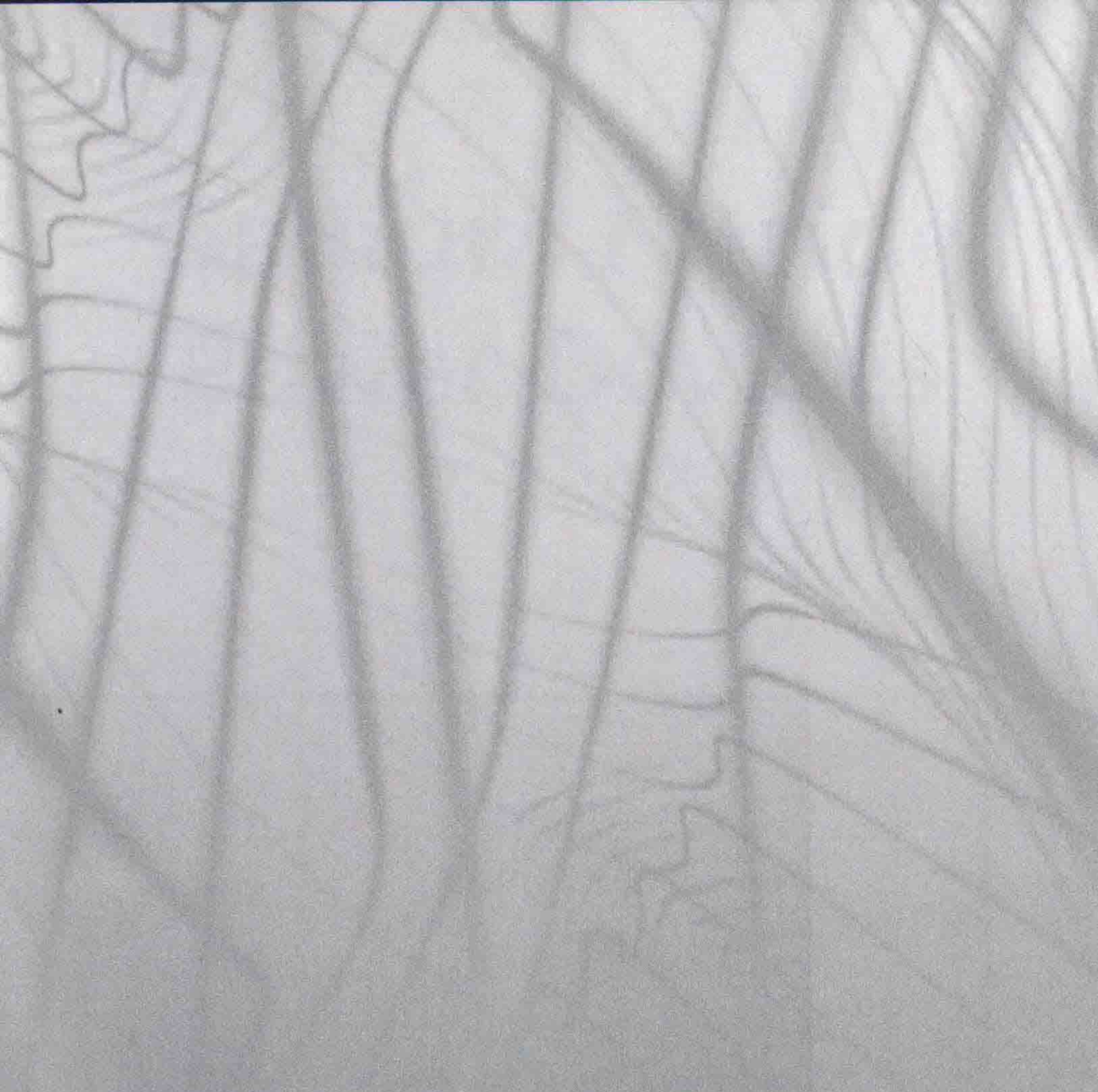
Email: editorial@panstanford.com
Web: www.panstanford.com

British Library Cataloguing-in-Publication Data
A catalogue record for this book is available from the British Library.

Gallium Nitride Power Devices

ISBN 978-981-4774-09-3 (Hardcover)
ISBN 978-1-315-19662-6 (eBook)

Printed in Canada



Gallium Nitride Power Devices

Preface

As a third-generation semiconductor, GaN has found broad technological applications in high-power devices by virtue of its high breakdown field and high electron mobility. Therefore, the development of GaN technology is regarded as important national strategic research for many countries. The industry has made phenomenal growth in GaN electronics. Moreover, many GaN-related papers have been published to report the progress in the fundamental concepts and performances of GaN devices.

To access both fundamental knowledge and advanced novel development, a book that could give information about comprehensive material physics and device structure as well as device operational principles was needed. To meet such a need, *Gallium Nitride Power Devices* was prepared. This book comprises nine chapters which discuss the growth technology of GaN wafers and the characteristics of polarization effects of GaN material and device process on device performance, reliability, and packaging. It is a textbook for undergraduate students, and it is also a reference book for graduate students as well as engineers and scientists in GaN research.

In the course of writing this book, I was fortunate to obtain the help of Wang Zhigang and Wang Bing from Southwest Jiaotong University, Cheng Kai from Enkris Semiconductor, Liu Zhihong from the Singapore-MIT Alliance for Research and Technology, and Jiang Lingli, Xia Pengkun, and Dongbin from the South University of Science and Technology of China.

Tianli Duan

Contents

Chapter 1

The Growth Technology of High-Voltage GaN on Silicon

Peng Xiang, Liyang Zhang, and Kai Cheng
Enkris Semiconductor, Inc., Suzhou, China
Peng.Xiang@enkris.com

1.1 Introduction

Due to the limited availability and relatively high cost of sufficiently large GaN substrates for homoepitaxial growth, GaN films are normally grown on foreign substrates, such as sapphire, SiC, and Si. Table 1.1 shows properties of III nitrides and these foreign substrates. SiC has the smallest lattice mismatch and thermal expansion coefficient (TEC) mismatch to GaN as compared to others, but the high price and limited diameter (normally ≤6 inches) of a SiC substrate make it unaffordable for power applications. GaN-on-sapphire substrate technology is very mature and is the mainstream in the light-emitting diode (LED) market, but it is unsuitable for power applications due to the poor thermal conductivity of sapphire.

Gallium Nitride Power Devices
Edited by Hongyu Yu and Tianli Duan

ISBN 978-981-4774-09-3 (Hardcover), 978-1-315-19662-6 (eBook)
www.panstanford.com

Si is the most widely used semiconductor nowadays, and using a Si substrate has many advantages over SiC and sapphire, such as a large diameter, low cost, and a ready-made process. The diameter of a Si substrate can be scaled to 12 inches, and the metal-organic chemical vapor deposition (MOCVD) reactor is available to grow 8-inch GaN epilayers on 8-inch Si substrates. In contrast, the SiC and sapphire substrate size is typically smaller than 6 inches. The cost of GaN power devices can be further reduced by using the ready-made 6- and 8-inch complementary metal-oxide-semiconductor (CMOS) process line. A Si substrate also shows high crystalline quality and minimized defect density, thanks to decades of development of the Si semiconductor industry. It has been well accepted that GaN on large-size silicon substrates is one cost-effective way to achieve high-volume production of GaN power devices. Figure 1.1 shows the epitaxial relationship of the GaN(0001) plane (c-plane) on the Si(111) plane. Usually, a Si(111) substrate is utilized for the epitaxial growth of c-plane GaN because of their same trigonal symmetry.

Table 1.1 Properties of III nitrides and substrates [1, 2]

Material		Lattice parameters (Å)	Lattice mismatch[a] to GaN	TEC[b] (10^{-6} K^{-1})	Thermal conductivity (W/cmK)	Diameter (inches)
III nitrides	AlN	$a = 3.112$ $c = 4.982$	2.48%	4.2	2.0	/
	InN	$a = 3.548$ $c = 5.7034$	−10.1%	5.7	0.8	/
	GaN	$a = 3.1891$ $c = 5.1855$	0	5.59	1.3	/
Substrates	Al_2O_3	$a = 4.765$ $c = 12.982$	13.9% Rotated 30°	7.5	0.3	2–6
	SiC	$a = 3.081$ $c = 15.117$	3.51%	4.2	4.9	2–6
	Si	$a = 5.431$	−17%	3.59	1.3	2–12

[a]Lattice mismatch $=(a_{GaN}-a_{eff.sub})/a_{sub}$
[b]TEC: Thermal expansion coefficient

However, the growth of GaN on Si is challenging owing to issues such as melt-back etching and a large thermal and lattice mismatch [4]. A common problem in the growth of GaN on Si is melt-back etching. The origin of melt-back etching is the alloying reaction between Ga and Si at high temperature (HT). Ga has high solubility in Si at high temperature. When Ga comes in contact with Si at high temperature, the alloy of Ga and Si forms and produces hollows and swellings on the substrate, which seriously destroys the epilayers (Fig. 1.2). Once the melt-back-etching process starts, it will expand during the following growth and cannot be stopped. Therefore it is extremely important to prevent melt-back for growing GaN on Si. Ga-free layers, such as AlN, SiC [5], AlAs [6], and Al_2O_3 [7], were employed to prevent Ga from contacting Si. Ascribed with the advantages of high thermal stability and convenience, AlN is normally used as a starting buffer layer for GaN on Si.

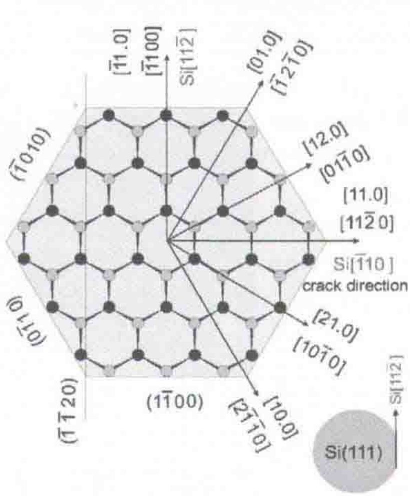
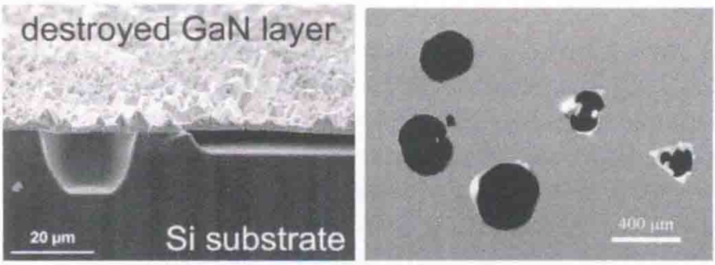


Figure 1.1 Epitaxial relationship GaN(0001) on Si(111). Reprinted from Ref. [3], Copyright (2002), with permission from Elsevier.

One of the biggest challenges is the large stress caused by the thermal mismatch between GaN epilayers and Si substrates. The TEC of GaN is 5.59×10^{-6} K^{-1}, which is much larger than that of Si, 3.59 $\times 10^{-6}$ K^{-1}. A GaN epilayer is usually grown at a high temperature of 1000°C using MOCVD. When GaN is cooling down from growth temperature to room temperature, a large tensile stress of about 1 Gpa is generated in the GaN film because the TEC of the Si substrate is significantly smaller than that of GaN. Consequently, there is a much greater risk that the GaN epilayers will crack if the thickness of GaN exceeds several hundred nanometers, as shown in Fig. 1.3. A GaN layer with a thickness of several hundred nanometers is insufficient for producing high-quality films and devices. GaN electronics on

Si can easily break down from the Si substrate because of the low critical electric field of Si. To achieve a high breakdown voltage, a film thickness of several micrometers is necessary for a GaN-on-Si power device.



(a) (b)

Figure 1.2 Destroyed GaN layer due to melt-back etching: (a) SEM image of a vertical view. Reprinted from Ref. [8], Copyright (2003), with permission from Elsevier. (b) Optical microscope image of a plan view.

Stress also introduces large wafer bow, which deteriorates the uniformity of the epilayer and causes failure during wafer handling and passing of the stepper in the lithography process, making the material unsuitable for device manufacturing. The wafer curvature κ can be obtained from the Stoney equation:

$$\kappa = \frac{6M_f\varepsilon_m h_f}{M_s h_s^{\,2}} \tag{1.1}$$

where ε_m, M_f, M_s, h_f, and h_s denote the biaxial mismatch strain, the biaxial moduli of the film, the biaxial moduli of the substrate, the thickness of the film, and the thickness of the substrate, respectively. Assuming the diameter of the substrate is D, the wafer bow can be obtained by

$$B = \frac{3M_f D^2}{4M_s h_s^{\,2}}\varepsilon_m h_f \tag{1.2}$$

The wafer bow is proportional to the square of the substrate diameter, indicating a larger value when a large-diameter Si substrate is utilized.

To grow crack-free GaN on Si with low wafer bow, stress engineering has to be executed. Compressive stress is introduced during growth by inserting Al-rich layers such as AlN [9–13], AlGaN [14–24], and AlN/GaN superlattices (SLs) [25–29] to counterbalance the tensile stress. Nevertheless, this compressive stress also should be carefully controlled. This compressive stress causes curvature of the wafer during growth, which will deteriorate the wafer temperature uniformity and cause plastic deformation (Fig. 1.4) if a too large curvature appears [30]. Thus stress engineering is of great importance and is challenging for the growth of a GaN-on-Si wafer.

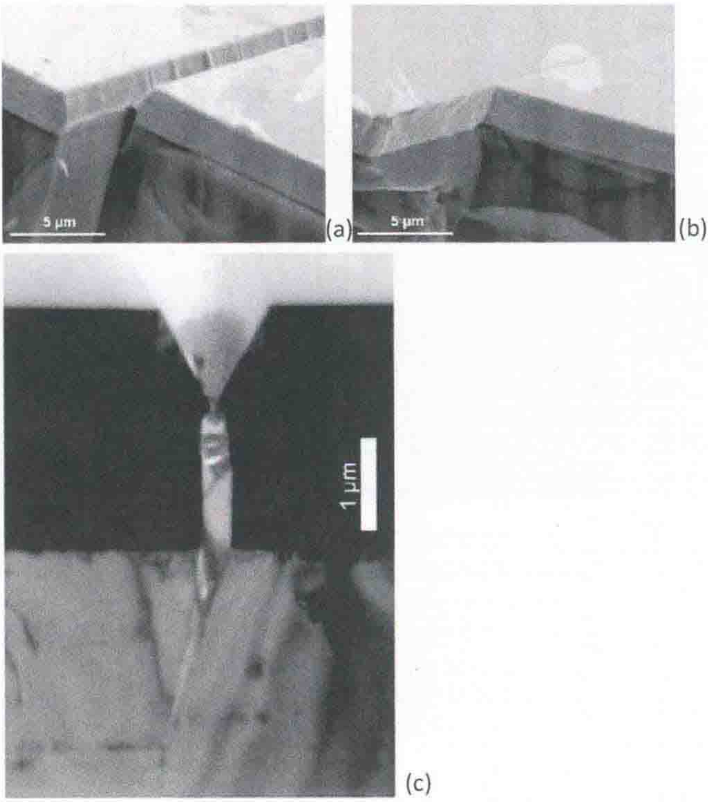


Figure 1.3 Two types of cracks for GaN on Si: (a) an open groove with facets occurs during growth and (b) a closed crack during cooling down; (c) cross section of an open crack. Reprinted from Ref. [3], Copyright (2002), with permission from Elsevier.

The large lattice mismatch between GaN and Si will introduce a high density of dislocations, which are usually larger than $10^8/cm^2$. High dislocation densities deteriorate the crystalline quality of GaN and the performance of power devices.

Apart from the large tensile stress and high dislocation density, GaN on Si has also suffered from high buffer leakage, which should be minimized for power applications. Compared to Si and GaAs, GaN grown on a heterosubstrate is a very imperfect crystal system with a high density of defects. Usually, the density of the background donor in unintentionally doped GaN is 10^{16}–$10^{17}/cm^3$ due to the existence of oxygen and silicon impurities and nitrogen vacancies, which introduces 10^{16}–$10^{17}/cm^3$ background electrons. Thus leakage current from the buffer layer will occur. Additionally, the Si substrate and the AlN/Si interface are conducting. A GaN buffer with a high background donor will also introduce leakage current from the Si substrate. Compositional doping [32–39] and removal of the Si substrate [40] are effective in reducing the buffer leakage and increasing the breakdown voltage of GaN on Si.

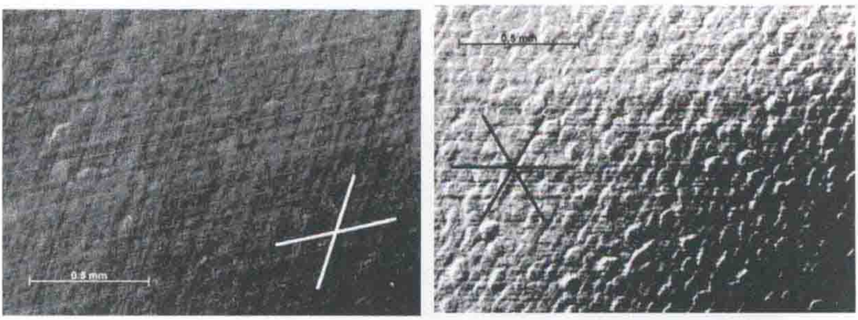


Figure 1.4 Nomarski microscope image of plastic substrate deformation for GaN-on-Si layers in two different appearances. The image on the left shows a weaker deformation, with slip lines in the Si(111) substrate only visible in two different directions (marked white), while the image on the right shows strong deformation, with slip lines propagating in all three preferred directions (marked black). Reproduced from Ref. [31] with permission from John Wiley and Sons.

1.2 The Nucleation Layer Growth

Due to the melt-back etching phenomenon mentioned earlier, GaN cannot be directly grown on a Si substrate at high temperature. AlN [20, 41–49], SiC [5], AlAs [6], and Al_2O_3 [7] were applied as the seeding layer for GaN grown on Si. AlN is the most universal nucleation layer that supports high-quality GaN on a Si substrate. With high thermal stability and good wettability on Si, the AlN buffer prevents the melt-back reaction and favors the subsequent growth of the GaN layer. In addition, compressive stress can be generated in GaN films grown on AlN because of the smaller lattice parameters of AlN, which can counterbalance the tensile stress when cooling down.