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CMOS锁相环：分析和设计

CMOS PLL Synthesizers: Analysis and Design

Keliu Shu
Edgar Sánchez-Sinencio

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CMOS PLL Synthesizers: Analysis and Design

●This book presents both fundamentals and the state of the art of PLL synthesizer design and analysis techniques.

●A complete overview of both system-level and circuit-level design and analysis are covered.

●A 16mW, 2.4GHz, sub-2V, Sigma Delta fractional-N synthesizer prototype is implemented in 0.35m m CMOS. It features a high-speed and robust phase-switching prescaler, and a low-complexity and area-efficient loop capacitance mulitplier, which tackle speed and integration bottlenecks of PLL synthesizer elegantly.

●This book is conceived as a PLL synthesizer manual for both academia researchers and industry design engineers.

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内 容 简 介

本书是一本关于小型 sigma-delta 频率综合器方面的优秀著作。作者分别从系统级和电路级对频率综合器的设计进行了阐述。主要创新点在低功耗高速分频器和减少芯片面积的环路滤波器的电容设计上。该书涉及 PLL 的基础问题，内容全面翔实，由浅入深，对 PLL 的关键问题提出了解决方案。

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《国外电子信息精品著作》序

20世纪90年代以来，信息科学技术成为世界经济的中坚力量。随着经济全球化的进一步发展，以微电子、计算机、通信和网络技术为代表的信息技术，成为人类社会进步过程中发展最快、渗透性最强、应用面最广的关键技术。信息技术的发展带动了微电子、计算机、通信、网络、超导等产业的发展，促进了生命科学、新材料、能源、航空航天等高新技术产业的成长。信息产业的发展水平不仅是社会物质生产、文化进步的基本要素和必备条件，也是衡量一个国家的综合国力、国际竞争力和发展水平的重要标志。在中国，信息产业在国民经济发展中占有举足轻重的地位，成为国民经济重要支柱产业。然而，中国的信息科学支持技术发展的力度不够，信息技术还处于比较落后的水平，因此，快速发展信息科学技术成为我国迫在眉睫的大事。

要使我国的信息技术更好地发展起来，需要科学工作者和工程技术人员付出艰辛的努力。此外，我们要从客观上为科学工作者和工程技术人员创造更有利于发展的环境，加强对信息技术的支持与投资力度，其中也包括与信息技术相关的图书出版工作。

从出版的角度考虑，除了较好较快地出版具有自主知识产权的成果外，引进国外的优秀出版物是大有裨益的。洋为中用，将国外的优秀著作引进到国内，促进最新的科技成就迅速转化为我们自己的智力成果，无疑是值得高度重视的。科学出版社引进一批国外知名出版社的优秀著作，使我国从事信息技术的广大科学工作者和工程技术人员能以较低的价格购买，对于推动我国信息技术领域的科研与教学是十分有益的事。

此次科学出版社在广泛征求专家意见的基础上，经过反复论证、仔细遴选，共引进了接近30本外版书，大体上可以分为两类，第一类是基础理论著作，第二类是工程应用方面的著作。所有的著作都涉及信息领域的最新成果，大多数是2005年后出版的，力求“层次高、内

容新、参考性强”。在内容和形式上都体现了科学出版社一贯奉行的严谨作风。

当然，这批书只能涵盖信息科学技术的一部分，所以这项工作还应该继续下去。对于一些读者面较广、观点新颖、国内缺乏的好书还应该翻译成中文出版，这有利于知识更好更快地传播。同时，我也希望广大读者提出好的建议，以改进和完善丛书的出版工作。

总之，我对科学出版社引进外版书这一举措表示热烈的支持，并盼望这一工作取得更大的成绩。

中国科学院院士
中国工程院院士
2006 年 12 月

Preface

Thanks to the advance of semiconductor and communication technology, the wireless communication market has been booming in the last two decades. It evolved from simple pagers to emerging third-generation (3G) cellular phones. In the meanwhile, broadband communication market has also gained a rapid growth. As the market always demands high-performance and low-cost products, circuit designers are seeking high-integration communication devices in cheap CMOS technology.

The phase-locked loop frequency synthesizer is a critical component in communication devices. It works as a local oscillator for frequency translation and channel selection in wireless transceivers and broadband cable tuners. It also plays an important role as the clock synthesizer for data converters in the analog-and-digital signal interface.

This book covers the design and analysis of PLL synthesizers. It includes both fundamentals and a review of the state-of-the-art techniques. The transient analysis of the third-order charge-pump PLL reveals its locking behavior accurately. The behavioral-level simulation of PLL further clarifies its stability limit. Design examples are given to clearly illustrate the design procedure of PLL synthesizers. A complete derivation of reference spurs in the charge-pump PLL is also presented in this book.

The in-depth investigation of the digital $\Sigma\Delta$ modulator for fractional-N synthesizers provides insightful design guidelines for this important block. As the prescaler is often the speed bottleneck of high-frequency PLL synthesizers, it is covered in a single chapter in this book. An inherently glitch-free low-power phase-switching prescaler was developed. The timing analysis of the switching control loop gives good understanding for a sound design. As spurs generated from the delay mismatch in the phase-switching

prescaler might be a concern, it is mathematically examined. Another single chapter in this book is devoted to the loop filter, which is an integration bottleneck in narrow-band PLL because its big capacitor takes a large chip area. A simple area-efficient on-chip loop filter solution was proposed. It is based on a capacitance multiplier, which is of very low complexity and power consumption. Detailed analysis and design of this novel loop filter was addressed.

As this book features a complete coverage of PLL synthesizer design and analysis techniques, the authors hope it will be a good manual for both acdemia researchers and industry designers in the PLL area.

List of Acronyms and Symbols

AAC	Automatic Amplitude Control
BPF	Band-Pass Filter
CCO	Current-Controlled Oscillator
CDR	Clock and Data Recovery
CMOS	Complementary Metal Oxide Semiconductor
CP	Charge-Pump
DAC	Digital-to-Analog Converter
DAS	Direct Analog Synthesizer
DDS	Direct Digital Synthesizer
DFDD	Digital Frequency Difference Detector
DLL	Delay-Locked Loop
DPA	Digital Phase Accumulator
DUT	Device Under Test
FDC	Frequency-to-Digital Converter
FF	Flip-Flop
FHSS	Frequency-Hopping Spread Spectrum
FM	Frequency Modulation
FN	Fractional-N
FS	Frequency Synthesizer
GSM	Global System for Mobile communications
IC	Integrated Circuit
ILFD	Injection-Locked Frequency Divider
ISF	Impulse Sensitivity Factor
ISM	Industrial Scientific Medicine
LF	Loop Filter
LO	Local Oscillator
LTI	Linear Time-Invariant
LSB	Least-Significant-Bit

MASH	Multi-stage noise Shaping
NAND	Negative AND logic
NCO	Numerically Controlled Oscillator
NMOS	N-channel Metal Oxide Semiconductor
NOR	Negative OR logic
OPA	Operational Amplifier
OSR	Over Sampling Ratio
OTA	Operational Transconductance Amplifier
PD	Phase Detector
PFD	Phase-Frequency Detector
PGS	Patterned Ground Shield
PLL	Phase-Locked Loop
PMOS	P-channel Metal Oxide Semiconductor
PSD	Power Spectral Density
RF	Radio Frequency
rms	Root-Mean-Square
SC	Switched Capacitor
SCL	Source-Coupled Logic
SDM	Sigma-Delta Modulator
SNR	Signal-to-Noise Ratio
SSB	Single-Sideband
TSPC	True-Single-Phase-Clock
VCO	Voltage-Controlled Oscillator
XOR	Exclusive OR logic

ω	angular frequency in *rad/s*
ω_{-3dB}	PLL $-3dB$ loop bandwidth
ω_c	PLL loop (unity-gain / crossover) bandwidth
ω_{c1}	1st corner frequency of capacitance multiplier impedance
ω_{c2}	2nd corner frequency of capacitance multiplier impedance
ω_{c3}	3rd corner frequency of capacitance multiplier impedance
ω_n	natural frequency
ω_{p1}	1st pole-frequency of loop filter transimpedance
ω_{p2}	2nd pole-frequency of loop filter transimpedance
ω_{p3}	3rd pole-frequency of loop filter transimpedance
ω_{ref}	PLL reference angular frequency (at PFD)
ω_z	zero-frequency of loop filter
$\omega_{1/f}$	corner angular frequency of $1/f$ noise
$\Delta\omega_{1/f^3}$	corner angular frequency of oscillator $1/f^3$ phase noise

$\Delta\omega$	angular frequency offset from carrier
$\Delta\omega_H$	PLL hold range
$\Delta\omega_L$	PLL lock range
$\Delta\omega_P$	PLL pull-in range
$\Delta\omega_{PO}$	PLL pull-out range
ϕ	phase
ϕ_m	phase margin
$\Delta\phi$	amplitude of phase modulation
$\Delta\phi_{rms}$	PLL output *rms* phase noise
θ	phase
θ_e	phase error at PFD inputs
θ_{in}	input phase (noise)
θ_{out}	output phase (noise)
θ_{vco}	VCO phase noise
φ	random phase variation
ζ	damping factor
ε	normalized settling frequency error of PLL
£	phase noise in *dBc/Hz*
σ_c	*rms* of cycle jitter
σ_{cc}	*rms* of cycle-to-cycle jitter
τ	time
δ	impulse function (Dirac delta function)
δ_T	periodic impulse function with period T
Γ	ISF function
B	current ratio
C_1	1st capacitance of passive loop filter
C_2	2nd capacitance of passive loop filter
C_3	3rd capacitance of passive loop filter
C_{p1}	1st parasitic capacitance of capacitance multiplier
C_{p2}	2nd parasitic capacitance of capacitance multiplier
f	frequency in *Hz*
f_0	carrier frequency
f_c	PLL loop (unity-gain / crossover) bandwidth
f_{div}	loop divider output frequency
f_m	modulation frequency

f_{ref}	PLL reference frequency (at PFD)
f_{vco}	VCO frequency
f_{RF}	RF frequency (of mixer)
f_{LO}	local oscillator frequency
Δf	offset frequency from the carrier
$\Delta f_{1/f^3}$	corner frequency of oscillator $1/f^3$ phase noise
F	active device noise factor
g	conductance, transconductance
G	conductance, transconductance
h	transfer function
H	transfer function
H_{cl}	PLL closed-loop input-to-output phase (noise) transfer function
H_e	PLL input phase (noise) to PFD phase error transfer function
H_{ol}	PLL open-loop input-to-output phase (noise) transfer function
H_{V_C}	PLL input phase to LF output voltage transfer function
i	current
i_{cp}	charge-pump current noise
I	current in-phase signal
I_c	control current of CCO
I_{cp}	charge-pump current
I_{cpi}	charge-pump current of integration path
I_{cpp}	charge-pump current of proportional path
I_{dn}	charge-pump current for discharging the load capacitor
I_p	output current of LF's proportional path
I_{up}	charge-pump current for charging the load capacitor
I_z	output current of LF's integration path
j	integer number
k	binary integer input of DPA or digital SDM Boltzmann constant
K	PLL loop gain
K_{pd}	PFD and charge-pump gain in *A/rad*
K_{vco}	VCO conversion gain in *rad/s/V*
K_{cco}	CCO conversion gain in *rad/s/A*

L	integer number (order of SDM) inductance
m	integer number
M	modulus of DPA or digital SDM
n	integer number
n_Q	output integer of digital SDM
N	number (nominal) frequency divide ratio of loop divider
N_B	integer part of fractional-N divide ratio
P	prescaler divide ratio power
P_r	PLL reference spur level in *dBc*
q	charge
Q	quadrature signal quality factor quantization noise
Q_L	loaded quality factor
R	resistance auto-correlation function
R_1	1st resistance of passive loop filter
R_2	2nd resistance of passive loop filter
R_φ	auto-correlation function of random phase φ
S	power spectrum
S_φ	power spectral density of random phase variation
S_V	power spectral density of signal $V(t)$
t	time
t_{on}	charge-pump turn-on time in locked state
T	time temperature
T_L	PLL lock-in time (rough estimation)
T_P	PLL pull-in time
T_{ref}	period of PLL reference signal
ΔT_{abs}	absolute jitter
ΔT_{cn}	cycle-to-average jitter
ΔT_{ccn}	cycle-to-cycle jitter
u	unit step function
v	voltage
V	voltage

V_c	VCO control voltage, LF output voltage
V_p	output voltage of LF's proportional path
V_z	output voltage of LF's integration path
v_{lf}	loop filter output voltage noise
y	admittance
z	impedance
Z	impedance, transimpedance
Z_{lf}	loop filter transimpedance

Contents