High Speed Computer and Algorithm Organization

Edited by

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Urbana, Illinois

ACADEMIC PRESS, INC. New York San Francisco London 1977

A Subsidiary of Harcourt Brace Jovanovich, Publishers

The material was prepared with the support of National Science Foundation Grant No. MCS 76-10823. However, any opinions, findings, conclusions, or recommendations expressed herein are those of the author(s) and do not necessarily reflect the views of NSF.

ACADEMIC PRESS, INC.
111 Fifth Avenue, New York, New York 10003

United Kingdom Edition published by
ACADEMIC PRESS, INC. (LONDON) LTD.
24/28 Oval Road, London NW1

Library of Congress Cataloging in Publication Data

Symposium on High Speed Computer and Algorithm Organization, University of Illinois, 1977.
High speed computer and algorithm organization.

1. Electronic digital computers—Congresses.
2. Algorithms—Congresses. I. Kuck, D. J.
II. Lawrie, Duncan Hamish, Date III. Sameh, Ahmed.
IV. Title.

QA76.5.S95 1977 001.64'4 77-14236
ISBN 0-12-427750-0

PRINTED IN THE UNITED STATES OF AMERICA

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Preface

The Symposium on High Speed Computer and Algorithm Organization was held on April 13–15, 1977, in Champaign, Illinois. It was sponsored by the University of Illinois, Department of Computer Science, in cooperation with the IEEE Computer Society and the ACM, SIGARCH, and SIGNUM, with support from the National Science Foundation. About 50 papers were presented covering high speed computer design, high speed algorithms, the software, and the performance of such systems. With the exception of the paper presented by Robert Johnson, which is not available for publication, the present volume contains long or short versions of all the papers presented at the symposium.

Our original motivations for proposing such a symposium were to attempt to capture the state of the world of supercomputers and their performance in the 1970s. It has been twenty years since the design of the IBM STRETCH, ILLIAC II, UNIVAC LARC, ATLAS, etc.; fifteen years since the design of the CDC 6600; and ten years since the design of the CDC STAR, Burroughs ILLIAC IV, and TI ASC. What are the present trends and what might the future hold?

The recently announced CRAY-1, Burroughs BSP, and the redesigned CDC STAR all indicate that supercomputer developments will continue. The availability of large-scale integrated circuits including microprocessors, large semiconductor memory chips, etc., indicates that there may be some new and interesting tradeoffs in the design of such systems. On the other hand, the programming and development of software for large systems is always a problem, as is the understanding of algorithms that fit well with new machine organizations.

Our hope was that this symposium would bring together workers from the hardware, software, and algorithm areas (a fairly rare event) and lead to a proceedings volume that would reflect these three aspects of high speed computation. Since all three aspects are crucial for the success of a computer system, we felt that such a volume would be useful for practitioners as well as students of high speed computer system design and use. We invited 13 papers and selected the remaining ones from a much larger number of submitted papers.

The papers can be partitioned under three headings:

(1) computer system design and theory,
(2) numerical algorithms, and
(3) system, software, and algorithm performance.

This book is divided into these three sections and within each section the papers are organized as follows. First, the invited papers are presented,

followed by long contributed and then short contributed papers. Within each of these categories, we tried to arrange the topics from general to specific discussions or from simple machines to more complex, although in a number of cases a somewhat arbitrary ordering was used.

The success of the symposium and the final form of this book has been shaped by a number of people to whom we are indebted. First, the program committee consisted of S. Fernbach, M. J. Flynn, J. Gary, C. W. Gear, and J. Ortega. John Lehmann of the NSF provided much help as did the publisher. Ed Kalb of the Office of Continuing Education at the University of Illinois carried out much of the symposium planning. A list of referees appears at the end of the book; we are much indebted to all of them for their insightful and prompt work. We are grateful to J. N. Snyder for his welcoming remarks, and the session chairmen: R. M. Brown, E. W. Davis, Jr., E. Davidson, J. B. Dennis, F. Dorr, M. J. Flynn, M. Franklin, D. Gajski, D. Heller, J. Lehmann, C. L. Liu, D. McIntyre, D. Mickunas, J. Robertson, and D. Slotnick. Most importantly, the final form of the book was shaped by Mrs. Vivian Alsip; we are very grateful to her for her careful and devoted help.

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I

Computer System Design and Theory

IT'S REALLY NOT AS MUCH FUN BUILDING A SUPERCOMPUTER AS IT IS SIMPLY INVENTING ONE

N. R. Lincoln
Control Data Corporation

At least one segment of the computer milieu seems to be awash with creative genius these days. The advent of "cheap", "dense", "high-speed" circuit technology has made it possible for just about everyone in the business to become a "supercomputer" architect. Readers of "trade journals" are constantly titillated by the potential of "a mass of minis", or "a melange of micros". The range of application of new LSI parts seems limitless when employed in building a super processor of the 100-1000 megaflop (millions of floating point operations per second) category. For those who have been privileged (or cursed) to participate in the genesis, production and delivery of what are loosely called super-computers, the current rage of optimism and naivete about such projects is disconcerting.

Perhaps it might be useful to provide the prospective producers and consumers of this "new wave" of supercomputer horsepower with some of the insights gained over the past fifteen-plus years of large scale machine developments. The point to be made by this is that not only is there a great gap in time, money and resources between the "inventing" and the "doing", but there are many risks to be assumed by manufacturer and customer alike when dealing with advanced technologies and architectures.

PREMISES

1. There will be a continuing need for computers of the "supercomputer" class (1000-5000 "megaflops" in 1985).
2. The realization of such computers will be governed by the same economic and engineering considerations that have dominated past efforts.

3. Parallelism in data handling, control and computation will be needed to achieve the supercomputer goals.
4. Reliability, maintainability and system integrity must meet standards exceeding those commonly met by 1977 standard product medium-scale computer systems.
5. Programmability (the ability to quickly and efficiently map an algorithm onto a given machine) of any new supercomputer will be a preeminent concern of almost all users.

LESSONS LEARNED

The history of supercomputer developments (from the manufacturers' point of view) has taught us a few things about:

1. The effects of technology,
2. Software interaction,
3. The human element.

1. Technology

The design of the CDC 6600 began originally in 1960 and ended abruptly in the summer of 1961. Technology wasn't yet ready to match the vision of the chief architect. Not only did major features such as large memory (131K), long word (60 bits), and an ensemble of peripheral processors (PPU's) dominate the direction of the project, but the performance goal for an interregister transfer to be completed in 200 nanoseconds was an absolute requirement. With a hardheaded and singleminded engineer/architect in charge this meant that the semiconductor art of that time would have to be stretched until circuit technology yielded a device capable of meeting the performance goals. The first such effort, requiring a symphysis of circuit design and transistor technology, failed Thus resulted a hiatus in the summer of 1961 as the chief designer awaited a new birth at "silicon valley" to give him the tools to meet a 100 nanosecond clock speed.

The fact that a new circuit was successful with a second attempt in a few short months indicates the incredibly dynamic environment at the silicon vendor's plant at that time, and more significantly, the chief architect's ability to assess the probable state-of-the-art and match it to his

concept for a supercomputer.

Lesson I

Most supercomputers are conceived around a set of compromises between what is desired and what is possible, with the final specification usually requiring some extension of the extant technology beyond its comfortable limits. At the moment of their conception, few supercomputers were built with standard off-the-shelf parts, since speed requirements generally demanded aggressive developments in circuit performance (with little regard to cost and power dissipation), packaging and circuit interconnect. What is needed at such a time is a modicum of ESP and the ability to make judicious choices in selecting the technologies to be employed. Among the considerations that affect such choices are:

a. The state of development and maturity of a given technology at project inception versus the expected state of that technology at the time the computer is being mass produced and delivered. (What we have here is a restatement of the "learning curve", wherein we want to guess the best possible time and the best possible version to grab and run with to build a supercomputer);

b. The vendor ability or willingness to build the technology for us. (Low volumes, high start-up costs and high manufacturing skill requirements are characteristic of this breed of technology);

c. The probability that the technology will achieve high volume usage by other customers, thus ensuring alternate vendors long-term product availability, reduced costs and greater reliability due to the ability to select from larger volumes of devices.

Having conquered the circuit speed problem, it was still necessary to deal with the packaging of the devices. Two major objectives had to be achieved:

a. Reduction of the delay between circuits;

b. Increased density to permit the packing together of multiple functional elements. (Increased density also reduces the transit time across chassis of logic.)

The creation of the "cordwood" package provided the needed system with resistors providing the connective tissue between opposed circuit boards. Higher circuit density not

only meant higher speeds however, but also higher power densities. The problem of evacuating 3 watts of power from a collection of logic in about 8 cubic inches was not inconsequential. Freon cooling, once established as the means for removing this heat, challenged the mechanical design team of the 6600 as much as the manufacturability of the tightly knit "cordwood" package.

Lesson II

Circuit design and system architecture are only pieces in a large puzzle called "Supercomputer CPU." A major limitation on the feasibility of a given supercomputer project could well be the mechanical, power, packaging and cooling requirements of the overall electronic design. The physical space necessary to surround high performance circuits with heavy bus bars and cooling coils or air plenums may, in fact, be so great as to make the computer physically too large to install in any installation short of the Grand Canyon, or to power or to cool short of submergence in the waters of Hoover Dam.

Once it became clear that several copies of the CDC 6600 were going to be sold, consideration for long-term manufacturability and maintenance became highly important. Reducing circuit interconnect delays works against freely accessible logic (for maintenance and construction purposes). Certain tradeoffs have to be made, of course, but in the long run, supercomputers have emphasized performance over the manufacturing processes. It is alleged that many of the present supercomputer proposals, while highly ingenious and efficient, may in fact be unmanufacturable with processes commonly used in the 1970's.

Early installation experience with any breed of supercomputers has, almost as a matter of tradition, yielded discomfitting degrees of reliability and stability. To a degree, in the past such behavior has been acceptable for the "first-of-its-kind" computers. Since many states-of-the-art are usually being stretched along the way, customers have to contend with "first batch" parts, and not-quite-mature technology. Although this risk has always been present in any initial super procurements, the actual effects have not been realistically assessed in some instances.