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Automated Inspection and High Speed Vision Architectures

Michael J. W. Chen, Rolf-Juergen Ahlers
Chairs/Editors

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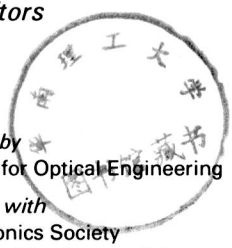

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AUTOMATED INSPECTION AND HIGH SPEED VISION ARCHITECTURES

Volume 849

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AUTOMATED INSPECTION AND HIGH SPEED VISION ARCHITECTURES

Volume 849

INTRODUCTION

This third conference on automated inspection in the annual symposium on Advances in Intelligent Robotics Systems was again a successful international conference with excellent participation. The conference name has been changed from Automated Inspection and Measurement to Automated Inspection and High Speed Vision Architectures, reflecting our current focus on high speed vision methodologies and applications. More than thirty papers from nine countries are included in this proceedings.

There are four sessions in this proceedings. High Speed Sensing and Processing Architectures is the subject of the first session, covering CCD sensors to specialized architectures. Sequential and Parallel Vision Algorithms is the topic of the second, with emphasis on algorithms for various architectures and system implementations. The third session deals with Real-Time Cost-Effective Implementations for Computer Vision, illustrating some real-time vision systems and implementation techniques. The final session is Integrated System Design, addressing various cases of industrial applications and the engineering concepts in their system integrations.

We wish to thank the program committee for their assistance in inviting and selecting some of the excellent technical papers. I have felt most delighted to have been associated with the series of conferences on Advances in Intelligent Robotics Systems. Finally, I hope that readers will find the papers in this proceedings a useful resource and also share our enthusiasm in providing the information exchange on the subject of automated inspection and high speed vision architectures and applications.

Michael J. W. Chen
AITech International Corporation

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AUTOMATED INSPECTION AND HIGH SPEED VISION ARCHITECTURES

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High Speed Sensing and Processing Architectures

Chair
Michael J. W. Chen
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CCD Image sensors for high speed inspection systems

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Abstract

Automatic industrial visual inspection systems require high speed video output and the ability to discern fine detail under an extreme range of illumination conditions. In particular the field of robotic vision requires high speed readout rates in order to process very large volumes of data in real time.

A new CCD image sensor technology (DYNASENSOR™ CCD technology) has been developed which provides a very wide dynamic range and can discern fine spatial detail with light contrast ratios of greater than a million. This technology has been applied to the realization of linear and area high speed image sensor arrays. Further, these image sensors do not exhibit saturation effects and are free of blooming even at extremely high illumination levels.

The basic high speed photoelement will be described and its theory of operation will be presented. For high speed this photoelement can operate in the conductive or integration mode. The transient analysis of the device will be described. This photoelement, which can be used to form linear arrays, will be compared to a conventional photodiode operating in the integration mode. Architectures of high speed linear image sensor arrays will be discussed.

Fabricated silicon high speed low noise linear image sensors of various lengths (128x1 and 1024x1) which employ the DYNASENSOR CCD photoelement as well as random access array will be described. These arrays are low noise devices with noise equivalent electrons at room temperature of 50 to 150 electrons. Effective horizontal video data rates of 250 to 400 MHz can be achieved if the detector is configured in a linear tapped architecture. The basic photoelement, which makes use of an optimized ion implanted doped profiled channel region can detect variations in light intensity on an object of over seven orders of magnitude. This is 10^3 to 10^4 better than any reported CCD image sensor array. The typical noise equivalent power of these arrays is less than 10^{-10} W/cm^2 at a wavelength of 0.632 μm which is ideally suited for industrial applications.

1. Introduction

There are two major modes of operation of n^+-p photodiodes. The conductive mode and the integration mode. Photodiodes operating in the conductive mode have an initial transient period before they reach their equilibrium state. The duration of this period is dependent on the incoming light level as well as on the photodetector capacitance. At low light levels a conductive mode detector is typically slower than the integrating mode detector; response time is typically on the order of milliseconds. Generally, to obtain fast transient response an integrating mode detector such as a photodiode is preferred. The major disadvantage of integrating mode detectors is its limited dynamic range and the time required to transfer the information out of the photodetector. The DALSA DYNASENSOR CCD photoelement is unique in that it permits ultra wide dynamic range operation in addition to fast transient response to low energy light signals. For comparison purposes, the standard photodiode will be presented initially, followed by the novel DYNASENSOR CCD photoelement [1,2,3,4].

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2. Standard Photodiode operating in the integration mode

A standard photodiode operating in the integration mode [5] consists of an n^+ - p junction where its n^+ diffusion is set to a positive potential and then left to float. This creats a depletion region at the beginning of the integration period. The photodiode then integrates by collecting photogenerated electrons for a frame period. (A frame consists of video data collected and stored by the entire array of photodetectors during one integration period. One frame period is also the length of time it takes to transfer all the video data from the entire array to the output.) An integrating photodiode collects photogenerated electrons which it stores on its reverse bias capacitance. As the photogenerated electrons are collected the potential across the depletion layer of the diode decreases; at the same time its depletion layer width also decreases. The decrease of the potential across the diode is proportional to the incoming light intensity and the integration time [5]. At the end of the integration period, the collected photogenerated electrons from the n^+ diffusion are transferred into the CCD transport shift register of the image sensor.

3. The DYNASENSOR CCD photodetector

The DYNASENSOR CCD photodetector is a new high performance photodetector used in applications requiring CCD linear and area arrays for high speed, wide dynamic range and low noise.

This new photodetector consists of a photodiffusion, an adjacent optimized ion implant doped profiled channel region and a positively biased drain diffusion. This is shown in Figure 1.

Photodiffusion leakage current and the flow of current over the profiled channel region into the drain diffusion are both functions of the photodiffusion potential. The photosensing diffusion potential decreases as the illumination level increases. With an increase in photodiffusion potential, the leakage current increases quadratically and the profiled channel current decreases exponentially. Under dark illumination, the photodiffusion reaches a potential where the diode leakage current and the profiled channel current become equal. Under illumination, electron-hole pairs are generated at the photodiffusion resulting in a dominant electron current flow in the same direction as the diode leakage current. During illumination, in order to maintain an equal current flow into and out of the photocollection node, the photodiffusion potential falls, increasing the profiled channel current exponentially. The exponential dependency of the profiled channel current and the photodiffusion potential yields the logarithmic dependency of the DYNASENSOR's output voltage with light.

The spectral response of a silicon DYNASENSOR CCD photoelement is similar to that of a silicon n^+ -p photodiode. However, the present new photoelement can be designed to provide an improvement of spectral response in the blue spectral region. A typical responsivity (without the presence of blue enhancement improvement) curve as a function of the incident wavelength is shown in Figure 2.

3.1 Transient Response

The response time of any photodetector is a major consideration when dealing with high speed inspection systems. The first region of operation is entered when the incident light level is low. Low light levels correspond to radiation energies close to the NEE of the detector. The second region of operation is entered when the incident light level is much higher than the photodetector NEP. In this region of operation the incident light level has sufficient energy to cause the DYNASENSOR CCD photoelement to reach its equilibrium state.

As the incident light intensity increases the voltage across the n^+ photosensitive region of the photoelement decreases. Upon application of incident light the photoelement voltage decreases. The profiled channel current increases with the increasing light level to the point where it becomes equal to the photogenerated current. The time required to reach this steady state value depends on the incident light intensity and the n^+ node capacitance.

Upon removal of the incident light, the voltage across the n^+ diffusion of the photoelement increases. The profiled channel current eventually decreases to the point where it becomes equal to the photodiffusion dark leakage current. The time necessary to reach this point is a function of the initial photoelement voltage and the n^+ node capacitance.

The two most significant parameters affecting the response time are the magnitude of the photogenerated current and the detector photocollection n^+ node capacitance. A simplified equivalent circuit of the DYNASENSOR CCD photoelement is shown in Figure 3. The transient time for turn-on and turn-off of light pulses is the time it takes for either the profiled channel current or the dark leakage current to charge or discharge the photoelement capacitance, respectively. Then the two currents become equal. In both cases, current is flowing in all sources as shown in Figure 3. In a complete analysis all current sources must be considered.

When the incident light does not have sufficient energy (i.e. at low light intensity or with a short duration light pulse) the detector does not have enough time to reach its equilibrium state. However, the detector still responds to light and approximates its operation to that of an integrating mode detector. That is, at low light levels the voltage of the n^+ region of the photoelement continuously decreases almost linearly with incident light. This contrasts the previous situation, where there is sufficient light energy, the detector reaches its equilibrium state relatively fast. In this latter case the voltage on the n^+ diffusion is logarithmically dependent on the incoming light intensity.

3.2 Dynamic Range

The dynamic range is normally defined as the ratio of the maximum to minimum incoming detectable light intensity. With integrating mode detectors such as the conventional photodiode, the dynamic range is determined by the charge storage capability of the CCD readout shift registers at the high end and the noise level of the image sensor at the low end. The conventional method used to improve dynamic range in these arrays is to increase the shift register charge storage capability. At the low end, noise reduction techniques are used through temperature control or complex analog signal processing techniques. To achieve a dynamic range of 50,000 and assuming two hundred noise equivalent electrons, a charge storage capability of 1.0×10^7 electrons would be required. In order to accommodate this amount of charge, unrealistic shift registers channel widths would be required. Therefore, with an integrating mode detector it is difficult to achieve dynamic range over four orders of magnitude of input light intensity.

Another method of increasing the dynamic range is to improve the operation of the photodetector as opposed to increasing the charge storage capability of the shift register. DALSA's DYNASENSOR CCD technology utilizes an optimized, ion implant doped, profiled MOSFET photodetector specifically designed for wide dynamic range. When this new detector operates at high speed and at low light levels, photons are collected and stored in an integrating fashion. However, at bright light levels where transient periods are short, the detector switches into a conductive mode. The light intensity is logarithmically compressed into small charge packets, easily carried by the CCD shift register. As a result of the logarithmic conversion, dynamic ranges of over six orders of magnitude are obtained. Experimental results of the output voltage of the photodetector as a function of incident light intensity are shown in Figure 4. Here, seven orders of dynamic range is clearly evident. The wavelength of the incident light for this measurement was 0.632 μm.

4. Linear Image Sensor Architectures

There are three major types of linear image sensor architectures [6] with which the DYNASENSOR CCD photoelement can be used. Each has specific applications to which it is well suited. The major criteria used when determining the best suited architecture for an application are simplicity, total number of photoelements, centre to centre spacing and minimum frame period. The latter is the longest array readout period which can be tolerated in a given application.

4.1 Straight Architecture

The straight architecture, shown in Figure 5, is the simplest of the three. It offers a single serial output and standard input and output structures. Limitations of this architecture are centre to centre spacing and its long readout time (minimum frame period). The minimum centre to centre spacing is dictated by the minimum CCD element length, rather than the DYNASENSOR photoelement pitch. As the number of photodetectors increase, the number of CCD shift register stages increase on a one to one basis, causing the minimum frame period duration to increase. For example, given a 1024 linear photoelement array multiplexed with a CCD readout shift register and operating at a clock frequency of 10MHz, the minimum frame period duration is 102.4 μs.

Improvements have been made in the technology used for the CCD readout shift registers. Our profiled buried channel CCDs provide increased fringing fields between the gates which improves the charge transfer efficiency and clock speed to more than 20 MHz. In our developed image sensor arrays charge transfer inefficiencies of 10^{-5} have being experimentally observed. Using the increased speed of operation of the CCD, in the above example the readout period is reduced to 51.2 μs. In such CCD devices the signal charge while it is being transferred, resides in the bulk of the silicon and away from the SiO_2 - Si interface; this eliminates surface state noise. In order to further reduce the noise of the overall array, a buried channel MOSFET technology is used to realize the output video amplifier. It is important to note that these technological improvements are not restricted to the straight architecture but apply to all architectures with which the new photoelement is used.

4.2 Bilinear Architecture

The bilinear architecture shown in Figure 6, consists of two readout shift registers placed above and below the photoelements; each shift register has its own output video amplifier [7]. In applications where two separate video outputs is not a limitation, a bilinear architecture is preferred over the straight architecture. In the bilinear scheme the centre to centre spacing is improved by a factor of two since the even photoelements feed their signal into one of the readout shift registers, while the odd detectors feed their video signal into the second CCD readout shift register. As a result, the photodetector pitch can be reduced to half the CCD shift register pitch, this is an attractive feature of this architecture. An equally important additional advantage of this scheme is the availability of the video signal from each CCD shift register channel. When the video signal of this two separate channels is multiplexed externally, the output video rate is increased beyond 40MHz. A 1024 photoelement bilinear array with a CCD clock frequency of 20 MHz offers an overall readout time of only 25.6 μs.

Some bilinear architecture imager sensors combine both the even and odd outputs into one output at the end of the two shift register channels. In this scheme the two output channels are combined into one in the correct sequence with the use of an on-chip additional CCD shift register. In this case the latter shift register is required to operate at twice the clock frequency of the readout shift registers. This arrangement has the advantage of eliminating the need of an off-chip multiplexer. The disadvantage of this scheme is that the maximum video rate is limited by the speed of the output multiplexing shift register. In this architecture if the maximum clock frequency of operation of the CCD shift registers is 20 MHz it would limit the array readout time to 51.2 μs.

In our developed bilinear CCD image sensor arrays the readout shift registers can operate at more than 20 MHz clock rate. These arrays have separate low noise output amplifiers and can provide an overall readout time of better than 25.6 μs.

4.3 Tapped architecture

Our developed tapped array architectures [8] are significantly different from both the straight and bilinear architectures; one of our high speed tapped array schemes is shown in Figure 7.

On a tapped array architecture, outputs are located at periodic intervals along the photodetector array. This has the significant advantage of reducing the minimum frame duration by a factor equal to the number of outputs. On a 1024 element array with eight tapped outputs, each operating at 20 MHz yields a minimum frame duration of 6.4 μs. This would correspond to an effective output video rate of 160 MHz. Shorter frame durations can be achieved by reducing the total number of detectors in the linear array. For example, a 128 element array with eight outputs yields a minimum frame duration of 800 ns. The number of outputs can be increased further to reduce the frame duration; however, the total power dissipation of the image sensor increases with each additional separate on-chip video amplifier output.

5. Random Access Image Sensor Arrays

The DYNASENSOR CCD photoelement can also be configured into both linear and area random access arrays. The advantage of this architecture is that the location of important video data can be quickly determined, accessed and processed without waisting time on non relevant video data. This is very important in robotic applications where large volumes of data must be manipulated at high speed.

A linear array random access device consists of a single decoder which receives the address input and then selects the transfer of video data from a single detector into the output circuit. In this case the access time is much shorter than the readout time of the linear image sensor arrays. The area array random access architecture consists of both vertical and horizontal input address decoders which select a single photoelement out of the entire array, and then transfer its video signal to the output within a short access time. This results in a user selected output sequence.

6. Other Applications

Figure 8 shows a photomicrograph of our developed quad logarithmic wide dynamic range photodetector. In this application the basic photoelement is a DYNASENSOR. The output voltage of each of the four channels is logarithmically dependent on the incident light intensity. The photodetectors do not saturate or bloom [4].

7. Noise

In order to determine the minimum number of detectable photons by our linear arrays, a low noise analysis was performed and noise measurements carried out.

Detailed studies have been carried out at DALSA to identify and determine the nature of fundamental noise sources in buried channel CCD imaging arrays [9]. The noise sources are as follows.

Starting with the DYNASENSOR CCD photodetector, the predominant noise source is KTC noise. KTC noise is caused by random thermal motion of electrons in the photosensitive diffusion (Johnson noise). This noise source is a function of the photosensitive diffusion capacitance.

Moving along the signal path of the image sensor, the next noise component is associated with bulk state traps within the CCD transport shift register. Fortunately, since surface channel CCDs are not used, a previously predominant noise source, surface state noise, has been eliminated. Also associated with the shift register is the random thermal generation of dark leakage current. This component is a function of the length of time the charge is within the shift register as well as the physical volume of the charge packet. In our profiled buried channel CCD readout shift registers we minimized the dark leakage noise source.

Finally, there are two noise components associated with the output section of the image sensor. The first is KTC noise of the charge sensing floating diffusion node, a function of the node capacitance. The second component is the thermal Johnson noise of the output amplifier which is dependent on the transconductances of the associated MOSFETs and the bandwidth of the amplifier.

Typical amount of noise equivalent electrons contributed by each significant source of noise at room temperature in one of our early arrays are as follows:

(i) KTC noise of the output sensing diffusion of the CCD shift register is 46 electrons;

(ii) KTC noise of the wide dynamic range photodetector due to the capacitance of the sensing diffusion is 45 electrons;

(iii) bulk state trapping noise in the buried channel CCD shift register is 37 electrons;

(iv) dark leakage current noise of the buried channel CCD shift register is 3 electrons;

(v) output amplifier noise is 80 electrons.

The total noise is the geometric sum of the above and it comes to 109 electrons.

8. Conclusion

The DYNASENSOR CCD photoelement used in linear and tapped array architectures has been shown to offer high speed operation suitable for industrial inspection systems requiring wide dynamic range. In addition the use of low noise profiled buried channel CCD and buried channel MOSFET technologies offer high speed and low noise. The new DYNASENSOR CCD photoelement can be used in random access image sensor arrays. Such image sensor area arrays offer high speed and low noise. User selectable and dynamically changeable data sequences are all additional attractive features.

9. Acknowledgments

The authors would like to thank P.T. Jenkins for reading the manuscript and other contributions. Technical discussions with N.D. Prince were useful. D.G. Bedrosian contributed to the clock circuitry. J.R. Campbell packaged the devices. The contributions of Dr. James Robar are also appreciated.

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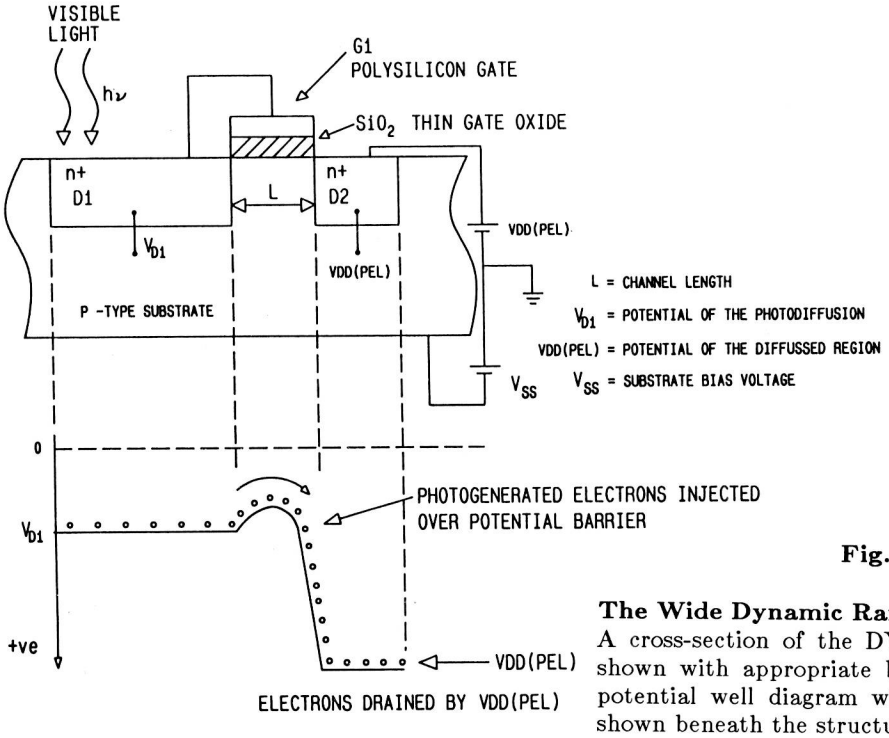

Fig. 1.

The Wide Dynamic Range DYNASENSOR:
A cross-section of the DYNASENSOR photodetector structure is shown with appropriate bias voltage sources. The corresponding potential well diagram with the profiled channel current flow is shown beneath the structure.

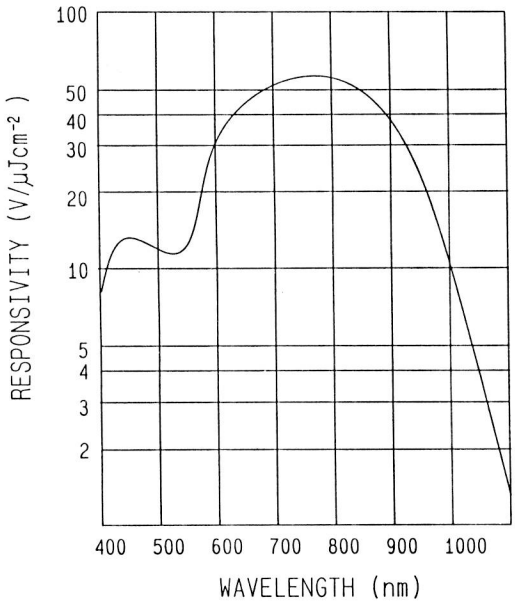

Fig. 2.

Responsivity vs. Incident Light Wavelength:
Typical experimental responsivity curve of a DYNASENSOR as a function of wavelength.

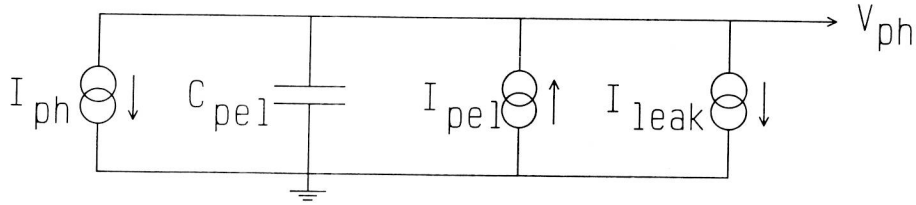

Fig. 3. **An Equivalent Circuit of the DYNASENSOR Photodetector:** A simplified equivalent circuit of the DYNASENSOR photodetector is shown with current sources corresponding to the photogenerated current (I_{ph}), the profiled channel current (I_{pel}) and the diode leakage current (I_{leak}) along with the detector collection node capacitance (C_{pel}). The output voltage V_{ph} is logarithmically proportional to the incident light intensity.

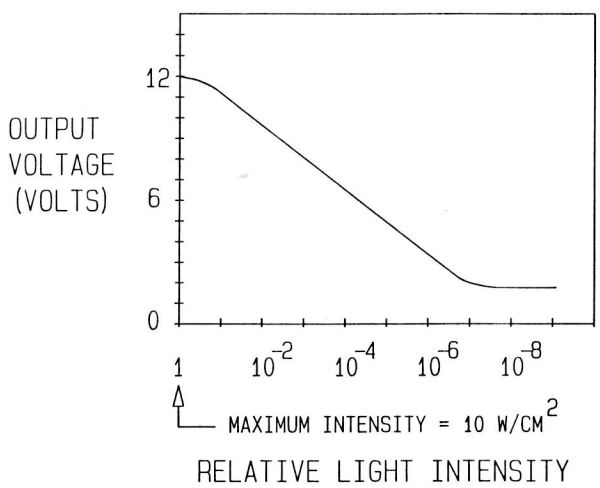

Fig. 4.

Output Voltage vs. Incident Light Intensity:
The output video voltage as a function of the incident light intensity of a linear array using the DYNASENSOR CCD photoelements.

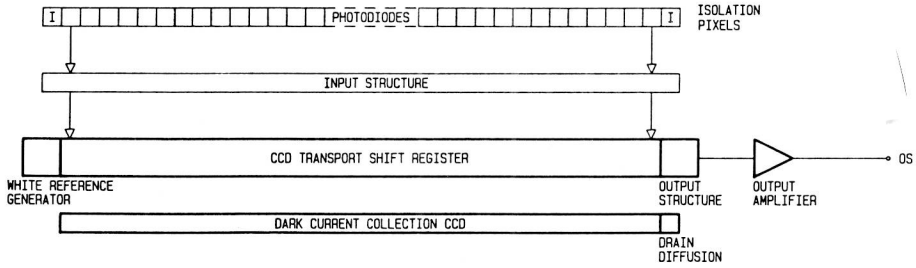

Fig. 5. A Straight Architecture Linear Photodiode Array:
A standard linear array is shown, it consists of one CCD readout shift register and a single output amplifier.

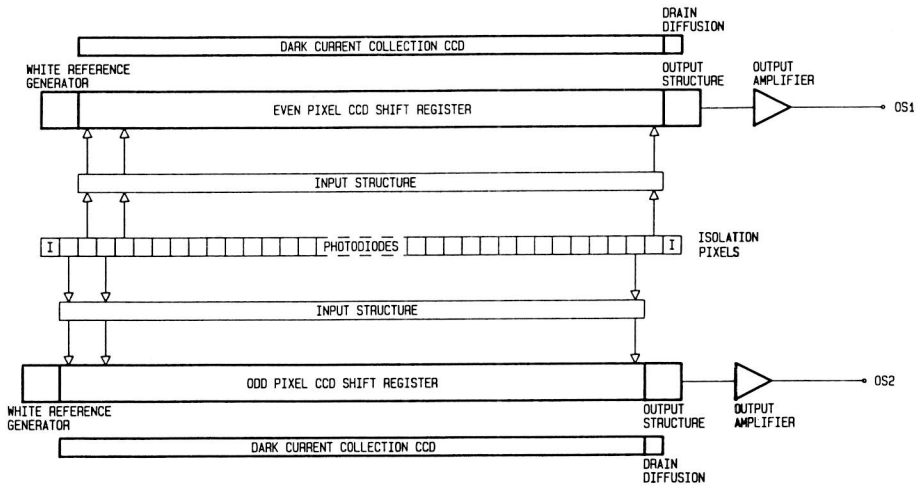

Fig. 6. A Bilinear Architecture Linear Array:
A standard bilinear architecture linear array is shown, it consists of even and odd transport CCD shift registers and two output amplifiers.

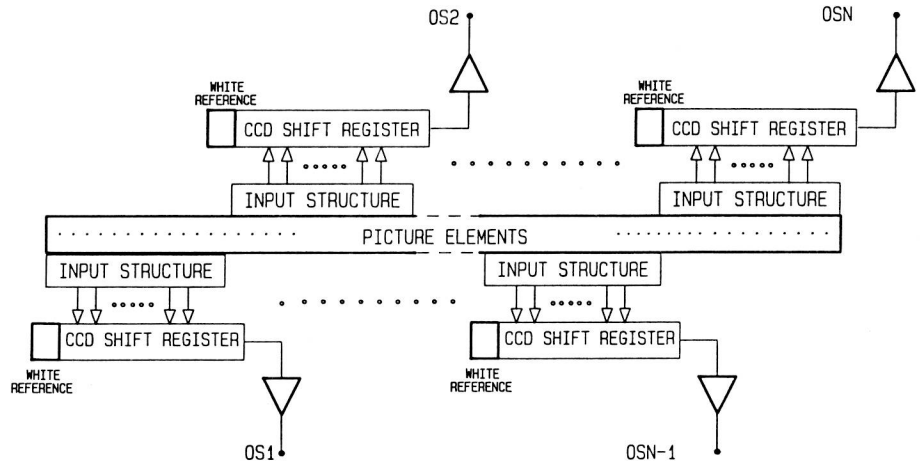

Fig. 7. A High Speed Tapped Architecture Linear Array: A standard tapped architecture linear array with N outputs is shown. By operating the outputs in parallel, very short array readout times are possible.

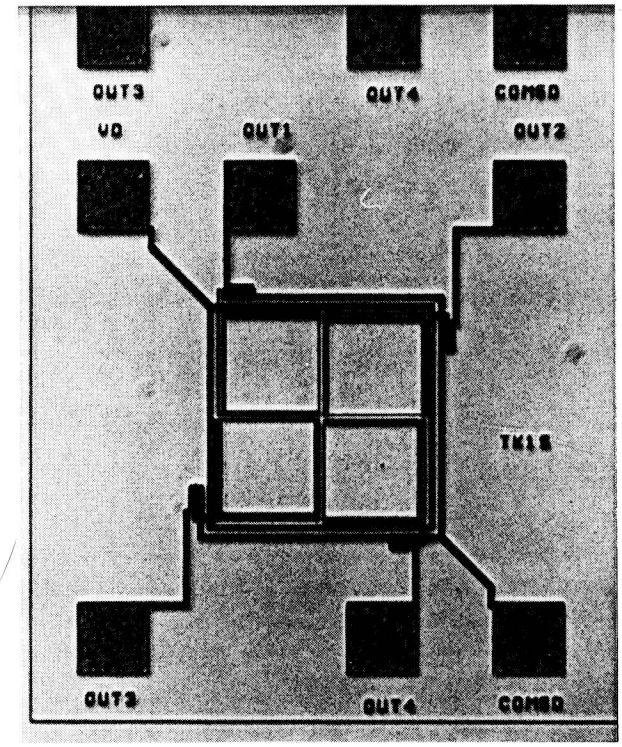

Fig. 8. A Quad Logarithmic Photodetector: A photomicrograph of a quad logarithmic photodetector using DYNASENSOR CCD photoelements.