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Transactions on High-Performance Embedded Architectures and Compilers I

Per Stenström
Editor-in-Chief

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Editorial Board

Editor-in-Chief's Message

It is my pleasure to introduce the first volume of *Transactions on High-Performance Embedded Architectures and Compilers*, or *Transactions on HiPEAC* for short. *Transactions on HiPEAC* is a new journal which aims at timely dissemination of research contributions in computer architecture and/or compilation methods for high-performance embedded computer systems. Recognizing the convergence of embedded and general-purpose computer systems, this journal intends to publish original research and surveys on systems targeted at specific computing tasks as well as systems with broader application bases. The scope of the journal, therefore, covers all aspects of computer architecture as well as code generation and compiler optimization methods of interest to researchers and practitioners designing future embedded systems. Examples of topics of interest include:

- Processor architecture, e.g., network and security architectures, application-specific processors and accelerators, and reconfigurable architectures
- Memory system design
- Power, temperature, performance, and reliability constrained designs
- Evaluation methodologies, program characterization, and analysis techniques
- Compiler techniques for embedded systems, e.g, feedback-directed optimization, dynamic compilation, adaptive execution, continuous profiling/optimization, back-end code generation, and binary translation/optimization
- Code size/memory footprint optimizations

Journal publications are usually associated with a significant delay between submission and final publication. *Transactions on HiPEAC* will rectify this by seriously cutting down on manuscript handling time. The time to the first response will not exceed ten weeks. If minor revisions only are requested, the goal is to publish such papers within six months. Articles that are requested to undergo a major revision will be requested to be resubmitted within three months. Articles that are accepted will immediately be available electronically. By the end of each year, a printed volume will be published by Springer.

In This Volume

First, I am very delighted that Sir Maurice Wilkes accepted to write the leading article of the first volume of the journal. Having contributed to our field ever since the beginning of the electronic computer era, he has an unprecedented broad perspective of the exciting evolution of computers to the point that we know them today. In his leading article, which is partly based on the keynote address he contributed to the first HiPEAC summer school (ACACES 2005), Prof. Wilkes shares with us his reflections on the evolution in computer architecture over the

last few decades. He also provides his outlook on the forces that will be important over the next decade. His article appears as the first regular paper in this volume.

An important deliverable for the HiPEAC Network of Excellence is a roadmap of the challenges facing high-performance embedded architectures and compilers. The HiPEAC community has put together a roadmap along ten themes that highlights the research challenges we are faced with in the next decade. I'm pleased that the roadmap appears in this volume. It is the second regular paper.

Apart from publishing regular papers, *Transactions on HiPEAC* will sometimes publish papers on special topics or highlights from conferences. This volume contains three such specialized themes organized into three parts: Part 1, Part 2, and Part 3. Part 1 is devoted to the best papers of the 2005 International Conference on High-Performance Embedded Architectures and Compilers (HiPEAC 2005). Part 2 is devoted to the topic of optimizing compilers and is edited by Mike O'Boyle, University of Edinburgh, Francois Bodin, IRISA, and Marcelo Cintra, University of Edinburgh. Finally, Part 3 is devoted to the best papers on embedded architectures and compilers from the 2006 ACM International Conference on Computing Frontiers and is edited by Sally A. McKee, Cornell University. Organizing specific themes in this journal will be a recurring activity in the future and I encourage prospective guest editors to propose themes for future volumes.

Finally, I have been fortunate to engage a set of distinguished members of our community to form the first editorial board. It is my pleasure to introduce this set of fine people.

Per Stenström
Chalmers University of Technology
Editor-in-chief
Transactions on HiPEAC

Editorial Board

Per Stenström is a professor of computer engineering of Chalmers University of Technology and a deputy dean of the IT University of Göteborg. His research interests are devoted to design principles for high-performance computer systems. He is an author of two textbooks and 100 research publications. He is regularly serving program committees of major conferences in the computer architecture field as well as actively contributing to editorial boards: He has been an editor of *IEEE Transactions on Computers* and is an editor of the *Journal of Parallel and Distributed Computing* and the *IEEE Computer Architecture Letters*. Further, he served as the General as well as the Program Chair of the ACM/IEEE Int. Symposium on Computer Architecture. He is a member of the ACM and the SIGARCH, a Fellow of the IEEE, and a founding member of the Network of Excellence in High-Performance Embedded Architectures and Compilation Methods funded by the European Commission.

Koen De Bosschere obtained his PhD from Ghent University in 1992. Currently, he is research professor at the engineering school of the same university where he teaches courses on computer architecture and operating systems. He is the head of a research group of 20 researchers and has co-authored 150 contributions in the domain of optimization, performance modeling, microarchitecture, and debugging. He is the coordinator of the Flemish research network on Architectures and Compilers for Embedded Systems (ACES), and he is the Belgian representative of the HiPEAC network of Excellence. Contact him at Koen.DeBosschere@elis.UGent.be.

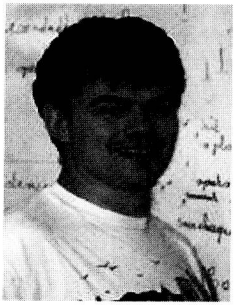
Jose Duato is Professor in the Department of Computer Engineering (DISCA) at UPV, Spain. His research interests include interconnection networks and multiprocessor architectures. He has published over 340 papers. His research results have been used in the design of the Alpha 21364 microprocessor, and the Cray T3E, IBM BlueGene/L, and Cray Black Widow supercomputers. Dr. Duato is the first author of the book "Interconnection Networks: An Engineering Approach". He served as associate editor of IEEE TPDS and IEEE TC. He was General Co-chair of ICPP 2001, Program Chair of HPCA-10, and Program Co-chair of ICPP 2005. Also, he served as Co-chair, Steering Committee member, Vice-Chair, and Program Committee member in more than 55 conferences, including HPCA, ISCA, IPPS/SPDP, IPDPS, ICPP, ICDCS, Europar, and HiPC.

Manolis Katevenis received his PhD degree from U.C. Berkeley in 1983 and the ACM Doctoral Dissertation Award in 1984 for his thesis on "Reduced Instruction Set Computer Architectures for VLSI". After a brief term on the faculty of Computer Science at Stanford University, he is now based in Greece, with the University of Crete and with FORTH since 1986. After RISC, his research has been on interconnection networks and interprocessor communication. In packet switch architectures, his contributions since 1987 have been mostly in per-flow queueing, credit-based flow control, congestion management, weighted round-robin scheduling, buffered crossbars, and non-blocking switching fabrics. In multiprocessing and clustering, his contributions since 1993 have been on remote-write-based, protected, user-level communication.

His home URL is http://archvlsi.ics.forth.gr/~kateveni

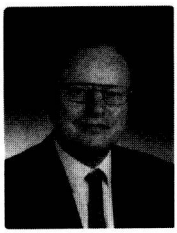
Michael O'Boyle is a Reader in the School of Informatics at the University of Edinburgh and an EPSRC Advanced Research Fellow. He received his PhD in Computer Science from the University of Manchester in 1992. He was formerly a SERC Postdoctoral Research Fellow, a Visiting Research Scientist at IRISA/INRIA Rennes, a Visiting Research Fellow at the University of Vienna and a Visiting Scholar at Stanford University. More recently he was a Visiting Professor at UPC, Barcelona. Dr.O'Boyle's main research interests are in adaptive compilation, formal program transformation representations, the compiler impact on embedded systems, compiler-directed low-power optimization and automatic compilation for parallel single-address space architectures. He has published over 50 papers in international journals and conferences in this area and manages the Compiler and Architecture Design group consisting of 18 members.

Cosimo Antonio Prete is Full Professor of Computer Systems at the University of Pisa, Italy, and a faculty member of the PhD School in Computer Science and Engineering (IMT), Italy. He is Coordinator of the Graduate Degree Program in Computer Engineering and Rector's Adviser for Innovative Training Technologies at the University of Pisa. His research interests are focused on multiprocessor architectures, cache memory, performance evaluation, and embedded systems. He is an author of more than 100 papers published in international journals and conference proceedings. He has been project manager for several research projects, including: the SPP project, OMI, Esprit IV; the CCO project, supported by VLSI Technology, Sophia Antipolis; the ChArm project, supported by VLSI Technology, San Jose, and the Esprit III Tracs project.



André Seznec is "Directeur de Recherches" at IRISA/INRIA. Since 1994, he has been the head of the CAPS (Compiler Architecture for Superscalar and Special-purpose Processors) research team. He has been conducting research on computer architecture for more than 20 years. His research topics have included memory hierarchy, pipeline organization, simultaneous multithreading and branch prediction. In 1999-2000, he spent a sabbatical with the Alpha Group at Compaq.

Olivier Temam obtained a PhD in computer science from University of Rennes in 1993. He was Assistant Professor at the University of Versailles from 1994 to 1999, and then Professor at the University of Paris Sud until 2004. Since then, he has been a senior researcher at INRIA Futurs in Paris, where he heads the Alchemy group. His research interests include program optimization, processor architecture, and emerging technologies, with a general emphasis on long-term research.



Theo Ungerer is Chair of Systems and Networking at the University of Augsburg, Germany, and Scientific Director of the Computing Center of the University of Augsburg. He received a Diploma in Mathematics at the Technical University of Berlin in 1981, a Doctoral Degree at the University of Augsburg in 1986, and a second Doctoral Degree (Habilitation) at the University of Augsburg in 1992. Before his current position, he was scientific assistant at the University of Augsburg (1982-89 and 1990-92), visiting assistant professor at the University of California, Irvine (1989-90), professor of computer architecture at the University of Jena (1992-1993) and the Technical University of Karlsruhe (1993-2001). He is a Steering Committee member of HiPEAC and of the German Science Foundation's priority programme on "Organic Computing". His current research interests are in the areas of embedded processor architectures, embedded real-time systems, organic, bionic and ubiquitous systems.

Mateo Valero obtained his PhD at UPC in 1980. He is a professor in the Computer Architecture Department at UPC. His research interests focus on high-performance architectures. He has published approximately 400 papers on these topics. He is the director of the Barcelona Supercomputing Center, the National Center of Supercomputing in Spain. Dr. Valero has been honored with several awards, including the King Jaime I by the Generalitat Valenciana, and the Spanish national award "Julio Rey Pastor" for his research on IT technologies. In 2001, he was appointed Fellow of the IEEE, in 2002 Intel Distinguished Research Fellow and since 2003 he is a Fellow of the ACM. Since 1994, he has been a foundational member of the Royal Spanish Academy of Engineering. In 2005 he was elected Correspondant Academic of the Spanish Royal Academy of Sciences, and his home town of Alfamén named their public college after him.

Stamatis Vassiliadis is currently the chairperson of computer engineering and a T.U. Delft chair professor in the Faculty of Electrical Engineering, Mathematics and Computer Science. He has also served in the ECE faculties of Cornell University, Ithaca, NY and State University of New York (S.U.N.Y.), Binghamton, NY. He worked for a decade with IBM in the Advanced Workstations and Systems laboratory in Austin TX, the Mid-Hudson Valley laboratory in Poughkeepsie NY and the Glendale laboratory in Endicott NY. In IBM he was involved in a number of projects regarding computer design, organizations, and architectures and the leadership to advanced research projects. He has been involved in the design and implementation of several computers. For his work he received numerous awards including 24 publication awards, 15 invention achievement awards and an Outstanding Innovation Award for Engineering/Scientific Hardware Design in 1989. Six of his patents have been rated with the highest patent ranking in IBM and in 1990 he was awarded the highest number of patents in IBM. While at IBM, he was awarded 73 USA patents ranking him as the top all-time IBM inventor. Dr. Vassiliadis received best paper awards at the PDCS (2002), the IEEE CAS(1998, 2001),the IEEE ICCD (2001) and honorable mention best paper award at the IEEE/ACM MICRO 25(1992). He is an IEEE and ACM fellow.

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