

Intel's Automotive Microcomputer Operation

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INTEL'S AUTOMOTIVE MICROCOMPUTER OPERATION

1.0 INTRODUCTION

Intel's Automotive Operation offers memory and microcontroller products, qualified and tested to meet automotive application requirements. The Automotive Operation draws upon Intel's leading edge technologies, including 1-micron, EPROM, and FLASH processes.

Intel's Automotive Operation is chartered to provide the customer with the most reliable product possible, to continuously improve device performance, to exceed customers' expectations, and to become the vendor of choice.

The Automotive Operation is involved in designing, manufacturing, and marketing of memory and microcontroller products for the automotive world. These products are primarily used to control the engine and transmission, the braking system, the suspension, power steering, instrumentation and audio systems, as well as communications between the different systems.

The automotive products perform both analog and digital signal processing in extremely harsh environments which demand the highest levels of quality and reliability. The expected lifetime for automotive products is twenty years or more. Special consideration must be taken in design and manufacturing to meet these requirements. Testing of automotive products extends beyond that of commercial products. It is because of these unique requirements that Intel has developed specialists in Automotive applications, design, and quality and reliability.

2.0 AUTOMOTIVE PRODUCTS

2.1 Memories

The Automotive Operation offers a wide range of memory products. These include, ROMs, EPROMs, QROMs, OTP, and FLASH memory products available.

MASKED ROMs

Masked ROMs are the least flexible memory product because they can be programmed (wafer implant) only once during wafer fabrication. They typically come in low cost plastic packages and are suited to high volume applications.

EPROMs

Erasable Programmable ROMs are more flexible than ROMs because they allow the user to program the device and to reprogram the device if necessary by erasure with ultraviolet light. They are available only in ceramic packages which are much more expensive than plastic packages. EPROMs are most suited for development work.

QROMs

Quick-ROMs are EPROM die in a plastic package programmed only once by Intel. The advantage is shorter TPT than a ROM but at a cost closer to a ROM than an EPROM.

OTPs

One time programmable devices. Essentially a QROM programmed by the end user, hence even shorter TPT than a QROM. The disadvantage is that the memory can not be verified for data retention by Intel.

FLASH

Similar to an EPROM but with the ability to be erased electrically rather than by ultraviolet (UV) light. Advantages are that the contents of the memory can be updated by the end user from remote locations with the device in the system.

Memory products are used to qualify new processes and packages. Because the failure mechanisms for memories are very well understood allowing for rapid failure analysis during the qualification procedure. For a new process qualification, the lead qualification vehicle would be a memory in a ceramic package followed by a memory in a plastic package. This flow is used as ceramic packages are more reliable than plastic packages and allow for faster failure analysis should failures occur.

2.2 Microcontrollers

Testing and failure analysis of microcontrollers is considerably different than memories. An exact failing mechanism is very difficult to identify in a random logic device. Thus, the certification process for a random logic device relies heavily on the data collected using memory devices on the same process and fault grading for each transistor's functionality. A typical microcontroller qualification would share data from the memory product qualification wherever applicable (e.g. lifetest data). Additional stress test data would be collected to ensure there are no package related failure mechanisms.



3.0 CERTIFICATION PHILOSOPHY

3.1 Qualifications

3.1.1 INTRODUCTION

New Intel products undergo a Product Qualification process as a way to address quality and reliability. Product Qualification is a confirmation that the product meets and will continue to meet Intel's quality and reliability standards over time. Continuous improvement is also embraced via the multi-level certification steps, as customer requirements and improving product/process capabilities change.

The quality and reliability data base is established with a lead product on a new process and package. The lead product/process/package combination constitutes the driving force for the continuous improvement of the intrinsic reliability through process in-line and end-of-line monitors.

The follow-on product qualification focuses on verifying that the product has no reliability or quality problems. Confidence in the intrinsic reliability performance comes from the lead product; the follow-on products are treated in a modular approach.

3.1.2 PRODUCT QUALIFICATION LEVELS

There are four levels of product qualification, with Level-IV being the initial milestone. Beyond this product entry gate, the levels allow intelligent qualification methodology and systematic engineering decisions. Interlocking qualification phases provide flexibility with control and discipline. These levels apply to both new and modified products. Figure 1 shows the flow of qualification levels.

Qualification Levels	Product Status			
Level-IV	Product Market Entry- Prototype Samples			
Level-III	Limited Qualification Data- Limited Shipments			
Level-II	Complete Qualification Data-Unlimited Shipments			
Level-I	Continuous Improvement Stage			

Figure 1

Level-IV: This level represents the entry of a product into the market to meet a customer's design and prototyping needs. This level is not intended for volume shipments. A limit on shipments is defined (typically 3K units) to contain risks due to minimal certification data. Customers are not advised to perform any qualifications on Level-IV units.

Level-III: The product reaches this level as quality and reliability data is acquired and/or substituted. Limited data on the product, and justifiable data substitution from other products increases the confidence that Intel's high quality and reliability standards are not being compromised. Shipments are limited (typically 21K units) during this confidence building phase.

Level-II: The product has completed both internal and generic customer data requirements. The product meets/exceeds all stated quality and reliability objectives. On reaching Level-II qualification, unrestricted volume shipments are allowed. A Product Qualification summary report is published at this phase.

Level-I: The product/process is fully characterized and is in statistical control. There are no intrinsic problems with the design; additional design stepping changes will not be made. The electrical test program has no changes anticipated. All known test holes and errata have been fixed or an approved plan is in place. Continuous improvement is driven through the ongoing improvement phase through Fab, Assembly, Test, and Customer feedback.

3.1.3 PRODUCT QUALIFICATION STRESS REQUIREMENTS

All quality/reliability data requirements are to be specified in the product Quality/Reliability Validation (QRV) plan that is published prior to data acquisition. What follows is a brief description of the major reliability stresses and data acquisitions for lead and follow-on products. Additional stresses not mentioned may be performed based on customer request. The data requirements are divided into four areas:

- a. Operating Life Failure Rate Evaluation
- b. Environmental Stresses
- c. Steady State Stresses
- d. Special Tests

3.1.3.a. Operating Life Failure Rate Evaluation

This evaluation assesses the operating life failure rate (the bathtub curve) of a given product. The data, in turn, will assist our customers in calculating the failure rate of their systems. The stresses used for this purpose are: Burn-In (B/I), Extended Life Test (ELT), High Voltage Extended Life Test (HVELT), and the Low Temperature Extended Life Test (LTELT). Burn-In is



done to measure and screen out infant mortality. ELT at 125°C, 5.25V to 5.5V, accelerates failure mechanisms and measures Failure rate In Time (FIT). HVELT at 125°C with a higher V_{CC} voltage (typically 6.5V to 7.0V) further accelerates voltage dependent failure modes (Electromigration, oxide defects). The LTELT at low temperature of -10° C with high V_{CC} may be done to evaluate hot electron trapping problems.

LEAD PRODUCT: The Operating Life Failure Rate Evaluation is an essential requirement to identify any process or design problems for corrective action in the early days of a product. This data establishes the failure rate and the required production burn-in time. On a lead product these stresses are also used to measure failure rates at different V_{CC} voltage levels to establish an intrinsic data base for a given process. Reduction of burn-in (ROBI) duration is achieved as the process matures and monitors show a progressively declining fallout.

FOLLOW-ON PRODUCT: A 100% Burn-In will be required of a follow-on product in its infancy. The Burn-In duration is set by the lead product. The failure rate curve for each product is established. Any failures beyond the intrinsic rate established by the lead product may be due to product design. The Design problems should be detected early and corrected to bring the failure rate to the intrinsic level. If this does not happen, the follow-on product will be treated as a lead product.

3.1.3.b. Environmental Stresses

These stresses are designed to test the mechanical or operational integrity and stability of the component against environmental changes. A system containing the component may be operating in hot and humid environment of the tropics or it may be used in very cold climate, resulting in temperature and humidity stresses. The reliability stresses in this group are: (1) Temperature Humidity Bias (THB), (2) Steam, (3) Temperature Cycling and (4) Thermal Shock. THB and Steam evaluate the moisture effects on the component, leading to metallic corrosion, electrical parametric shifts and package deterioration. The test read-out should be a room temp QA test only to avoid failure recovery at high temperature. Temperature cycling and thermal shock test the component for severe or sudden changes of the ambient temperature and the effects of on/off cyclic operations. A preconditioning to simulate the surface mount process for plastic packages is done before subjecting them to environmental stresses. The following paragraphs give a detailed description of each

Preconditioning Stress

Surface Mount plastic packages are subjected to a severe thermal cycle/shock by rapid rise in temperature during the surface mount assembly process. The temperature differential between the surface and the internal body of the part causes mechanical stresses. These stresses, aggravated by absorbed moisture, can cause package cracks and other effects such as bond failure. Additionally, the highly corrosive atmosphere of the solder flux will also degrade the lead finish. A preconditioning stress flow is designed to simulate the actual conditions of surface mount process.

Temperature Humidity Bias Test (85/85)

LEAD PRODUCT—This test is performed to evaluate in an accelerated manner, the resistance of the components to the deteriorating effects of high humidity and heat. These conditions cause corrosion of metal lines, bond pad degradation and detrimental changes in electrical properties. Monitoring for moisture resistance should continue on the lead/worst-case product after initial certification.

FOLLOW-ON PRODUCT—If the follow-on product uses the same general package as the lead product and its die size is equal to or smaller than that of the lead product, test data from the lead product can be substituted for ship release decision. The data and the justification for this is documented in the product QRV Plan.

Steam Test

LEAD PRODUCT—This test gives a rapid indication of die passivation or package problems as indicated by metal corrosion, electrical parameter shift, lead finish and solder plating deterioration. Steam wets the component surface during stress, as opposed to THB, which just provides a humid environment without condensation. Monitoring for steam resistance is continued on the lead/worst-case product after it is certified.

FOLLOW-ON PRODUCT—This test is done on most follow-on products since the efforts required for Steam test are relatively small and it gives significant moisture resistance data.

Temperature Cycling, Thermal Shock (T/C, T/S)

LEAD PRODUCT—The two tests are similar except that the thermal shock is sudden. Both test for mechanical resistance of the component against temperature changes. The temperature changes during testing tend to simulate the changes in environment as well as the heating and cooling produced by the intermittent operation of the component. Both T/C and T/S are done for lead product certification, while the T/C only is sufficient for a follow-on product.

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FOLLOW-ON PRODUCT—For hermetic package, the data substitution from a lead product is applied if the follow on product uses similar die size and generic package. A justification for such use is documented and made a part of the product QRV plan. However, T/C evaluation is done on all follow-on products using a plastic package to check for design sensitive thin film failure modes.

3.1.3.c. Steady State Life Tests

The shelf life of a component is an important characteristic besides its operating life. Bake accelerates degradation due to aging of the component. High Temperature Reverse Bias (HTRB) is another stress type where a reverse bias is applied during bake. HTRB is often used during process certification but can be used for product certification for special situations.

Bake/High Temperature Reverse Bias

LEAD PRODUCT—Bake at 250°C is needed to certify hermetic packages only. It is an accelerated storage test and also indicates contact failures. It is also a test for EPROM data retention.

FOLLOW-ON PRODUCT—The certification data from the lead product is used for a follow-on product, unless it is significantly different and would justify a separate bake. The use of the lead product data is justified and documented in the QRV plan.

3.1.3.d. Special Tests

This is a group of specialized tests of diverse nature which are evaluated during product certification. The failure modes indicated by these are dependent on the process/design/assembly of a product. Since they are of diverse nature, they are grouped under Special Tests.

Electro-Static Discharge (ESD)

All components are designed to withstand normal amounts of electrostatic discharge during assembly, test

and handling. Intel uses two ESD standards, the human body model (Military standard) and the charged device model. Intel's Technology Development Group develops standard I/O structures and design guidelines for the Design Engineers to follow.

Latch-Up (LU)

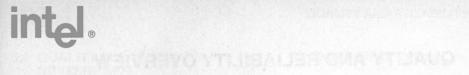
Latch-up is caused by turning on the parasitic PNPN structure in CMOS circuits, due to a noise pulse, junction breakdown, or power supply power transient overshoot. This will cause the circuit to malfunction temporarily or go into a destructive mode. Latch-up immunity is built into a component by proper process design and layout design rules. Latchup, unlike ESD can be tested during the product testing in production. Like ESD, Latchup is verified during the DV efforts. Once a product is confirmed to have adequate latch-up immunity level this test is needed only in the final QA test program to monitor any abnormal process shifts.

Electromigration (EM)

Electromigration is a phenomenon of mass transfer mainly created by electron drag force. This causes metal thinning or voids leading to functional failure. For a given process EM is controlled by limiting the current density in the circuit metal lines.

EPROM Program/Erase Endurance

The data stored in a EPROM can be erased by UV light and written again. The floating gate is charged by the injection of hot electrons during each write operation. Some of these electrons get trapped in the gate oxide during each cycle. This build up of trapped charge gradually increases the device threshold and reduces injection effeciency, resulting in non-functional EPROMs after a number of program-erase cycles. This test measures the number of these cycles.



Quality and Reliability Overview

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1.0 QUALITY/RELIABILITY IN DEVELOPMENT

1.1 Introduction

The Quality and Reliability (Q & R) organization has subgroups whose main responsibilities are to support Intel's development efforts. This development work involves new fabrication technologies, new assembly processes, new packages and new product designs. As these development areas vary greatly, so do the requirements for the Q & R group supporting them. There are three main areas of expertise in the O & R subgroups: fabrication process reliability, assembly process/package reliability, and product reliability. These O & R groups are responsible for working with their particular development teams to ensure that quality and reliability issues are addressed early in the development cycle. The goal is to be proactively involved, so the impact to introduction schedules and customer expectations is minimized

1.2 Certification Philosophy

Manufacturability Emphasis

One of the main improvements in performing new process, package or product certifications is that we are now focusing on and articulating new requirements for manufacturability as well as the previous quality and reliability requirements. These manufacturability requirements cover both the design and execution aspects of the manufacturing system. There are a number of indicators that can be used to determine manufacturability: critical-step process control capability, line yield, die yield, in-line and end-of-line monitors, and many more. Adding these manufacturability requirements has resulted in a more cooperative effort on general problem-solving between the Q & R and engineering development groups.

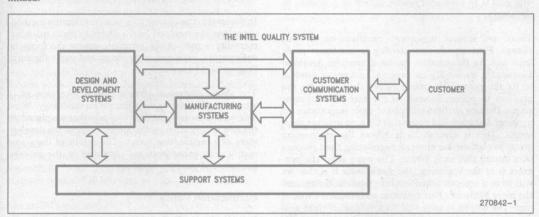


Figure 1-1. Intel Quality System Diagram



The goal of all certifications is to produce a reliable and manufacturable product. In the past the emphasis has been on resolving reliability issues during the qualification exercise and resolving manufacturability issues after the product was in production. With this change in certification methodology, the manufacturing issues have to be resolved during the certification. The end result is that issues are resolved early in the process, where the impact to the program schedule and to customer's expectations is minimal. This leads us to our next reason for the methodology change.

Proactive Engineering Emphasis

Under the old qualification methodology, problems periodically showed up late in the development cycle. Invariably, these delayed production introductions, affected customer commitments, and created crises for the development team. In order to improve this situation, the new certifications are designed to emphasize proactive engineering early in the development cycle. The goal is to push every issue, actual or potential, to the source.

These are several important ramifications of this change. First we are now striving to anticipate problems and fix the product before a problem develops. Essentially, we modify the process, package or product to fix the potential problem rather than wait for the problem to occur. Second, in the early development stages, the new certification places more importance on problem detection and resolution than on product shipments. This is critical, as it allows the engineering group to concentrate more on engineering than production during this early phase. The more solid the program is in the beginning, the more likely it is that we will have a smooth transition into manufacturing, and the more likely it is that customer commitments will be met. The emphasis on a smooth introduction into production leads us to the next reason for changing the certification methodology.

Continuous Information Emphasis

In the past, qualifications were run on a fixed number of production lots. If they met the reliability requirements, the product, process or package was qualified. Then the production line would be ramped. Since Engineering was still working with the process to address the then current manufacturing issues, there was always the possibility that the qualification samples were not fully representative of later material. This problem, along with the need to make manufacturability as important as reliability in the certification process, forced a change in the way we approached these certifications.

The change we made was to perform continuous certifications. Material from the very first fabrication runs on package builds is now put into the same stresses or tests that are called for in the certification. The idea is to start gathering information as quickly and as continuously as possible. Early material is usually changing lot to lot or build to build. It is during this time period that we strive to gather reliability and manufacturability data on every lot. As the manufacturing stabilizes, change slows down as does the need to gather certification type data from every lot or build. Ideally, in some time interval, the gathered data satisfies the reliability and manufacturability certification requirements.

Executing such a certification approach is non-trivial. For new processes and packages, particularly the newer, large-die, state-of-the-art packages and processes, this approach works very well. Since early material is generally scarce, trying to do a traditional qualification would result in serious program delays. For these products, continuous certification is the only way we can bring these into production.

In summary, the change to a new certification methodology was the result of Intel's desire to make manufacturability a part of the program, renew the focus on anticipatory, proactive engineering and make the certification effort continuous.

The above discussion gives a general overview as to why Intel changed its certification methodology. What follows are the internal requirements that we placed on the new certification methodology through the development of a certification policy. The details of the actual certification procedures are discussed in the process, package and product sections.

Certification Policy

In order to develop a certification procedure that valued manufacturability and reliability equally, insured proactive engineering and was a part of our continuous quality improvement process, several things had to happen. First, we needed a certification policy. The policy had to spell out requirements for both manufacturability and reliability. It had to specify a number of pre-silicon engineering activities, and it had to require that they occur as early in the development process as possible. The goal was to promote proactive engineering.

The last part of the policy was more difficult since the term "continuous certification" would mean many things to many people. This was resolved by developing a four-level certification procedure. It was similar to the Set Qual, Conditional Qual and Full Qual of old, with specific requirements for going from level to level. But it also promoted a continuous improvement approach to the certifications, since one moved from level to level by demonstrating better manufacturability and reliability.



There were other requirements to the certification policy. Internally, we wanted the four levels to be consistent among the process, package and product. We wanted to make sure that each of the four levels, independent of what was being certified, had to have requirements for manufacturability, reliability, quality, change control, monitors, and customer notification. Also, there had to be policy statements requiring specific pre-silicon engineering activities to drive and promote high-leverage, low-risk problem anticipation, detection and resolution. In support of the business units and our customers, there also had to be provisions for shipping material at each of the four levels. However, regardless of the certification level, the customer's requirements for accepting the product shipments had to be met.

The resulting certification policy meets all these requirements and is written in such a way as to promote continuous learning. The policy gives a structure within which the development team can easily work. But, the development team is not told which reliability exercises to run, what manufacturing indicators to track, or the exact details for the pre-silicon engineering work. There are checksheets for various areas, reliability and manufacturing requirements, and examples of every certification run to date to guide the development team. However, the team has latitude throughout the certification process so that they and the certification specifications can benefit from the quality improvement process.

Today's certifications are of very complex technologies and designs. Rarely are certification plans the same from one effort to the next. Each technology brings something unique that requires new thinking and new approaches to certification. The policy is designed to promote continuous learning in such an environment.

The actual specifications for product, process and package certifications are extensions of the policy but include greater detail and structure. They are also designed to be modified and updated to incorporate things learned from each new certification. The result is a certification policy and specifications that promote continuous personal improvement for the engineers through learning. Conversely, the engineers' learning promotes continuous improvement in the certification process through feedback and change.

Throughout Chapters 1 and 2, the concept of continuous improvement, as part of the certification process, is everywhere. It is a subtle but important point to note that certifications are processes, not tasks. The idea is that, as a process, the activity never stops; it is continuous. This contrasts with qualifications being treated as tasks. Since the emphasis of tasks is getting to the end, much of what occurs during the journey can be overlooked. By treating certification as a process, the emphasis is on the journey, where much of the continuous improvement and learning take place.

1.3 Process Development

Introduction

The development of a new wafer fabrication process is the responsibility of the Technology Development organization and its associated Reliability Engineering group. Their goal is to develop and transfer the process into production. The development activity begins with a need. A typical need is a reduction in chip cost, an increase in chip performance or an increase in chip functionality. The next step is to express the need as a set of target goals. The development team then determines how it is going to meet these goals. Since there are a number of ways to do this, the team has to determine the approach that gives the desired result while minimizing the negative impact to other variables. For example, in order to meet functionality targets, a new chip might require a die size too large to make the chip cost-effective. Or, the need to reduce costs by reducing die size, while maintaining functionality, might result in a process too complex to be manufacturable. Whatever compromises are made, the result has to satisfy an internal or external customer need, and the process has to be transferable into production.

The transfer of any process into production requires that the process be capable of hitting the target performance goals, be cost-effective and manufacturable, and meet the corporate reliability requirements. To satisfy these goals, the development activity must balance a number of complex and often competing variables (such as die size vs process complexity or manufacturability, and speed vs reliability).

Process Reliability Engineering

The Process Reliability group has the responsibility of ensuring that the new technology is inherently reliable. This goal is reached if there are no intrinsic wearout mechanisms built into the technology, the defect densities are reduced enough to allow for efficient and economical manufacturing, and the layout and circuit design rules provide sufficient margins to guarantee reliable operation throughout the lifetime of the product.

1.4 Package Development

Introduction

As silicon technology advances and more complex designs are created, there is a continuing demand for new packages and assembly processes. The performance requirements for these new packages and assembly pro-



cesses have become very complex and demanding. Electrical performance is so critical that the package's electrical parasitics have become a major factor in determining how well a device performs. A package must meet electrical requirements for inductance and capacitance in order to meet the increased speed requirements of new product designs. The need to meet the heat dissipation requirements of the larger devices is driving the development of special package designs and assembly processes with improved thermal performances. In addition, mechanical requirements are becoming more demanding and complex as end users are requiring smaller packages with increased numbers of leads.

Additionally, there are other demands on new packages and assembly processes as customer's manufacturing techniques change. One example is surface mounting, which is used for attaching the finished product to a circuit board. This technique places great demands on both thermal and mechanical package performance. Internally, there are requirements for reliability, manufacturability and cost that also impact the development of new packages and assembly processes.

Package Reliability Engineering

The package development efforts and goals are basically the same as those of the new technology development team. The goal is to produce a reliable, manufacturable product that meets our customers' needs for functionality, performance, and cost. The reliability engineer's responsibility is also the same: produce an inherently reliable product. The main characteristic associated with being inherently reliable is the same for processes and packages: no intrinsic wearout problems. The wearout issues are attacked the same: understand the failure mechanisms, learn which package or assembly process parameters affect the wearout mechanisms, learn how the product design and layout affect the wearout mechanisms, and then make the necessary changes to the package or assembly process to eliminate the wearout problem from the useful life of the finished product.

1.5 Product Development

Introduction

The development cycle for products is the same as it is for packages and processes. First, there has to be a need for a new product, or there has to be an idea for a new product that would create a demand for it. If a new product design requires a new package or a new process technology, the package or process development will include the new product in its certification plans (previously referred to as the lead vehicle). For this section, a new product refers to a follow-on product; that is, the fabrication process and the package are already certified (Level II or I) on a lead vehicle.

The development team's major goals are to design a product that meets the functionality and performance targets, doesn't create a need to modify the process or package, and has quality and reliability consistent with the lead vehicle. As with all of the development efforts discussed in this chapter, the goal is a manufacturable, reliable product that satisfies our customers' needs.

Product Reliability Engineering

The product reliability engineer has overall responsibility for the reliability of the finished product. However, most process issues are handled by the process reliability engineers, and most packaging issues are handled by the package reliability engineers. This allows the product reliability engineer to concentrate on two main areas: design and test. Another skill, unique to the product reliability engineer, is product failure analysis. This is not only useful in resolving reliability problems but also in helping the development team resolve product yield and performance issues. Additional responsibilities involve making sure that special customer requirements are comprehended in the certification plans and that the customers continue to receive reliability support on the product after it is certified.

2.0 QUALITY/RELIABILITY IN MANUFACTURING

2.1 Introduction

The certification of new technologies, new assembly processes and new packages is a joint activity between the technology development teams and special subgroups in the Quality and Reliability organization (as described in the previous section). This section deals with certifications involving the transfer of previously certified processes and packages to new manufacturing sites and with certifications involving changes to existing processes and packages. These certifications are a joint activity between the Manufacturing and Quality and Reliability groups. The end result is a process or package that exceeds both internal and external customer reliability and manufacturability performance needs.

The Manufacturing Quality and Reliability (Q & R) organization has three main functions:

- Certifying all process/package changes
- Monitoring existing processes/packages
- Low yield analysis

The main emphases of the Q & R group are on continuous improvement, protecting the end user, and protecting the factory.



2.2 Process and Package Certification Philosophy

The Quality and Reliability (Q & R) organization's role in supporting manufacturing continues throughout the lifetime of the process. Once new processes and packages are developed and certified as reliable and manufacturable, all subsequent changes are controlled, with emphasis on reliability and manufacturability through the Manufacturing and Quality and Reliability organizations. Since all certifications have requirements for reliability and manufacturability performance, all certification exercises are a joint effort between the Quality and Reliability and Manufacturing groups.

2.3 Process Control

Fabrication and assembly processes are controlled through five major activities: in-line and end-of-line process monitors, low yield analysis, change control, and a comprehensive auditing program.

2.3.1 IN-LINE MONITORS

Manufacturing monitors are used extensively to control various fabrication and assembly processes. Each process step has a number of monitored variables. For a bonding operation they might include machine controls (power, pressure, time, frequency, etc.) and finished-product monitors (bond pulls, thermal cycling, etc.). For a photoresist development step, these variables might be equipment-related (develop volume, water pressure, spin speed, etc.) and inspections-related (amount of residual resist, levels of contamination, etc.). Anything that might impact the final product's general performance or factory flow is monitored.

The goal for all our manufacturing monitors is to operate under statistical process control (SPC). In Intel factories, SPC is more than just a method for plotting data; it is a feedback system designed to provide information to engineering and manufacturing on how processes are running so that problems can be identified and corrective action taken. When negative trends are spotted, corrective action is taken to get the process back in control. When positive trends are noted, the cause of the shift is examined to learn how it can be made a permanent part of the process and maintained under SPC. The SPC program is changing constantly as we learn which variables are most critical and as we develop corrective actions to process control excursions.

2.3.2 END-OF-LINE MONITORS

A second set of process control monitors are reliability monitors. Some reliability monitors are a subset of manufacturing monitors and are referred to as process reliability monitors. They are executed in-line or at the end-of-line in either wafer fabrication or assembly. The rest of the reliability monitors come from the reliability certification exercises. These include the fundamental wearout stresses, which are typically run on special test structures, and the environmental stresses which are used to measure reliability performance on the finished product.

The establishment of manufacturing and in-line/endof-line reliability monitors is part of the certification procedure. This means that a process or package is not certified at any of the four levels unless the critical manufacturing and reliability monitors are defined and in place.

2.3.3 LOW YIELD ANALYSIS

The third method of process control is low yield analysis. This is a reactive activity, as opposed to the primarily proactive monitoring activity. While the goal is to attain and maintain control of all process steps, the reality is that there are periodic excursions, or deviations, from a state of total control. These excursions have to be dealt with swiftly for the benefit of our customers and the factory.

The simplest type of excursion occurs when the SPC charts indicate that a situation is out of control. Affected material is usually still in the factory and can be contained or even reworked (although most process steps strive for a no-rework procedure).

The determination of what went wrong and what corrective actions are needed is not always easy. While engineering has the primary responsibility for resolving these issues, the quality and reliability organization becomes involved when the reliability of the affected material is in question. This can be a complex activity, as some process excursions do not readily appear to have an impact on product reliability. However, over time, a history of problems and their impact to device performance and reliability makes it progressively easier to handle future excursions.

Yield excursions are another action trigger. A yield excursion occurs when yields fall below their normal SPC variability. Because yield excursions greatly impact factory flow and thus affect commitments to customers, they always have a high priority.

The most critical type of excursion the quality and reliability group addresses involves end-product reliability. While SPC and yield excursions also involve product reliability, they occur early in the manufacturing cycle and usually have little end-customer impact. Product reliability excursions, on the other hand, occur on production material.

Since product monitors usually lag production by a number of weeks, a reliability excursion detected in the



product monitors is a sign that more material could be affected than just the material represented by the failing monitor lot. Therefore, reliability excursions always receive the highest priority.

While the effort to determine the cause of the problem and a corrective action is critical, there must be an equally vigorous effort made to protect the customer. Therefore, reliability problems are worked from both ends: one effort identifying and fixing the causes of the problem and the other moving the problem away from the customer and back to the factory.

Containment of such problems is not easy. Suspected material must be identified by location and isolated. Additional monitors are run to determine the scope of the problem, usually, only one or a very few lots are involved.

These monitors and the subsequent failure analysis are used to make an assessment of the reliability of the affected material. For some problems a reliability screen, such as burn-in, can be implemented to screen out the defective units. For other problems, the end user is asked to be involved in deciding the usefulness of the affected material.

Frequently, what Intel calls a reliability problem is not a problem for the end user. This is a result of many things: Intel's reliability requirements are set to satisfy the most stringent of our customers' requirements, individual customer reliability requirements vary, application reliability needs vary and our customers' customers have a variety of reliability needs. However, sometimes the reliability performance is a problem. These instances require that every effort be made to protect the customer from poor reliability while we resolve the problem internally and strive to get our affected customer commitments back on track.

Not all product reliability problems require all these efforts. It may be that the problem is contained within the factory, or that the problem has very little impact on the field failure rate (as determined with the end user), or that it is simply a false alarm. However, when a reliability excursion is found to be widespread, the Q & R group and the factory attack the problem using every available resource to isolate the cause and protect the customer.

2.3.4 MANUFACTURING CHANGE CONTROL BOARDS

A third process control mechanism is the Manufacturing Change Control Board (MCCB). The MCCB's main function is to communicate factory changes to our customers and to provide feedback to the factory on customer concerns, issues or requests with the proposed changes. It also has the responsibility for approving the changes.

While the MCCB is the main change control body for Intel, there are other change control boards that are used to control change within smaller groups but whose output is still subject to MCCB approval. These include the process change control boards (PCCBs) which each fabrication plant uses to control process changes; the division change control boards which controls design/testing changes; and the assembly change control board which controls package/materials and assembly process changes.

2.3.5 AUDITS

The fourth process control mechanism at Intel is our auditing activity. There are three types of audit programs: self-audits, internal or corporate audits, and customer/military audits. Audits help control the factory by identifying discrepancies through the use of specifications and identifying issues that might result in misprocessing.

3.0 QUALITY SUPPORT SYSTEMS

3.1 Introduction

The systems discussed in this chapter are not exclusively aimed at either Intel manufacturing or our customers but rather are basic to the concept of a total quality system. They fill the gaps between our major quality and reliability programs in design and development, manufacturing, and customer support, and serve to link these major systems as a seamless, integrated whole.

Intel support systems are divided into three categories: change management systems, quality management systems, and process control management systems.

3.2 Change Management Systems

To address customer concerns and contractual obligations with regard to process and product change control, Intel has developed an "Intelligent Multi-level Change Control System". Its purpose is to ensure that Intel customers are not adversely impacted by any Intel-generated process or product changes. This network is also responsible for ensuring that customers are given adequate notice and sufficient information to fully address any concerns caused by these changes.

3.3 Quality Management Systems

Intel's Quality Management Systems consists of an extensive auditing system and Material Review Board (MRB) activities.



3.3.1 AUDITS

Intel's extensive audit system forms a key part of our Quality Improvement Process. All Intel audits include quality evaluations conducted in the spirit of continuous improvement, as well as verifying compliance to specifications.

All audit activities at Intel include the same elements: planning, preparation, implementation, corrective action definition, continuous improvement planning, closed-loop tracking to completion, and leveraging of results across Intel.

The various types of audits and quality evaluations in Intel are summarized in Table 3-1 and discussed thereafter.

Customer Audits

The Intel Quality Audit Department acts on behalf of Intel customers to satisfy their quality management objectives and to help Intel achieve and maintain vendorof-choice status. As such, it is responsible for coordinating the scheduling, planning and execution of all customer quality system surveys and customer quality system audits at Intel.

In addition, the Quality Audit Department administers, develops and coordinates the Intel self-audit system through a distributed structure of plant auditors and self auditors that support customer audit activities.

Self-Audit System

Intel's distributed self-audit system revolves around a strong self-audit concept owned by the individual manufacturing plants and operations. The plant/operation is divided into self-audit areas by process or station. A self-audit team, comprised of various functional content experts, audits each self-audit area on a quarterly basis.

A plant auditor/coordinator administers the self-audit system in each operation, trains the self auditors, con-

Table 2-1. Intel Audit System Functions

Type of Audit	Scope/Site	Frequency	Auditors
Customer Vendor of Choice Audits	Quality Systems Audits of Intel Operations	By Customer and Plant Agreement	Customer Quality Auditors
Plant/Operation Level Self Audits	All Wafer Fab, Assembly, and Test Manufacturing Operations	Once per Quarter	Self Audit Area Teams Plant Auditors and Management
Corporate Q & R Operations Audits	All Wafer Fab, Assembly, and Test Manufacturing Operations	Once per Year	Intel Components Auditor
Corporate Contracting Audits	All Intel Wafer and Unit Contracting Operations	Once per Year	Intel Components Auditor
Corporate Military Audits	All Military/B Wafer Fab, Assembly, Test and Contracting Operations	Once per Year	Intel Military/ Components Auditor
Customer Military Audits	Military Test/Assembly Operations by Product	Per Contract Agreement	Customer Military Auditors
CSC/JAN Product Audits	All Intel Jan Wafer Fab, Assembly and Test Operations	Per Contract Agreement	Certified Jan Auditors
Internal Customer/Supplier Audits	Customer/Supplier Relationships and Processes Internal to Intel	Senior Management Initiated	Senior Manager Customer/Supplier Partners
Mr. Clean Environment Audits	All Intel Facilities	Typically Once per Quarter	Operations and Facilities Managers
Intel Supplier Continuous Quality Improvement Audits	All Direct Material Suppliers	From Six Months to Two Years by Performance	Intel Commodity and Quality Engineering Specialists



solidates corrective action plans, issues quarterly reports to the Corporate Quality Audit Department, and tracks corrective actions and continuous improvement line items to completion. These plant auditors are trained and guided by the corporate auditors and the site Q & R organization. They coordinate and host all customer quality system audits in their operation.

Factory working teams of plant, operations, and auditors meet regularly to share information and methods for leveraging audit results across Intel.

Intel's self-audit system has led to an increased level of integrity and openness about problem-reporting without fear of management punitive action. Teamwork and continuous process improvement are our goals.

Operations, Military and Contracting Q & R Audits

The Corporate Q & R Quality Audit Department, along with the Military Q & R and Components Contracting Q & R organizations, administers the Intel corporate Q & R audits. These are required at least once a year in every Intel manufacturing location, including component contractors.

The corporate Q & R audits are detailed quality system and customer and military requirement audits performed by the corporate components/military auditors. In addition, they perform a quality evaluation of the local self-audit system and its performance, examine specific items from a corporate continuous quality improvement viewpoint, and gather and share information for leveraging improvements across Intel. All Intel manufacturing locations and operations, including the components contracting operations, are included in these audits.

As part of the operations audits or in separate military audits, all Intel military manufacturing operations are audited for compliance with both customer and governmental military requirements. The Components/Military auditors act as the government auditors from the Defense Electronic Supply Center (DESC) would in verifying that all program requirements are met. Several Intel plants have been certified to produce military/B-grade product or have been certified by DESC to produce Jan product under the rigid government audit standard MIL-M-38510/XXX. The Intel auditors work closely with the local Defense Contract Administration Services (DCAS) representatives and military customers to verify that Intel meets or exceeds all federal and customer requirements for military products.

Management Quality Audits

Management quality audits are a key part of the Intel audit system. They provide management leadership and demonstrate commitment to the continuous quality im-

provement process. There are three types of management audits at Intel: management self-audits, internal customer/supplier partnership quality audits, and Mr. Clean audits.

Management Self-Audits. As part of each operation's self-audit system, the most senior management staff in each plant conducts management self-audits of their own organization. These audits typically occur quarterly and provide leadership, communication, direction, and leverage to the self-audit system in each operation.

Internal Customer/Supplier Partnership Quality Audits. These audits constitute a practical way for senior management to evaluate the quality of service between internal Intel organizations. Pairs of senior managers having a customer/supplier relationship within Intel, initiate a joint quality evaluation of their "shop floor" processes to enhance their relationship. These audits serve to identify continuous improvement opportunities and demonstrate management leadership and commitment for making the customer/supplier partnership concept part of our quality culture.

Mr. Clean Audits. From Intel's inception, a clean and disciplined work environment has been an important part of our culture. Senior managers share the role of Mr. Clean, a site-level inspector who, accompanied by facilities and building managers, regularly evaluates every Intel building for cleanliness, neatness, safety and repair status. Conditions in every area of every building are evaluated according to a common standard. A report is issued quantifying variances and assigning corrective actions. The objective is to ensure a safe, pleasant, trouble-free environment that is conducive to producing superior quality work and defect-free products.

Supplier Quality Audits

Intel depends heavily on its suppliers and expects them to have continuous quality improvement processes of their own, stressing commitment, teamwork and attention to detail. Supplier Quality Audits are conducted with all direct material suppliers, with the objective of assessing the suppliers' quality systems, process control capability, and product quality.

More complex supplier quality survey audits are conducted as part of Intel's Supplier Continuous Quality Improvement (SCQI) program described in Chapter 2. SCQI is a comprehensive partnership with key suppliers that includes a total commitment to continuous quality improvement, quality planning, statistical process control, production performance, quality data, product quality, delivery, costs and supplier quality assessment.

Supplier quality audits focus on guaranteed integrity of all materials supplied to Intel.



3.3.2 MATERIAL REVIEW BOARD

Intel's Material Review Board (MRB) is an internal quality control body that makes decisions on discrepant material, deciding whether the material will be screened, scrapped, returned to vendor or used as is. The MRB has several specific responsibilities. The first of these is to contain any materials problem so that customers will not receive discrepant material. The problem is then documented exhaustively and the discrepant material quarantined. At the same time, a recovery plan is executed to either contain the problem by screening so the material can be shipped or scrap the material and replace it with new material.

MRB membership varies with the product group and situation involved. However, representation is always required from engineering, manufacturing, Q & R, and planning organizations. Each member has the authority to make decisions for and the responsibility to obtain sign-off of his or her management. Final decisions are arrived at by overall concensus. The MRB writes a final report and distributes it. The corporate auditing group receives these reports and uses them to follow up on annual audits and quarterly self-audits.

While MRB reports are valuable for historical reference, they are also a potential source of product/process health evaluations. We regularly review these reports to assess trends which will help us continuously improve.

3.4 Process Control Management Systems

Process control management systems include statistical process control (SPC) activities, document control, calibration of measurement systems, traceability, and data systems.

3.4.1 STATISTICAL PROCESS CONTROL

Intel's commitment to total quality pervades our entire business, from product design to supplier selection, and from manufacturing to field support. As VLSI-based products have become increasingly complex, we've realized that assembly line inspections are no longer sufficient to guarantee predictable quality levels. Quality and reliability have to be designed and manufactured in from the ground up if they're going to be there at all.

Statistical Process Control (SPC) is a tool Intel uses to assure high levels of quality and reliability are achieved and maintained in all our factory areas. Intel has been developing and implementing a statistical process control program in its own factories since the early 1980s and has more recently begun implementing SPC with major commodity suppliers.

3.4.2 DOCUMENT CONTROL

Given the critical and highly technical nature of our business, the document control system has special importance. The document control system at Intel deals with the specifications that represent the cumulative technical know-how of design, development and manufacturing activities. The Document Control Department is responsible for the administration of this important system. Their responsibilities include indexing, distributing, archiving, maintenance, review and change management of documents. Document Control, however, is not responsible for the content of these documents; this is the responsibility of the technical experts.

Like the geographically dispersed organizations that it supports, the document control centers (DCs) are located at all Intel facilities. DCs are closely linked with the operations they support and report to those operations. This provides the local flexibility needed to meet organizational needs while allowing common requirements to be specified for all operations. Since key requirements do not vary across sites, customers are assured that products from all Intel facilities will exhibit the same quality characteristics.

3.4.3 CALIBRATION

Calibration is a process which compares test and measurement instruments of unknown status to well-defined standards of known accuracy to detect, eliminate by adjustment, and report any variations in accuracy or capability. It is a process verifying the operational integrity of instruments. It provides two major benefits. First, it allows confident use of instruments by minimizing the associated uncertainties. Second, it fulfills requirements for traceability to recognized national standards.

The primary function of Intel's calibration program is to ensure measured integrity of any instrument used in inspection or testing that provides quantitative or quality data concerning Intel products. The program includes all disciplines involving measurements (mechanical, electrical, electronics, and physical measurements). The policies of this program are designed to meet the requirements of MIL-STD-45662 and those of major customers. Accuracy and repeatability of measurements is assured by maintaining traceability to national standards or to naturally occurring physical phenomena.

Calibration of test or inspection equipment directly affects outgoing product quality. The calibration system must provide for the prevention of inaccuracies by ready detection of deficiencies and timely positive action for correction. Through the periodic calibration of