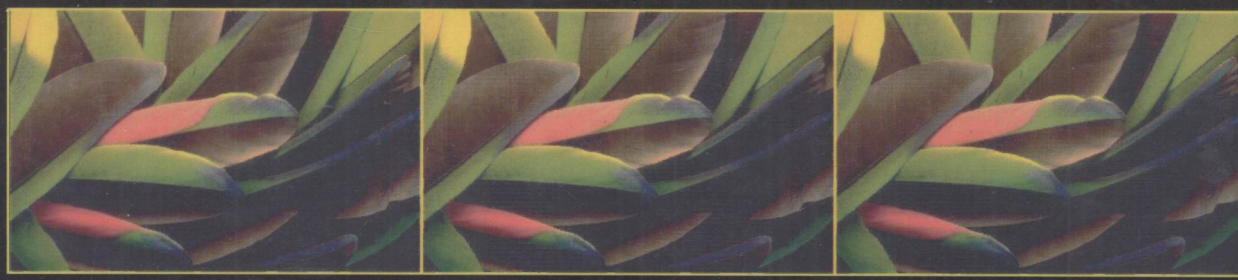
# New Developments in Computer Science Research



Susan Shannon
(Editor)

NOVA

# NEW DEVELOPMENTS IN COMPUTER SCIENCE RESEARCH

SUSAN SHANNON
EDITOR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Tele. 631-231-7269 Fax 631-231-8175
e-mail: Novascience@earthlink.net
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# NEW DEVELOPMENTS IN COMPUTER SCIENCE RESEARCH

# PREFACE

The books in this series present leading-edge research in the field of computer research, technology and applications. Each contribution has been carefully selected for inclusion based on the significance of the research to the field. Summaries of all chapters are gathered at the beginning of the book and an in-depth index is presented to facilitate access.

Digital electrical engineering is a non-formalized theory and one of the major causes of this situation consists in the complexity of Mother Nature, things cannot be completely different from those in medicine, for example. We are too restricted to finding quick solutions to the problems that arise in order to take the time to strengthen a sound theoretical foundation of the reasoning that we do. Obviously, the political, military, economical and technological importance of digital electrical engineering is itself an obstacle in the spreading of consolidated theories. In fact, the reader of such literature can remark the existing distance from the deductive theories, the way that the mathematicians use them. Chapter 1 reproduces a point of view that is considered to be representative in this direction belonging to L. Rougier: '*Reasoning is deductive or is not at all*'.

One of the most important problems of hybrid systems is the *reachability problem*. As this problem has been shown to be undecidable even for certain classes of linear hybrid systems, the main focus of the hybrid systems literature appears to be to find *effective* semi-decision procedures for this problem. Such an algorithmic approach involves finding methods of computation and representation of reach sets of the continuous variables within a discrete state of a hybrid system. In chapter 2, after presenting a brief introduction to hybrid systems and reachability problem, the authors propose a computational method for obtaining the reach sets of continuous variables in a hybrid system. In addition to this, they also describe a new algorithm to over-approximate with polyhedra the reach sets of the continuous variables with linear dynamics and polyhedral initial set. It also illustrates these algorithms with some simple and interesting examples.

Symbolic computation in algebraic categories enable the automatic modeling of modern algebra theories. On this theoretical background, chapter 3 introduces constructive and algorithmic definitions for the basic concepts (category, domain, etc.) and for a number of algebraic structures. Adopting a parameterized and object oriented approach, the categories defined for the algebraic structures will be particularized in specific domains. Chapter 3 reveals the utility of the parameterized categorical approach by deriving a multivariate polynomial category (over various coefficient domains), which is used by our Mathematica implementation of Buchberger's algorithms for determining the Gröbner basis. These

implementations are designed according to domain and category parameterization principles and underline their advantages: operation protection, inheritance, generality, natural extendibility. In particular, such an extension of Mathematica, a widely used symbolic computation system, with a new type system has a certain practical importance.

Chapter 4 directs attentions to the effects of production experiences on the R&D competition and innovations for the next generation product when the R&D knowledge is accumulated by production experiences as well as by R&D expenditure. Based on the numerical analyses of unique Nash strategies in the R&D race, we find that the challenger invests more than the incumbent, and the difference between the challenger's and the incumbent's investment rates increases with the marginal production experience (a rate at which production experiences contribute to the R&D knowledge). However, an increase in this difference is dominated by the increase in the marginal production experience itself, and thus the incumbent has a higher probability to win the R&D race at any time point (conditioned on no occurrence of innovations up to that time point) if the marginal production experience is sufficiently large. Moreover, as the marginal production experience gets higher, the rate of the overall R&D knowledge accumulation increases. The rapid innovations and the persistent leadership in CPUs for personal computers and EPROM chips may be better explained by this effects of production experiences on the R&D competition.

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*Chapter 1*

# Real Time Models of the Asynchronous Circuits: The Delay Theory

**Serban E. Vlad**
Oradea City Hall, P-ta Unirii, Nr. 1, 410100, Oradea, Romania
www.geocities.com/serban_e_vlad, serban_e_vlad@yahoo.com

## List of Abbreviations

| | | |
|---|---|---|
| SC | Stability condition | 6.1.1 |
| DC | Delay condition | 6.2.1 |
| $CC_{BDC}$ | Consistency condition (of the bounded delay condition) | 7.1.2 |
| BDC | Bounded delay condition | 7.2.2 |
| FDC | Fixed delay condition | 7.4.2 |
| AIC | Absolute inertial condition | 8.1.2 |
| AIDC | Absolute inertial delay condition | 8.2.1 |
| $CC_{BAIIDC}$ | Consistency condition (of the bounded absolute inertial delay condition) | 8.3.2 |
| BAIDC | Bounded absolute inertial delay condition | 8.4.1 |
| RIC | Relative inertial condition | 9.1.2 |
| RIDC | Relative inertial delay condition | 9.2.1 |
| $CC_{BRIDC}$ | Consistency condition (of the bounded relative inertial delay condition) | 9.3.2 |
| BRIDC | Bounded relative inertial delay condition | 9.4.1 |
| DBRIDC | Deterministic bounded relative inertial delay condition | 9.5.3 |
| BDC', AIC', RIC' | Variants of BDC, AIC, RIC | 10.1 |
| DBRIDC', SDBRIDC' | Variants of DBRIDC | 10.2.2 |

# 1. Introduction

Digital electrical engineering is a non-formalized theory and one of the major causes of this situation consists in the complexity of Mother Nature, things cannot be completely different from those in medicine, for example. We are too restricted to finding quick solutions to the problems that arise in order to take the time to strengthen a sound theoretical foundation of the reasoning that we do. Obviously, the political, military, economical and technological importance of digital electrical engineering is itself an obstacle in the spreading of consolidated theories.

In fact, the reader of such literature can remark the existing distance from the deductive theories, the way that the mathematicians use them. We reproduce a point of view that we consider to be representative in this direction belonging to L. Rougier: '*Reasoning is deductive or is not at all*'.

The consequences of non-formalization are known. Many researchers do not give the right importance to the scientific language and words like *definition*, *theorem*, *proof* are titles of descriptive paragraphs rather than having the meaning that is accepted by the logicians. A fascinating job is, in this context, the translation in a precise mathematical language of what is intuitively, imprecisely explained with natural language by the engineers and this can be done in several ways. Our work has many such examples, let's just mention here the notion of inertia that is important and confusing at the same time. By reading with a ball-point pen in our hand, we infer that the inertia's inertia is not inertia, a paradox that should end the discussion on the validity of a theory. The theoretical construction continues however, without visible implications on the subsequent results, by using the methods of the non-deductive investigations.

The purpose of delay theory is that of writing systems of equations and inequalities with electrical signals, that model the behavior of the asynchronous circuits.

The (*electrical*) *signals* are the functions $f : \boldsymbol{R} \to \{0,1\}$ where $\boldsymbol{R}$, the set of the real numbers, is the time set. We ask that they:

- be constant in the interval $(-\infty,0)$, with the variant that we have used elsewhere: be null in the interval $(-\infty,0)$, in other words 0 is the initial time instant
- be constant on intervals $[t',t'')$ that are left closed and right open
- have a finite number of discontinuity points (i.e. a finite number of switches) in any bounded interval.

The *asynchronous circuits* (also called *asynchronous systems*, or *asynchronous automata* or *timed automata* in literature) are these electrical devices that can be modeled by using signals.

The fundamental (asynchronous) circuit in delay theory is the *delay circuit*, also called *delay buffer*, the circuit that computes the identity $1_{\{0,1\}}$ and the fundamental notion is that of *delay condition*, or shortly *delay*, the real time model of the delay circuit.

We show the way that the 'inertia's paradox' has been solved. First, the definition of the delays is given. Second, the pure delays are defined. Third, all the delays different from the pure delays are considered to be by definition inertial. Fourth, the serial connection of the delays is their composition, as binary relations. The serial connection of the inertial delays results in an inertial delay, but the type of inertia is likely to differ. The bounded delays have the nice property that, under the serial connection, the delays remain bounded and thus the type of inertia remains the

same; the absolute inertial delays are in the same situation. The relative inertial delays are not closed under the serial connection, the 'paradox'.

We shall describe now, informally, the work of the delay circuit.

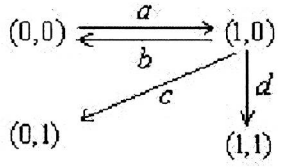



Fig 1

We have noted with $u : \boldsymbol{R} \to \{0,1\}$ its input and with $x : \boldsymbol{R} \to \{0,1\}$ its output. Both $u, x$ are signals. In Fig 1, the couples of binary numbers, temporarily called *states*, represent values $(u(t), x(t))$, with $t \in \boldsymbol{R}$ and $a, b, c, d$ are the *labels* (= the *names*) of the transitions $(u(t'), x(t')) \to (u(t''), x(t''))$. In such transitions, we suppose that $t' < t''$ and that $t''-t'$ is a small infinitesimal. A suitable notation for this is $t' = t''-0$.

The real numbers $0 < d_{r,\min} \le d_{r,\max}$ are given, the meaning of the index '$r$' being that of *raise* (switch from 0 to 1) of a signal, event symbolized by the validity of the equation

$$\overline{x(t-0)} \cdot x(t) = 1$$

Dually the real numbers $0 < d_{f,\min} \le d_{f,\max}$ are given, the meaning of the index '$f$' being that of *fall* (switch from 1 to 0) of a signal and that event is symbolized by the validity of the equation

$$x(t-0) \cdot \overline{x(t)} = 1$$

We suppose that at the initial time instant $t_0 \ge 0$ the circuit is in the initial state $(0,0)$:

$$\forall \xi \in (-\infty, t_0), u(\xi) = 0$$

$$\forall \xi \in (-\infty, t_0], x(\xi) = 0$$

This state is *stable*, meaning that the delay circuit could remain indefinitely long there, if the input is 0:

$$\forall h > 0, \forall \xi \in [t_0, t_0 + h), u(\xi) = 0 \Rightarrow x(t_0 + h) = 0$$

A switch of the input takes place at $t_0$

$$\overline{u(t_0 - 0)} \cdot u(t_0) = 1$$

and the delay circuit follows the trajectory labeled $a$, i.e. $(0,0) \to (1,0)$. The hypothesis states that both the input and the output remain constant in the interval $[t_0, t_1)$

$$\forall \xi \in [t_0, t_1), u(\xi) = 1$$

$$\forall \xi \in [t_0, t_1), x(\xi) = 0$$

and the problem is to describe the behavior of the circuit at $t_1$. Three possibilities exist, those of running one the transitions $b, c, d$, depending on the values of $t_1$ and $u(t_1)$.

$b$ : it is necessarily run at $t_1$ if $t_1 - t_0 < d_{r,\min}$ and if $u$ switches from 1 to 0 at the time instant $t_1$

$$t_0 < t_1 < t_0 + d_{r,\min} \text{ and } u(t_1 - 0) \cdot \overline{u(t_1)} = 1 \text{ and } \overline{x(t_1 - 0)} \cdot x(t_1) = 0$$

The interpretation is that the circuit's inertia did not allow a fast switch of $x$ from 0 to 1 happen.

$b, c$ : any of them is possible to be run at $t_1$ ( $x(t_1) = 0$ for $b$ and $x(t_1) = 1$ for $c$) if $d_{r,\min} \le t_1 - t_0 < d_{r,\max}$ and if $u$ switches from 1 to 0 at $t_1$

$$t_0 + d_{r,\min} \le t_1 < t_0 + d_{r,\max} \text{ and } u(t_1 - 0) \cdot \overline{u(t_1)} = 1 \text{ and } \overline{x(t_1 - 0)} \cdot x(t_1) = 0$$

$$t_0 + d_{r,\min} \le t_1 < t_0 + d_{r,\max} \text{ and } u(t_1 - 0) \cdot \overline{u(t_1)} = 1 \text{ and } \overline{x(t_1 - 0)} \cdot x(t_1) = 1$$

if $t_1 - t_0 = d_{r,\max}$ and if $u$ switches from 1 to 0 at $t_1$, then $c$ is necessary

$$t_1 = t_0 + d_{r,\max} \text{ and } u(t_1 - 0) \cdot \overline{u(t_1)} = 1 \text{ and } \overline{x(t_1 - 0)} \cdot x(t_1) = 1$$

$d$ : if $u(t_1) = 1$, then it is possible at $t_1$ for $d_{r,\min} \le t_1 - t_0 < d_{r,\max}$ and it is necessary at $t_1$ for $t_1 - t_0 = d_{r,\max}$ :

$$t_0 + d_{r,\min} \le t_1 \le t_0 + d_{r,\max} \text{ and } u(t_1 - 0) \cdot \overline{u(t_1)} = 0 \text{ and } \overline{x(t_1 - 0)} \cdot x(t_1) = 1$$

The intuitive description of the circuit continues by asking that the dual statements hold also, as resulted by the replacement of '*r*', 0, 1 with '*f*',1,0.

The circuit computes the identity on {0,1} because the states (0,0), (1,1) are stable and these are the only stable states of the circuit.

A possible manner of describing the previous facts is given by the system

$$\bigcap_{\xi \in [t - d_{r,\max}, t)} u(\xi) \le x(t) \le \bigcup_{\xi \in [t - d_{f,\max}, t)} u(\xi)$$

$$\overline{x(t-0)} \cdot x(t) \le \bigcap_{\xi \in [t - d_{r,\min}, t)} u(\xi)$$

$$x(t-0) \cdot \overline{x(t)} \le \bigcap_{\xi \in [t - d_{f,\min}, t)} \overline{u(\xi)}$$

and this might seem not quite obvious for the moment.

The chapter is organized in sections, numbered with 1, 2, 3, ... the sections have several paragraphs: 2.1, 3.2, ... and the paragraphs are usually organized in subparagraphs: 2.1.1, 4.5.2, ... The important equations and inequalities have been numbered, as well as all the figures and tables. The notation 3.2 (2) refers to equation or inequality (2) of paragraph 3.2 (that has no subparagraphs, in this case) and the notation 4.1.2 (3) refers to equation or inequality (3) of the subparagraph 2 from the paragraph 4.1.

In Section 2 we give several examples of models for the sake of creating intuition and this is a presentation of our intentions. The theory starting with Section 3 is supposed to be self-contained.

In Section 3 we fix some fundamental concepts and notations on the $\boldsymbol{R} \to \{0,1\}$ functions.

Section 4 defines the signals and gives some useful properties on them.

In Section 5 we present the informal definitions of the delays, with long quotations from several authors.

The sections that follow represent the core of this chapter. In Section 6 we define the delays, as well as their determinism, order, time invariance, constancy, symmetry and serial connection. Section 7 is dedicated to the bounded delays and in Sections 8, 9 we define and characterize the absolute and the relative inertial conditions and delays. Section 10 shows some variants of the concepts from Sections 7, 8, 9 and introduces a special form of deterministic delays. Section 11 closes the chapter with new examples and a generalization.

We thank in advance to all those that will want to bring corrections and improvements to our results.

# 2. Motivating Examples

## 2.1 Example 1: The Delay Circuit

The symbol of the delay circuit is the next one

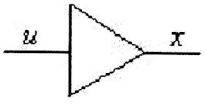



Fig 2

We consider different possibilities of modelation of this circuit, a way to anticipate the facts that will be presented later. $u, x$ are $\boldsymbol{R} \to \{0,1\}$ functions and moreover they are signals, with constant values for any $t < 0$.

**SC** *Stability*[1] (*unbounded delays*) If $u$ is of the form

$$u(t) = u(t) \cdot \chi_{(-\infty,t_0)}(t) \oplus u(t_0) \cdot \chi_{[t_0,\infty)}(t)$$

then $x$ is of the form

$$x(t) = x(t) \cdot \chi_{(-\infty,t_1)}(t) \oplus u(t_0) \cdot \chi_{[t_1,\infty)}(t)$$

where $t_0 \geq 0, t_1 \geq 0$ and $\chi_{(\ )} : \boldsymbol{R} \to \{0,1\}$ is the *characteristic function*.

**BDC'** *Upper bounded, lower unbounded delays* $d_r > 0, d_f > 0$ exist so that the next system is satisfied:

$$\bigcap_{\xi \in [t-d_r,t)} u(\xi) \leq x(t) \leq \bigcup_{\xi \in [t-d_f,t)} u(\xi)$$

**BDC** *Bounded delays* $0 \leq m_r \leq d_r, 0 \leq m_f \leq d_f$ exist and the system is the next one

$$\bigcap_{\xi \in [t-d_r,t-d_r+m_r]} u(\xi) \leq x(t) \leq \bigcup_{\xi \in [t-d_f,t-d_f+m_f]} u(\xi)$$

---

[1] In the abbreviations that we use: SC, BDC,... the letter 'C' comes from 'condition': stability (condition), bounded delay (condition),...

**FDC** *Fixed delays* (*ideal delays*) The relation between $u$ and $x$ is, for $d \geq 0$

$$x(t) = u(t-d)$$

**AIC** *Absolute inertia* $\delta_r \geq 0, \delta_f \geq 0$ exist so that $x$ satisfies

$$\overline{x(t-0)} \cdot x(t) \leq \bigcap_{\xi \in [t, t+\delta_r]} x(\xi)$$

$$x(t-0) \cdot \overline{x(t)} \leq \bigcap_{\xi \in [t, t+\delta_f]} \overline{x(\xi)}$$

This inertia condition is added to one of SC, BDC', BDC, FDC.

**RIC** *Relative inertia* $0 \leq \mu_r \leq \delta_r, 0 \leq \mu_f \leq \delta_f$ are given so that

$$\overline{x(t-0)} \cdot x(t) \leq \bigcap_{\xi \in [t-\delta_r, t-\delta_r+\mu_r]} u(\xi)$$

$$x(t-0) \cdot \overline{x(t)} \leq \bigcap_{\xi \in [t-\delta_f, t-\delta_f+\mu_f]} \overline{u(\xi)}$$

are satisfied. Similarly with absolute inertia, relative inertia is a request added to one of SC, BDC', BDC, FDC.

**DBRIDC** *Deterministic bounded relative inertial delays* If in BDC+RIC $\mu_r, \delta_r, \mu_f, \delta_f$ coincide with $m_r, d_r, m_f, d_f$ the system takes the special deterministic form

$$\overline{x(t-0)} \cdot x(t) = \overline{x(t-0)} \cdot \bigcap_{\xi \in [t-d_r, t-d_r+m_r]} u(\xi)$$

$$x(t-0) \cdot \overline{x(t)} = x(t-0) \cdot \bigcap_{\xi \in [t-d_f, t-d_f+m_f]} \overline{u(\xi)}$$

**SDBRIDC'** *Symmetrical deterministic upper bounded, lower unbounded relative inertial delays*, version of DBRIDC consisting in the next equation

$$Dx(t) = (x(t-0) \oplus u(t-0)) \cdot \overline{\bigcup_{\xi \in (t-d, t)} Du(\xi)} \cdot \chi_{[d, \infty)}(t)$$

where

$$Dx(t) = \overline{x(t-0)} \cdot x(t) \cup x(t-0) \cdot \overline{x(t)} = x(t-0) \oplus x(t)$$

is the left derivative of $x$.

All the solutions of BDC', BDC, FDC, DBRIDC, SDBRIDC' satisfy $x(0-0) = u(0-0)$ and some of the previous systems satisfy also supplementary *conditions of consistency* (i.e. the existence of a solution $x$ for any $u$).

## 2.2 Example 2 Circuit with Feedback Using a Delay Circuit

In the circuit from 2.1, Fig 2 we suppose that $u = x$ and this corresponds to the next circuit

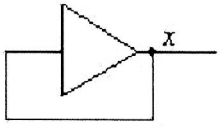



Fig 3

**SC** The satisfaction of SC does not bring any information on $x$, as it consists in a tautology of the form $\neg A \vee A$, where the proposition $A$ is the equation

$$\exists t_0 \geq 0, x(t) = x(t) \cdot \chi_{(-\infty,t_0)}(t) \oplus x(t_0) \cdot \chi_{[t_0,\infty)}(t)$$

Interpretation: the circuit can be stable or unstable.

**BDC'** The system is

$$\bigcap_{\xi \in [t-d_r,t)} x(\xi) \leq x(t) \leq \bigcup_{\xi \in [t-d_f,t)} x(\xi)$$

with $d_r > 0, d_f > 0$. Let $t_0 \geq 0$ so that $\forall t < t_0, x(t) = 0$. Because $\bigcup_{\xi \in [t_0-d_f,t_0)} x(\xi) = 0$, we get $x(t_0) = 0$. Similarly, let $t_0 \geq 0$ so that $\forall t < t_0, x(t) = 1$. Because $\bigcap_{\xi \in [t_0-d_r,t_0)} x(\xi) = 1$, we obtain $x(t_0) = 1$. $t_0$ was arbitrary previously, so that the only solutions of BDC' are the constant functions.

On the other hand, the constant functions satisfy any supplementary inertial condition AIC, RIC because $\overline{x(t-0)} \cdot x(t) = x(t-0) \cdot \overline{x(t)} = 0$.

**BDC** We have the system

$$\bigcap_{\xi \in [t-d_r,t-d_r+m_r]} x(\xi) \leq x(t) \leq \bigcup_{\xi \in [t-d_f,t-d_f+m_f]} x(\xi)$$

where $0 \leq m_r \leq d_r, 0 \leq m_f \leq d_f$. Let us suppose in the beginning, when solving it, that $x(0-0) = 0$. The solutions are the next ones.

Case $d_f - m_f > 0$

We can show analogously with BDC' that the only solution is $x(t) = 0$.

Case $d_f - m_f = 0$, $d_r > 0$

As the inequality $x(t) \leq \bigcup_{\xi \in [t-d_f,t]} x(\xi)$ is satisfied by all $x$, BDC has in this case the same solutions like (in other words: is equivalent with)

$$\bigcap_{\xi \in [t-d_r,t-d_r+m_r]} x(\xi) \leq x(t) \tag{1}$$

and any solution can be written under one of the forms

$$x(t) = 0 \tag{2}$$

$$x(t) = \chi_{[t_0,\infty)}(t) \tag{3}$$

$$x(t) = \chi_{[t_0,t_1)}(t) \oplus \chi_{[t_2,t_3)}(t) \oplus \ldots \oplus \chi_{[t_{2n},t_{2n+1})}(t) \tag{4}$$

$$x(t) = \chi_{[t_0,t_1)}(t) \oplus \chi_{[t_2,t_3)}(t) \oplus \ldots \oplus \chi_{[t_{2n},t_{2n+1})}(t) \oplus \chi_{[t_{2n+2},\infty)}(t) \tag{5}$$

$$x(t)=\chi_{[t_0,t_1)}(t)\oplus\chi_{[t_2,t_3)}(t)\oplus\ldots\oplus\chi_{[t_{2n},t_{2n+1})}(t)\oplus\ldots \tag{6}$$

(2),…,(6) represent all the signals $x$ with $x(0-0)=0$, where $0\le t_0<t_1<t_2<\ldots.$ is unbounded, arbitrary. (2), (3) satisfy (1) without supplementary requests. If the term $\chi_{[t_{2k},t_{2k+1})}$ satisfies $t_{2k+1}-t_{2k}>m_r$ we have that

$$\bigcap_{\xi\in[t-d_r,t-d_r+m_r]}\chi_{[t_{2k},t_{2k+1})}(\xi)=\chi_{[t_{2k}+d_r,t_{2k+1}+d_r-m_r)}(t)$$

is not null and in order that (4),…,(6) be solutions of (1), the next property should be true for all $k\ge 0$:

$$t_{2k+1}-t_{2k}>m_r\Rightarrow[t_{2k}+d_r,t_{2k+1}+d_r-m_r)\subset supp\ x$$

We have noted $supp\ x=\{t\mid x(t)=1\}$ the support set of $x$.

A special case of (1) is the one when $m_r=0$:

$$x(t-d_r)\le x(t) \tag{7}$$

and then for all $k\ge 0$ the next inclusion

$$[t_{2k}+d_r,t_{2k+1}+d_r)\subset supp\ x$$

is fulfilled. For example, the 'periodical' functions

$$x(t)=\chi_{[t_0,t_1)}(t)\oplus\chi_{[t_0+d_r,t_1+d_r)}(t)\oplus\ldots\oplus\chi_{[t_0+n\cdot d_r,t_1+n\cdot d_r)}(t)\oplus\ldots$$

where $0\le t_0<t_1\le t_0+d_r$ satisfy (7) because

$$x(t-d_r)=\chi_{[t_0+d_r,t_1+d_r)}(t)\oplus\chi_{[t_0+2d_r,t_1+2d_r)}(t)\oplus\ldots\oplus\chi_{[t_0+(n+1)\cdot d_r,t_1+(n+1)\cdot d_r)}(t)\oplus\ldots$$

An interesting situation in BDC+AIC is the special case $\delta_r\ge m_r,\delta_f=0$ when the inclusion

$$[t_{2k}+d_r,t_{2k+1}+d_r-m_r)\subset supp\ x$$

is true for all $k\ge 0$ and all solutions $x$, the hypothesis $t_{2k+1}-t_{2k}>\delta_r\ge m_r$ being satisfied due to AIC.

Adding RIC in the case $d_f-m_f=0,d_r>0$ of BDC, under the form

$$\overline{x(t-0)}\cdot x(t)\le\bigcap_{\xi\in[t-\delta_r,t-\delta_r+\mu_r]}x(\xi) \tag{8}$$

$$x(t-0)\cdot\overline{x(t)}\le\bigcap_{\xi\in[t-\delta_f,t-\delta_f+\mu_f]}\overline{x(\xi)} \tag{9}$$

implies if $\delta_r>0$ that $x(t)=0$. For $\delta_r=0$, inequality (8) becomes trivial: $\overline{x(t-0)}\cdot x(t)\le x(t)$ and then, if $\delta_f>0$, the restrictions corresponding to RIC on the solutions $x$ of BDC are expressed under the form, see (4),…,(6)

$$\chi_{\{t_1,t_3,\ldots\}}(t)=x(t-0)\cdot\overline{x(t)}\le$$

$$\le\bigcap_{\xi\in[t-\delta_f,t-\delta_f+\mu_f]}\overline{x(\xi)}=\chi_{(-\infty,t_0+\delta_f-\mu_f)\vee[t_1+\delta_f,t_2+\delta_f-\mu_f)\vee[t_3+\delta_f,t_4+\delta_f-\mu_f)\vee\ldots}(t)$$

i.e. equivalently

$$\{t_1,t_3,\ldots\}\subset(-\infty,t_0+\delta_f-\mu_f)\vee[t_1+\delta_f,t_2+\delta_f-\mu_f)\vee[t_3+\delta_f,t_4+\delta_f-\mu_f)\vee\ldots$$

$\delta_r=\delta_f=0$ means triviality for RIC.

Case $d_f - m_f = 0, d_r = 0$

BDC consists in

$$x(t) \le x(t) \le \bigcup_{\xi \in [t-d_f, t]} x(\xi)$$

and all the signals $x$ satisfy it.

By duality, the possibility $x(0-0) = 1$ is analyzed. We observe for example that if $d_f - m_f > 0, d_r - m_r > 0$ then the only solutions of BDC are the constant functions.

**FDC** The equation to be solved is

$$x(t) = x(t-d), d \ge 0$$

If $d > 0$, then the solutions are the two constant functions and if $d = 0$ then the solutions are all the signals.

**DBRIDC** The system is

$$\overline{x(t-0)} \cdot x(t) = \overline{x(t-0)} \cdot \bigcap_{\xi \in [t-d_r, t-d_r+m_r]} x(\xi) \tag{10}$$

$$x(t-0) \cdot \overline{x(t)} = x(t-0) \cdot \bigcap_{\xi \in [t-d_f, t-d_f+m_f]} \overline{x(\xi)} \tag{11}$$

and we suppose like before that $x(0-0) = 0$.

Case $d_r > 0$

The only solution is $x(t) = 0$.

Case $d_r = 0, d_f = m_f > 0$

The switch from 0 to 1 is possible, because (10) takes the trivial form $\overline{x(t-0)} \cdot x(t) = \overline{x(t-0)} \cdot x(t)$. From this moment $\bigcap_{\xi \in [t-d_f, t]} \overline{x(\xi)}$ is null, thus the solutions have one of the forms (2), (3).

Case $d_r = 0, d_f = m_f = 0$

All the signals $x$ satisfy the system, (10), (11) being both trivial.

Case $d_r = 0, d_f > m_f \ge 0$

The switch from 0 to 1 seems possible and let $t_0$ be the moment of the first such switch, thus $\overline{x(t_0-0)} \cdot x(t_0) = 1$. At the time instant $t_1 > t_0$ characterized by $[t_0, t_1) \subset supp\ x$, (11) becomes

$$\overline{x(t_1)} = \bigcap_{\xi \in [t_1-d_f, t_1-d_f+m_f]} \overline{x(\xi)} \tag{12}$$

For all $t_1 - d_f + m_f < t_0$, i.e. if $0 < t_1 - t_0 < d_f - m_f$, the right member of (12) is 1 and the switch of $x$ from 1 to 0 necessary. We have reached a contradiction showing that DBRIDC has no solution $x(t) \ne 0$.

The analysis of the situation when $x(0-0) = 1$ is similar.

**SDBRIDC'** The solutions of the equation

$$Dx(t) = 0$$

are the constant functions.

### 2.3 The Logical Gate NOT

The logical gate NOT that computes the complement in the set $\{0,1\}$ is symbolized like in the next figure

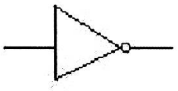
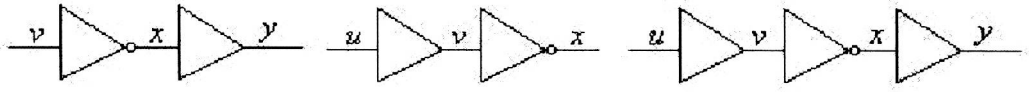


Fig 4

where the gate and the two wires are characterized by delays. It is modeled by one of the next circuits




a) b) c)

Fig 5

In Fig 5 the logical gate is ideal

$$x(t) = x(0-0)\cdot \chi_{(-\infty,0)}(t) \oplus \overline{v(t)}\cdot \chi_{[0,\infty)}(t) \tag{1}$$

as well as the wires and the delays are localized in the delay circuits. Writing the relations between $u, v$, respectively between $x, y$ follows, like at 2.1. The last step is the elimination (if possible) of the intermediary variables: $x$ at a), $v$ at b), $v$ and $x$ at c). We give some examples.

**SC** Fig 5 c)

The fact that $u$ is of the form

$$u(t) = u(t)\cdot \chi_{(-\infty,t_0)}(t) \oplus u(t_0)\cdot \chi_{[t_0,\infty)}(t) \tag{2}$$

implies that $v$ is of the form

$$v(t) = v(t)\cdot \chi_{(-\infty,t_1)}(t) \oplus u(t_0)\cdot \chi_{[t_1,\infty)}(t) \tag{3}$$

thus, from (1), $x$ is given by

$$x(t) = x(t)\cdot \chi_{(-\infty,t_1)}(t) \oplus \overline{u(t_0)}\cdot \chi_{[t_1,\infty)}(t) \tag{4}$$

and by using SC again for the second delay circuit we get

$$y(t) = y(t)\cdot \chi_{(-\infty,t_2)}(t) \oplus \overline{u(t_0)}\cdot \chi_{[t_2,\infty)}(t) \tag{5}$$

In (2),…,(5) $t_0 \geq 0, t_1 \geq 0, t_2 \geq 0$.

**BDC'** Fig 5 a)

$$\bigcap_{\xi\in[t-d_r,t)} x(\xi) \leq y(t) \leq \bigcup_{\xi\in[t-d_f,t)} x(\xi) \tag{6}$$

$$\bigcap_{\xi\in[t-d_r,t)} (x(0-0)\cdot \chi_{(-\infty,0)}(\xi) \oplus \overline{v(\xi)}\cdot \chi_{[0,\infty)}(\xi)) \leq y(t) \leq$$

$$\leq \bigcup_{\xi\in[t-d_f,t)} (x(0-0)\cdot \chi_{(-\infty,0)}(\xi) \oplus \overline{v(\xi)}\cdot \chi_{[0,\infty)}(\xi)) \qquad \text{(from (1), (6))} \tag{7}$$

**BDC'** Fig 5 b)