HEWLETT PACKARD

HP 1000 E-Series Computer HP 2109B and HP 2113B

Operating and Reference Manual

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MANUAL SUPPLEMENT

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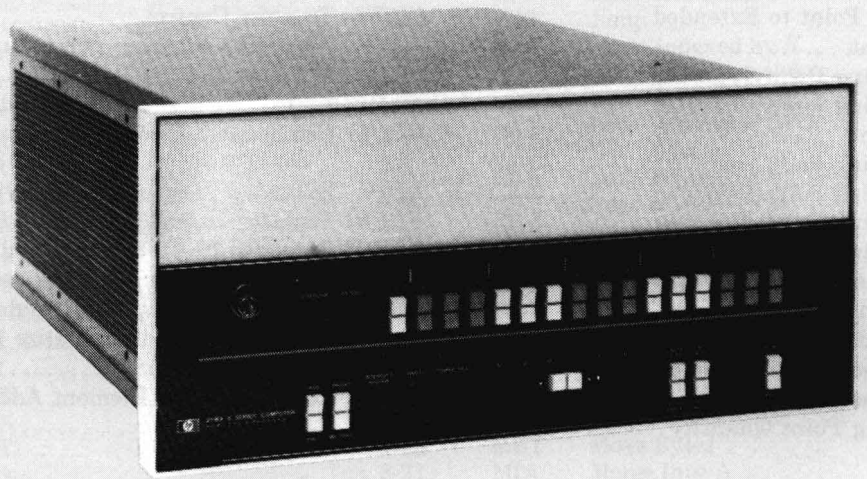

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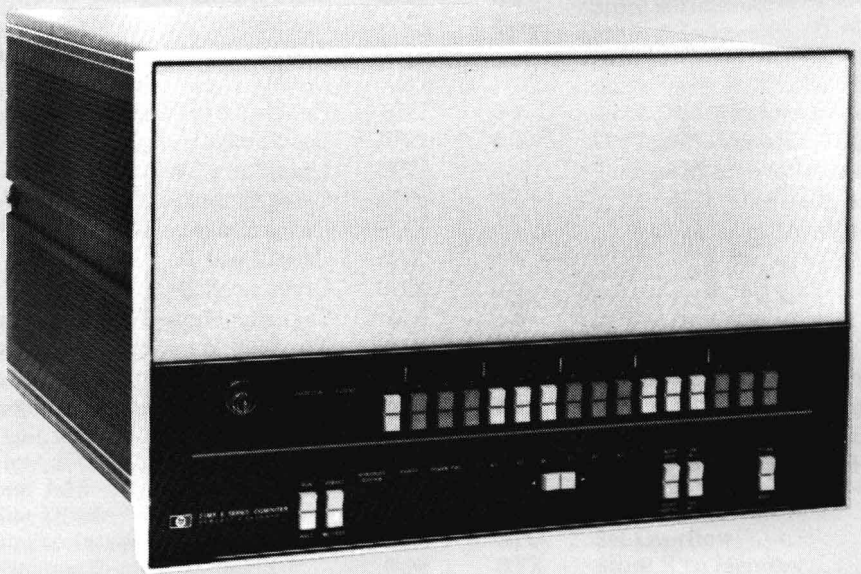

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Figure 1-1. HP 1000 E-Series Microprogrammable Computers

SECTION I
SYSTEM FEATURES

The HP 1000 E-Series computers HP 2109B and HP 2113B shown in figure 1-1 are high-performance machines designed to satisfy a wide range of computing needs. Because of a unique design philosophy, many features have been incorporated as standard in the E-Series; this same philosophy allows optional features to be added at low cost. E-Series computers have traditional HP quality and reliability built in from the ground up and compatibility with previous Hewlett-Packard computers is maintained. HP 1000 E-Series computers (hereafter referred to as E-Series computers), provide very cost-effective solutions to a variety of systems applications.

1-1. ARCHITECTURE

E-Series computers have a proven architecture that features a fully microprogrammed processor, including all arithmetic functions, input/output, and operator panel control. Four general purpose registers are available, two of which may be used as index registers. There are 128 standard instructions including index instructions, integer and floating point arithmetic instructions, input/output instructions, and a full complement of instructions for logical operations as well as bit and byte manipulation.

The E-Series computers have been optimized for performance. At the heart of the computer is a microprogrammed control section that directs the operations of the other functional units of the computer. In the E-Series, the control section has been speeded up for certain operations due to a sophisticated technique of varying the microinstruction cycle time. In addition, the efficiency of the microprogrammed routines that determine the machine language operation has been increased. The result is a high-performance computer that retains compatibility with earlier Hewlett-Packard computers and the flexibility of user microprogramming. The central processor unit (CPU) to memory interface is totally asynchronous in E-Series computers, thus assuring that faster memory speeds can be used to good advantage.

For those applications where even the HP standard set of instructions is not enough, E-Series computer users may expand their instruction repertoire by using HP-supplied instruction sets. Off-the-shelf enhancements include the Dynamic Mapping System (DMS) for expanded memory management and the Fast FORTRAN Processor for fast handling of compiler and extended precision routines.

1-2. USER MICROPROGRAMMING

The power and flexibility of microprogramming is made readily available to the E-Series computer user through the microinstruction set of 211 micro-orders. Microprogrammers have access to 12 special scratch pad registers in addition to the other internal registers of the E-Series, and may address up to 16K, 24-bit words of control store. E-Series computers also support up to three levels of nested subroutines in microprograms. Closely resembling assembly language programming in simplicity, microprogramming offers the advantages of speed and security as well as the ability to expand the instruction set to meet any computing need. Microprogramming is supported by Hewlett-Packard through software assembly and debug packages and customer training courses. User-developed microprograms may be permanently fused in programmable Read-Only Memory (pROM) chips for mounting on the Firmware Accessory Board, or may be loaded into Writable Control Store (WCS) modules where they can be dynamically altered.

1-3. SELF-TEST DIAGNOSTICS

A comprehensive set of diagnostic routines permanently stored in Read-Only Memory (ROM) are standard in E-Series computers. Two of these routines, executed each time the IBL/TEST functions is performed, tests the CPU and the enabled memory (up to 32K) for quick verification of operating condition. A third test, executed every time the machine is powered up, tests the CPU and all installed memory.

1-4. LOCAL AND REMOTE BOOTSTRAP LOADERS

The initial binary loading (IBL) function is easily performed on E-Series computers. For local bootstrap loading, a 64-word ROM-resident IBL program is called by pushbutton switch on the operator panel. A paper tape loader ROM and a disc loader ROM are standard. One or two additional loader ROM's may be included; these programs may be purchased as accessories or may be user-generated.

Computers at remote sites can be force-loaded from a central location through the use of the Remote Program Load (RPL) capability. All of the information normally keyed into the operator panel is set in a special set of switches on the CPU board so that the bootstrapping sequence may be initiated from a remote site.

1-5. POWER SYSTEM

E-Series computers are equipped with power systems designed to continue normal operations in environments where power may fluctuate widely. Input line voltages and frequencies may vary widely without affecting the operation of the computer. The optional Power Fail Recovery System provides automatic restart capability and, depending on the memory size, also provides between 1.75 and 4.25 hours of memory sustaining power in the event of complete power failure. (See Power Fail Recovery System specifications in table 1-1.)

1-6. MEMORY SYSTEMS

The HP 1000 E-Series computers are available with a variety of semiconductor memory systems. The memory systems are based on 16k-bit MOS/RAM semiconductor chips that offer field-proven reliability and economy. The Standard Performance Memory System consists of an HP 2102B memory controller and one or more 64k byte (12746A) or 128k byte (12747A) memory modules. The Standard Performance Memory System has a system cycle time of 595 nanoseconds. The High Performance Memory System consists of an HP 2102E memory controller and one or more 64k byte (12746H) or 128k byte (12747H) memory modules. The latest MOS/RAM technology combined with extensive testing assures maximum reliability.

The Fault Control Memory System provides fault-secure memory operation for the HP 1000 family of computers. These systems are offered in Standard and High Performance versions. The Standard version consists of an HP 2102C memory controller and one or more check bit array boards, along with the appropriate memory modules (12746A or 12747A). The High Performance Fault Control Memory System consists of an HP 2102H memory controller and one or more check bit array boards. 12746H or 12747H memory modules are used. Both of these systems are capable of correcting all single-bit errors, and of detecting all double-bit and most multiple-bit errors. The fault control systems are particularly valuable in computer systems with large amounts of memory or where fault-secure operation is essential.

Addressing physical memory configurations larger than 64k bytes is possible only through the use of the HP 13305A Dynamic Mapping System. The Dynamic Mapping System (DMS), which is a combination of hardware and firmware, is a powerful memory management scheme that allows E-Series computer users to address up to two milllion bytes of memory and provides read and/or write protection of each individual 2048 byte page. Four independent memory maps are provided, one for the system, one for the user, and two Port Controller maps for direct memory access operations. Control of the DMS is implemented through the use of 38 instructions.

1-7. INPUT/OUTPUT

The input/output system for E-Series computers features a multilevel vectored priority interrupt structure. There are 60 distinct interrupt levels, each of which has a unique priority assignment. Any I/O device can be selectively enabled or disabled, or the entire interrupt system (except power fail and parity error interrupts) can be enabled or disabled under program control.

Data transfer between the computer and I/O devices may take place under program control, Dual Channel Port Controller (DCPC) control, or under microprogram control. The DCPC provides two direct links between memory and I/O devices and is program assignable to any two devices. DCPC transfers occur on an I/O cycle-stealing basis not subject to the I/O priority interrupt structure. The total bandwidth through both DCPC channels is 2.0 million bytes per second (input); see Direct Memory Access specifications in table 1-1 for the output transfer rates and the DCPC latency times. For applications where higher transfer rates are desirable, E-Series computers have a special microprogrammed I/O capability that will allow transfer rates of up to 3.18 million bytes per second. This capability can be attained by making simple modifications to the interface hardware and by writing a block I/O control microprogram.

The HP 2109B Computer has nine I/O channels in the mainframe; the HP 2113B Computer has fourteen. The number of available channels may be increased by adding one or two HP 12979B I/O Extenders, providing sixteen channels each. All I/O channels are fully powered, buffered, and bidirectional. Because of the modular design of the E-Series computers, mainframe memory capacity is completely independent of I/O capacity so that either memory or I/O modules may be added without taking valuable mainframe space from the other. A full line of I/O interface controllers is available with E-Series computers for interfacing to any of the broad line of HP manufactured peripherals or to specialized devices.

1-8. SOFTWARE

The E-Series computers are fully program compatible with earlier Hewlett-Packard computers so that the user may take advantage of *many* man-years of software development.

A wide range of operating system software is available. The Real-Time Executive (RTE) systems are multiprogramming systems that permit priority scheduling of several real-time programs while concurrent background processing takes place. RTE software contains all the tools needed for dynamic control of real-time events and has an efficient file management capability for data processing applications. The most powerful version, RTE-IVB, supports up to 2.048 megabytes of memory managed by the Dynamic Mapping System.

Languages supported by Hewlett-Packard operating systems include two high-level compilers: HP FORTRAN IV; and HP BASIC; plus an extended, efficient assembler that is callable by FORTRAN. Utility software includes a debugging routine, and editor, and an extensive library of commonly used computational routines.

E-Series computer users may also take advantage of a wide variety of thoroughly tested and documented programs that have been contributed to the Hewlett-Packard User Library.

1-9. SPECIFICATIONS

Table 1-1 lists the specifications for the HP 2109B and the HP 2113B Computers and the Standard Performance, High Performance, and Fault Control Memory Systems. Both computers have been product accepted by the Underwriters' Laboratories (UL) and the Canadian Standards Association (CSA).

1-10. SYSTEM EXPANSION AND ENHANCEMENT

Table 1-2 lists the options and accessories available to expand or enhance the computer system.

Table 1-1. Specifications

CENTRAL PROCESSOR	
Address Space:	4,096 bytes (direct addressing) 65,536 bytes (indirect addressing) 2,097,152 bytes with Dynamic Mapping System (optional)
Word Size:	16 bits
Instruction Set:	128 standard instructions
Memory Reference:	14
Register Reference:	43
Input/Output:	13
Extended Arithmetic:	10
Index:	32
Bit Byte, Word Manipulation:	10
Floating Point:	6
Registers:	10
Accumulators:	Two (A and B), 16 bits each. Explicitly addressable; also addressable as memory locations.
Index:	Two (X and Y), 16 bits each
Memory Control:	Two (T and P), 16 bits each; one (M), 15 bits.
Supplementary:	Two (Overflow and Extend), one bit each
Display:	One, 16 bits
CONTROL PROCESSOR	
Address Space:	16,384 words (64 modules of 256 words each)
Word Size:	24 bits
Word Formats:	Four
Word Fields:	Five
Instruction Execution Time:	Variable; 175 nS or 280 nS

Table 1-1. Specifications (Continued)

CONTROL PROCESSOR (Continued)

Micro-Orders (Microinstructions):	211
Operations:	15
Special:	32
ALU and Conditional:	68
Store:	32
S-Bus:	32
Reverse Skip Sense	32

INITIAL BINARY LOADERS

ROM resident; capacity of four 64-word programs callable from operator panel. Computer can be configured for forced cold loading from a remote site.

SELF-TEST

Automatic tests of CPU and memory operating condition. Executed on cold power-up and whenever operator panel IBL/TEST switch is pressed.

INPUT/OUTPUT

Interrupt Structure:

Multilevel vectored priority interrupt; priority determined by interrupt location.

I/O SYSTEM SIZE	HP 2109B	HP 2113B
Standard I/O Channels	9	14
With One Extender	25	30
With Two Extenders	41	46

Compatibility:

Instruction set and program compatible with HP 1000 E-Series computers (time loop programs excepted).

Current Available for:

I/O and Accessories

Model	+5V	+12V	−12V	−2V
2109B	38.8A	2.5A	2.0A	4.0A
2113B	38.8A	2.5A	2.0A	4.0A

Table 1-1. Specifications (Continued)

INPUT/OUTPUT (Continued)

DC Required:

Model	+5V (with PFRS)[4]	+5V (w/o PFRS)	−2V
12892B Memory Protect	1.3A	1.3A	0.05A
12897A DCPC	2.4A	2.4A	0.05A
12731A Memory Expansion Mod.	3.9A	3.9A	—
13307A DMI	0.78A	0.78A	—
13306A FFP	1.8A	1.8A	—
13197A 1k WCS	2.2A	2.2A	—
12990B Memory Extender	—	—	—
12992 Loader ROMs (each)	0.13A	0.13A	—
12979B I/O Ext. Buffer Card	2.0A	2.0A	1.35A
2102B Memory Controller	1.2A	1.7A	0.01A
2102C Fault Memory Controller	3.3A	4.1A	—
12779A Check Bit Array	0.25A	0.9A	—
12780A Check Bit Array	0.3A	1.1A	—
12746A 64k Byte Memory Module	0.475A	1.075A	—
12747A 128k Byte Memory Module	0.475A	1.075A	—
2102E Memory Controller	2.56A	3.2A	—
2102H Fault Memory Controller	3.3A	4.1A	—
12779H Check Bit Array	0.25A	0.9A	—
12780H Check Bit Array	0.3A	1.1A	—
12746H 64k Byte Memory Module	0.475A	1.075A	—
12747H 128k Byte Memory Module	0.475A	1.075A	—
13047A 2k UCS	7.39A[1]	7.39A[1]	—
13304A Firmware Accessory Board	1.8A[2]	1.8A[2]	—
12791A Firmware Expansion Mod.	5.4A[3]	5.4A[3]	—

[1] *1.15A + 0.78A for each 256 instructions; 7.39A when fully loaded.*

[2] *Due to power saver circuit, this is the maximum current regardless of amount of microcode loaded on the board.*

[3] *1.2A + 0.525A for each of 8 blocks of instructions words; 5.4A fully loaded.*

[4] *+5V current requirements with 12944A or 12991B Power Fail Recovery System installed. The difference in the two +5V current requirements is the current drawn by memory products operating totally from the Power Fail Recovery System.*

DIRECT MEMORY ACCESS — Available only with DCPC accessory.

Number of Channels: Two

Word Size: 16 bits

Maximum Transfer Block Size: 32,768 words

I/O Assignable: Assignable to any two I/O channels; all logic necessary to facilitate bi-directional direct memory transfer to and from I/O is contained on DCPC (controller).

DIRECT MEMORY ACCESS (Continued)

Transfer Rate:
(All rates in Mbytes/s)

(Standard Performance Memory)

(Standard Performance Fault Control

(High Performance Memory)

(High Performance Fault Control Memory)

HP 2102B	Minimum	Typical	Maximum
Input w/DMS	1.884	1.950	2.098
w/o DMS			
Output w/DMS	1.626	1.676	1.782
w/o DMS	1.672	1.778	1.938
HP 2102C			
Input w/DMS	1.946	1.018	2.096
w/o DMS			
Output w/DMS	1.586	1.626	1.726
w/o DMS	1.670	1.724	1.780
HP 2102E			
Input w/DMS	2.282	2.284	2.284
w/o DMS			
Output w/DMS	2.038	2.114	2.196
w/o DMS	2.196	2.284	2.284
HP 2102H			
Input w/DMS	2.28	2.28	2.28
w/o DMS			
Output w/DMS	1.902	1.968	2.038
w/o DMS	2.038	2.114	2.196

DCPC Latency (Channel 1):

Latency is defined as the time interval between the generation of a Service Request (SRQ) signal by an I/O device through the initiation of a DCPC channel 1 cycle to the completion of the I/O data transfer to or from the I/O interface PCA. Subsequent consecutive cycles execute at a specified DCPC rate.

Input and Output Latency Times:
(Times in us)

(Standard Performance Memory)

(Standard Performance Fault Control Memory)

(High Performance Memory)

(High Performance Fault Control Memory)

HP 2102B	Minimum	Typical	Maximum
Input w/o DMS	2.73	2.91	3.15
w/DMS	2.84	3.12	3.26
Output w/o DMS	3.43	3.64	3.95
w/DMS	3.57	3.92	4.10
HP 2102C			
Input w/o DMS	2.98	3.12	3.26
w/DMS	3.09	3.33	3.46
Output w/o DMS	3.75	3.93	4.11
w/DMS	3.89	4.21	4.36
HP 2102E			
Input w/o DMS	2.21	2.21	2.28
w/DMS	2.24	2.28	2.35
Output w/o DMS	2.75	2.75	2.84
w/DMS	2.80	2.87	2.98
HP 2102H			
Input w/o DMS	2.31	2.42	2.52
w/DMS	2.38	2.56	2.74
Output w/o DMS	2.84	2.94	3.05
w/DMS	2.98	3.16	3.33

Table 1-1. Specifications (Continued)

DIRECT MEMORY ACCESS (Continued)

A USER MICROCODE sequence of seven consecutive reads may provide conditions to produce the absolute worst case latency time. The absolute worst case latency times are as follows:

Memory System	Input	Output
HP 2102B	4.095 us	4.935 us
HP 2102C	5.125 us	6.031 us
HP 2102E	3.050 us	3.681 us
HP 2102H	3.510 us	4.100 us

PHYSICAL CHARACTERISTICS

Width: 42.6cm (16 3/4 in) behind rack mount; 48.3cm (19 in) front panel width on sides

Depth: 59.7cm (23 1/2 in); 58.4cm (23 in) behind rack mounting ears

Model	HP 2109B	HP 2113B
Height	22.2cm (8-3/4 in)	31.1cm (12-1/4 in)
Weight	20.4kg (45 lbs)	29.5kg (65 lbs)

ELECTRICAL CHARACTERISTICS

Line Voltage: 88 to 132 Vac; 176 to 264 Vac

Line Frequency: 47.5 to 66 Hz

Power Dissipation: 770 watts (maximum)

Power Supply: Sustains computer over a line loss of no greater than 8 ms at the minimum line (mains) voltage.

Input Line Transients: Sustains ±500V, 50μs pulse on power lines; sustains ±1kV, 100ns pulses on power lines.

Output Protection: All regulated voltages protected from overvoltage and overcurrent conditions.

Output Voltage Regulation: ±5% (except −2V is ±10%, and +30V is unregulated).

Thermal Sensing: Monitors internal temperature and automatically shuts down when computer temperature exceeds operating temperature. Resets automatically when temperature returns to operating temperature.

ENVIRONMENTAL LIMITATIONS

Operating Temperature: 0° to 55°C (+32° to 131°F)

Storage Temperature: −40° to 75°C (−40° to 167°F)

Relative Humidity: 20% to 95% at 40°C (104°F), non-condensating

Table 1-1. Specifications (Continued)

ENVIRONMENTAL LIMITATIONS (Continued)

Ventilation and Heat Dissipation: Intake: left-hand side; Exhaust: right-hand side.

	Model	2109B	2113B
Heat dissipation	KCal/hr. max.	538	538
	BTU/hr. max.	2138	2138
Air flow	cubic meters /min.	6.63	9.23
	cubic feet /min.	200	280

Altitude: Transportable to 15 300m (50 000 ft) in non-operating condition and 4500m (15 000 ft) for operation

Vibration and Shock: **Vibration:** .30mm (0.12 in) p-p, 10-55 Hz, 3 axis
Shock: 30g, 11 Ms, 1/2 sine, 3 axis
Contact factory for review of any application requiring operation under continuous vibration.

MEMORY SYSTEMS

Type: 16k N-channel MOS semiconductor RAM.

Word Size: 16 bits plus parity bit

Configuration: Controller plus multiple plug-in memory modules. Available in 64k and 128k byte modules.

Page Size: 2,048 bytes

Address Space: 65 536 bytes without DMS; 2.048 megabytes with DMS (2109B and 2113B)

System Cycle Times:
(All cycle times in ns)

Cycle	Minimum	Typical	Maximum
(Standard Performance Memory)			
READ w/o DMS	560	595	665
READ w/DMS	595	665	700
WRITE	595	665	700
REFRESH	595	665	700
(Standard Performance Fault Control Memory)			
READ w/o DMS	595	630	665
READ w/DMS	630	700	730
WRITE	595	630	665
REFRESH	595	630	665
(High Performance Memory)			
READ w/o DMS	350	350	385
READ w/DMS	385	420	455
WRITE	350	350	385
REFRESH	350	350	385
(High Performance Fault Control Memory)			
READ w/o DMS	386	421	456
READ w/DMS	456	491	526
WRITE	386	421	456
REFRESH	386	421	456

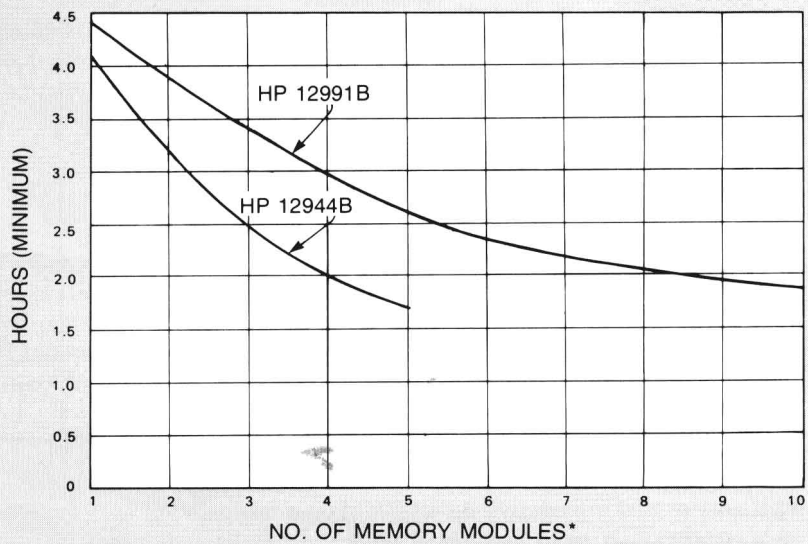
Table 1-1. Specifications (Continued)

MEMORY SYSTEMS (Continued)

Volatility Protection:	Sustaining power for line loss of no less than 8ms at the minimum line (mains) voltage. Power fail recovery system is optional.
Parity Error Detection:	Monitors all words read from memory. Switch selectable for either halt or ignore interrupt error when detected. With memory protect or DMS accessory, interrupt on parity error occurs.

POWER FAIL

Interrupt Priority:	Highest priority interrupt.
Power Failure:	Detects power failure and generates an interrupt to user-written power-failure routine. A minimum of 500 μs is available for the routine.
Power Fail Recovery Systems:	Available as an accessory. (HP 12944B or HP 12991B).
Power Restart:	Detects resumption of power and generates an interrupt to user-written automatic restart program which has been protected in memory by the sustaining battery.
Power Control and Charge Unit:	Monitors battery charge status and provides trickle charge.
Sustaining Battery:	Type: 14 volt, 5 ampere-hours, sealed lead acid Charging rate: 2A, maximum Capacity: HP 12944B and HP 12991B will sustain memory for the period of time shown in the graph below.



* Includes memory boards and fault control check bit array boards.