ADVANCES IN CERAMICS • VOLUME 19

MULTILAYER CERAMIC DEVICES

Edited by
John B. Blum
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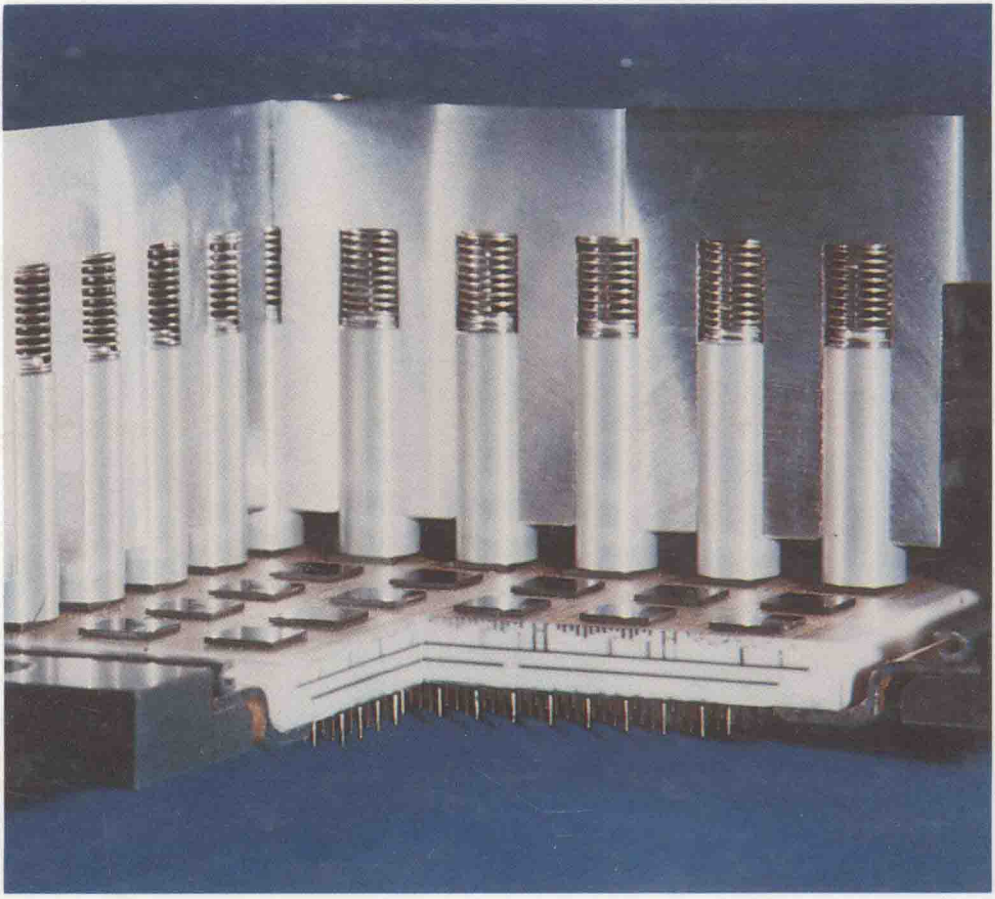
W. Roger Cannon



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The American Ceramic Society, Inc.
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Cover photo: Cutaway view of a Thermal Conduction Module which incorporates a 33-layer ceramic substrate. Courtesy IBM Corporation.

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Preface

Multilayer ceramic devices are becoming increasingly important in several key electronic applications. Multilayer ceramic capacitors are helpful in reducing the size of electronic circuitry. These capacitors are used extensively in computers, telephones, and many other applications. Multilayer ceramic packages are used to house electronic circuitry in a small, hermetically sealed volume which improves reliability and increases circuit speed in many important applications.

Multilayer devices based on ceramics also contain other materials. These devices are best thought of as materials systems. Consideration must be given to the organic additives and metallic pastes used in the devices as well as the ceramics.

In addition to being a materials challenge, multilayer ceramic devices are also a manufacturing challenge. As an example, IBM has expended a great deal of money and effort for perfecting the manufacture of their multilayer chip carrier. The manufacturing lessons learned in one portion of the manufacturing process of one device can be very valuable to other technologists.

Although the materials and manufacturing of these devices are different, many of the basic principles are similar. With this in mind, the Electronics Division of the American Ceramic Society decided to sponsor a topical meeting devoted to Multilayer Ceramic Devices in order to bring the researchers involved together. It was thought that, by promoting an interaction between people who had been interested in specific areas, many ideas of mutual interest could be discussed from different perspectives and experiences.

The topical meeting took place in Orlando, Florida, on October 13–16, 1985. This volume contains most of the papers presented at that meeting. It is hoped that it will be a useful reference as perhaps the first book which treats the important problems and technologies associated with multilayer ceramic devices.

The editors would like to dedicate this book to the memory of Chuck Hodgkins who passed away while the book was being edited. Chuck was well known to many in the capacitor business. It was through his help and with his recommendations that we became involved in this interesting area.

John B. Blum
Norton Company
and
W. Roger Cannon
Rutgers University

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Technology and Market Trends in Multilayer Ceramic Devices

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The major multilayer ceramic devices, integrated circuit packages and capacitors, are each approaching billion dollar markets in the United States. Each is being driven by trends occurring in the electronics industry, particularly as integrated circuits are moving to higher circuit densities and higher speeds. This in turn is leading to higher cost, more customized chip packages with higher *I/O*, made by new processes and using new materials. In multilayer ceramic capacitors, increasing use of automatic insertion and surface mount technology is changing the shape, size, and configuration of the devices. The drive to lower unit costs is also changing the traditional dielectric and electrode materials mix in these products. This paper presents analyses of the economical and technical driving forces in operation, in order to project what lies ahead and examine what this may mean for the U.S. ceramic industry.

Electronics has become the largest existing market for advanced ceramics. In the United States it has grown to over $2 billion a year (Table I). On a worldwide basis it is at least $4 billion a year.

Within this broad market category, multilayer ceramic devices — in both IC packages and capacitors — are now the largest segments, having reached about $600* million and $610† million, respectively, in total U.S. sales in 1984. Each is equivalent to the total volume of all other electronic ceramic products combined. This growth has been driven mainly by the burgeoning growth in integrated circuits, tracking at an average 20 to 25% per year over the past 20 years. Due to the long-term demand growth expected from the computer, telecommunications, and military markets, a growth rate of 15 to 20% is expected to be sustainable for the foreseeable future.

Ceramic multilayer capacitors are looked upon as the most compatible type of capacitor for future use with high-density, high-speed integrated circuits. Sales have nearly doubled from 1982 to 1984 and they are expected to continue their significant growth, approaching $1.4 billion by the turn of the decade (Table II).

The *ceramic integrated circuit package* provides a housing for the semiconductor chip with leads that connect the chip to the circuit, conduct heat away from the chip, and hermetically seal it from the environment. It has roughly doubled its market size between 1982 and 1984 to about $600 million. Ceramic packages share the market with plastic packages, and currently account for 20% of the units but upward of 50% of the dollar volume. Ceramic packages are of critical importance because of their high thermal conductivity and hermeticity in the more demanding circuit applications.

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*From various industry sources.
†Electronics Industries Association, Washington, D.C.

Table I. Electronic Ceramic Markets in the United States

	$ Million
IC packages*	600
Multilayer capacitors†	610
All other electronics‡	700
Total	1910

*Based on various industry sources.
†Electronic Industries Association, Washington, D.C.
‡Estimate based on various industry sources.

Table II. U.S. Multilayer Ceramics Market Projections ($ Millions)

	1982	1984	1990
IC packages*	430	600	2500–3000
Multilayer capacitors†	350	610	1400

*Projections based on various industry sources.
†Electronic Industries Association, Washington, D.C.; projection based on S. L. Blum, S. H. Kalos, and J. B. Wachtman, Jr., "MLCs Head Economic Growth in Advanced Ceramics," *Ceram. Ind.*, July 1985; pp. 26–30.

A number of forces are expected to drive the U.S. package market to significantly higher levels over the next five years, the most important of which is expanding growth in the higher lead count, more expensive and more sophisticated package configurations such as chip carriers, fine pitch chip carriers, pin grid arrays, and ceramic motherboards. Until fairly recently, the dual-in-line packages — the side braze and cerdip types — dominated the market and became standardized for such high-volume applications as 16K and 64K RAMs. This has allowed producers, such as Kyocera, to farm out large segments of their production process to low-cost cottage industry and to automate handling, assembly, and final processing in order to achieve output rates in the hundreds of millions of units.

The Ceramic Package Market

Currently, the U.S. ceramic IC package market is dominated by two Japanese suppliers, as shown in Table III. Kyocera and NTK together account for approximately 80% of all packages sold in this country. Narumi has also been increasing its presence to between 5 and 10%. The largest U.S. domestic supplier is General Electric, which has plans to significantly expand its operations over the next three to five years to compete with the Japanese. The other U.S. companies are small players who have carved out specific niches in the marketplace, typically in specialized and high-value packages where they do not have to directly confront the big suppliers. Yet, U.S. suppliers have found it difficult to achieve significant market penetration or presence. This can be attributed to a number of direct and indirect factors that have included poor product planning and market definition, low production yields, inability to tightly control the many manufacturing steps, not utilizing the most advanced technology available, slow product delivery times, and, more indirectly, the pervasive reputation of the few large Japanese suppliers for aggressive prototype delivery and production turnaround, who have been able to fine-tune their production process over a longer period of time.

Table III. Package Suppliers to U.S. Market (Market Shares Based on Sales Volume)

	Percent
Kyocera	55–70
NTK	15–25
Narumi	5–10
GE	4
American Hoescht (Metceram)	2
Cabot*	2
Raychem/Interamics	1
General Ceramics	1
Brush Wellman (EPI)	0.5
LDC	0.5
Diacon	0.5
Bourns	0.5
Shinko	0.5
	100

*Includes Augat, Spectrum, and Rhode Island Electric.

Market Driving Forces

Standardized DIP products have been steadily growing at 15 to 20% annually but have been noticeably slowing in the last couple of years. What has been keeping the market on its traditional growth path has been the accelerated growth above 20% per year in more complex package designs such as leaded and unleaded chip carriers and pin grid arrays.

The standard DIP packages, which cannot accommodate the newer, more sophisticated chips because of their geometry and limited lead counts, may actually begin to taper off and slowly decline within a couple of years as chip carriers and pin grid arrays become more dominant.

The market share numbers make it rather obvious that more U.S presence is needed in the industry. Military contractors do have concerns about the lack of an adequate domestic supplier base and the fact that many classified advanced circuit designs have been going offshore for package prototyping and production.

Technical Driving Forces

The major technical force for change in packaging technology is coming from the trend toward increasingly complex semiconductor chips for improved cost and performance. The new chips, such as the new microprocessors and gate arrays, have higher densities and generate more heat during operation. Chips with 500 000 active devices one or two years ago have given way to one to two million devices per chip now. This trend is reflected in package architectures that provide greater numbers of vias, higher lead counts, and more sophisticated materials and geometries for higher conductivity and greater heat removal. So far, ceramics have performed adequately in high-performance applications and are not expected to give ground to plastic packages, even though plastics have 80% of the market in unit volume, but rather are expected to maintain their present market share in the future.

Package configurations are being strongly influenced by the ongoing movement to surface mount technology. This is a prime technique for reducing size,

weight, and cost by improving the component packaging density. With the advent of new printed wiring board materials, which are matched to the temperature coefficient of expansion of ceramic chip carriers, high-density assemblies have been achieved. This has encouraged the introduction of various types of leadless chip carriers which possess such operating advantages as lower profile, better heat transfer, and more direct electrical paths for higher frequency circuit operation, particularly for military applications. There are also disadvantages associated with the failure of the direct solder connection to the substrate due to stresses created by thermal expansion mismatch between the package and substrate. As an alternative, leaded devices for surface mount are also available. For example, the small outline or SOIC package, smaller than the standard DIP, with compliant J leads, has received strong acceptance by many users for surface mount and may emerge as one of the more dominant package formats. It competes with the plastic leaded chip carrier in the same kinds of commercial and industrial applications. Surface mount technology diffusion has been somewhat slowed by the lack of suitable standardized package formats, their higher cost, less availability from vendors, and the high cost of new automated placing equipment required to exploit the benefits of surface mount.

The need for more interconnects and higher lead counts has brought about new package formats such as chip carriers with lead counts up to 164 on .0508 cm (.02 in.) centers; pin grid arrays are available now with over 300 leads. However, at present, in both these formats, the most common lead count in use is around 68. New designs with closer lead spacings called fine pitch chip carriers are being introduced; lead spacings are of 0.05 (0.02) to 0.063 cm (0.025 in.) and lead counts are 308 and 244, according to proposed JEDEC standards. It is these kinds of designs that are expected to experience significant future growth into the 1990s for increasingly complex semiconductor circuits.

Users are increasingly finding that they need a particular kind of package for a particular kind of semiconductor circuit, resulting in a growing need for customized packages. The ever-increasing proliferation of new package formats is expected to continue at an accelerating pace as each user finds it necessary to have his own unique type of package.

Flexible manufacturing technology has been developing concurrently through the application of CAD/CAM techniques so that now it has become possible to respond to users' special design needs with flexible tooling of packages. This stands in contrast to hard tooling, which previously locked-in a significant capital investment in equipment lacking adaptability and flexibility for new products. This capability of the package supplier should promote a much closer interface with the user in designing and prototyping the package than has existed in the past with standard-commodity DIP packages.

Materials Technology

So far, the bulk of ceramic packages have been produced from alumina ranging from 90 to 94% purity by either the dry-pressing process (for cerdips) or multilayer tapecast cofire technology, and, so far, alumina has performed adequately. However, package performance is being pressed to its limits with the commercial technology we have today. As semiconductor chips increase in speed and density, ceramic materials must become available that possess a lower dielectric constant to reduce signal propagation delay and maintain high thermal conductivity. They must also have lower sintering temperatures to accommodate higher conductivity interconnect materials like copper to replace the molybdenum

and tungsten alloys presently in use. As circuit board real estate is becoming increasingly tight, and as the sheer number of vias and interconnects grows, an increasing premium is being placed on better shrinkage uniformity and dimensional control and tolerances in the finished package.

Ceramics are expected to continue to be specified for the burgeoning high-performance end of the package market, particularly where hermeticity is required, even though concurrent improvements are continuing in plastic package design and materials.

In the area of ceramic substrates for package interconnection, control of ceramic powder characteristics and processing is critical to increasing the available sizes. Users would like to have substrates larger than the typical 6 inch by 6 inch dimensions today. Warping limits sizes much beyond this; however, alumina powder technology is being developed that is expected to facilitate warp-free substrates in the 21 by 21 cm (10 by 10 in.) size and potentially larger.

Ultimately, new package designs will be required to meet the challenges of gallium arsenide circuits that will be much higher speed and higher power devices. Such devices, while able to use existing package types, will likely require new types of materials approaches that are only at an embryonic stage today. At present, existing packages for GaAs chips are still low lead count, but chip quality will first have to improve before LSI and high-lead-count, sophisticated packages can come on the scene.

Materials Impact

For the present, alumina-based systems will meet the need in ceramic packages. Even new ceramic/organic composites of alumina-polyimide that provide lower dielectric constant, while maintaining good heat removal, are now in use.

But the need for more sophisticated materials with enhanced heat removal probably will develop by the late 1980s. Here aluminum nitride, berylium oxide, and silicon carbides may find increasing utilization. For example, silicon carbide substrates have been in use for multichip packages in Japan with the package filled with silicone gel for corrosion protection. Finer particle-size powders will enable smoother ceramic surfaces for finer conductive lines and traces and more space between.

Alternatives to alumina with lower dielectric constant and lower processing temperatures include glasses and cordierite, which may open up full-scale copper cofire technology. In particular, cordierite, with a dielectric constant about half that of alumina and a firing temperature 600°C below that of standard aluminas, is being studied at several laboratories.

As dimensional control and stability are improved, yields are expected to increase. In high-performance, high-lead-count packages, yields are in the range of 10 to 20% today. (It is higher in the DIP products.) The upside potential improvement could be as much as 100% or more in these products based on tolerances moving from the ±0.25 to 1% range to below 0.1%. This will facilitate some significant cost reductions in products like pin grid arrays and fine pitch chip carriers and open up even more market expansion.

Multilayer Ceramic Capacitors

The domestic multilayer ceramic capacitor industry has been one of the strongest and best established in the advanced ceramics field and market growth has been rapid. U.S. shipments in 1981 totaled 3.3 billion units valued at $345 million. By 1984, this more than doubled to 8.2 billion units valued

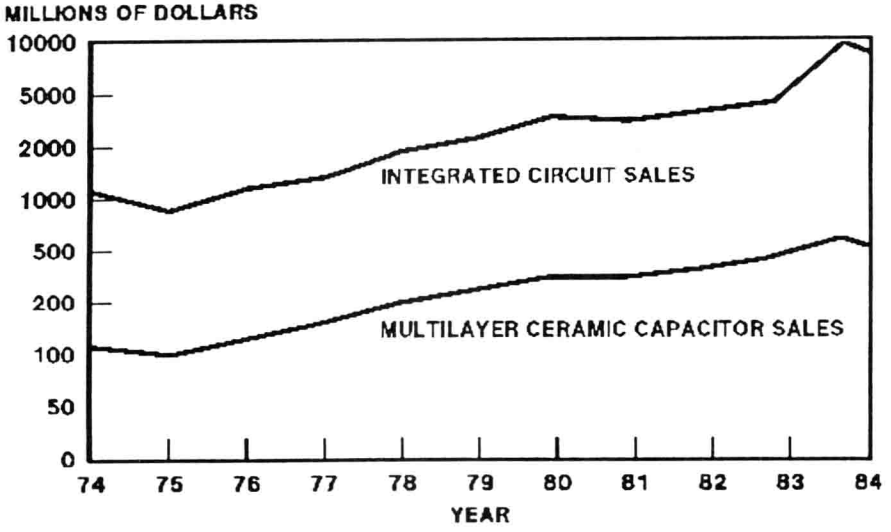

Fig. 1. U.S. integrated circuit and multilayer capacitor sales.

at $610 million. Multilayer ceramic capacitors have been the fastest growing segment of the capacitor market. Multilayer ceramic capacitors in 1973 accounted for only 11% of the 4.6 billion units of all capacitor types shipped. By 1984, this share had grown to 67% of the 12.1 billion total units shipped in that year. From their inception, multilayer ceramic capacitors have averaged between 25 and 35% annual growth.

The growth in multilayer ceramic capacitors has tracked closely with the growth in integrated circuits, with which they are associated for decoupling (Fig. 1). This relationship is expected to continue, with shipments projected to grow at the 15 to 20% per year level to about 20 billion units valued at $1.4 billion (Table II).

Multilayer Ceramic Capacitor Technology

There are three major directions in which multilayer ceramic capacitor technology is expected to move through the end of this decade and into the 1990s:

1. There will be a push toward lower average costs for capacitors at a given level of performance.
2. Improved reliability will be emphasized.
3. It will be necessary to achieve performance levels that ensure that multilayer ceramic capacitors remain compatible with future generations of integrated circuits.

Cost Reduction

The estimated industry average selling price per capacitor has been on a 33% learning curve during the 1970s; that is, each doubling of industry output has been accompanied by a 33% reduction in average selling price. More recently, during the late 1970s and early 1980s, the curve has been flattening out to about a 20 to 25% curve. Some of this decrease may be attributable to increases in noble metal prices, rather than a reduction in the rate of technological change.

Cost reduction has two aspects: one material-related, the other process-related. The major material issue has been the reduction of the more expensive precious metals content, particularly palladium, from the electrodes. The industry has moved to an average industry electrode composition of 70% silver-30% palladium. Efforts are continuing to reduce the palladium content still further. Ultimately, the producers would like to go to systems that use base metals such as lead, nickel, or copper. Limited market penetration has occurred to date because of the lower reliability in service of these capacitors. But with one major capacitor maker reportedly[‡] buying $32 million in palladium, in addition to other precious metals last year, the financial incentive remains very strong to move to cheaper materials systems.

Cost can also be reduced by increasing the volumetric efficiency of capacitance of multilayer ceramic capacitors. As the physical size decreases, the inputs of electrode and dielectric materials decrease. The dielectric layers can be made thinner with a potential reduction in the number of electrodes. However, processing costs could increase in the attempt to achieve sufficiently defect-free, reliable capacitors with thinner dielectric layers, below the 20 to 25 μm typical today. These may also have a greater susceptibility to critical flaws and dielectric breakdown from seeing a higher effective applied voltage.

Process control is under continuing review in order to optimize powder preparation; particle-size distribution; binder burnout; furnace atmosphere; control of condensibles such as bismuth, silver, and lead; and gas partial pressures moving toward the ultimate goal of zero rejects. The standardization of capacitor sizes and configurations to streamline the production process is making possible more continuous large-scale, lower cost, dedicated production runs as opposed to numerous smaller batch runs. In addition, fast firing techniques are being pursued as a means of better controlling microinhomogeneities in critical cation species in the dielectric in order to obtain enhanced properties.

Critical to the effort to reduce precious metal content is the need for lower firing temperature dielectrics compatible with the use of higher silver alloys and base metals in the electrodes, to avoid the oxidation and reactivity of these metals in processing.

Some of the dielectric systems that have been developed include:

1. Highly fluxed, glass-bonded, low-firing barium titanate formulations.
2. Lead-based complex perovskites that exhibit relaxor behavior, i.e., a frequency dependence of the dielectric constant, having much higher dielectric constants than barium titanate, and lower firing temperatures by several hundred degrees, some of which are compatible with full silver electrodes (e.g., lead titanates, lead magnesium niobate, lead iron niobate, and lead iron tungstate, among others).
3. Acceptor (e.g., calcium)-doped barium titanate to be used with a nickel electrode system, being produced now by Murata.
4. PLZT low-loss and low-saturation formulations.
5. Hot uniaxially pressed pure barium titanate, which is compatible with high silver-palladium electrodes.

Reliability Improvements

The reliability of multilayer ceramic capacitors, interpreted as a measure of

[‡]*American Metal Market,* June 11, 1985; p. 11.