科技资料

Digital Computer Technology for Airborne Applications

DIGITAL COMPUTER TECHNOLOGY FOR AIRBORNE APPLICATIONS

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1. SUMMARY

Over the last 30 years silicon has been the driving force behind the major advancements that have taken place in electronics systems and this will continue to be the case for the forseeable future. Electronic system performances and reliabilities will continue to improve at much the same rate and in the period ahead this will be achieved by the efficient design of systems in silicon.

This paper reviews current state of the art silicon technologies and circuits and makes some attempt to view the future.

2. INTRODUCTION

Silicon technology is now entering the submicron era but much more will be required to take full advantage of the technology than the mere scaling of component dimensions. As an example, with shrinking dimensions new component structures will be made possible to improve performance at the device level but in many applications interconnections will be the limiting factor in system performance. To achieve optimum performance it will be necessary to take account of all relevant factors and in many cases new system structures and architectures will be necessary if we are to make full use of advancing technologies.

The technologies and circuits described in this paper are, in the main, those in research, development and early production at Plessey Research, Caswell. They are, however, close to the state of the art in the world scene and give fair representation of current capabilities in silicon.

3. CMOS

CMOS is the mainstream VLSI technology for complex digital functions. A primary reason for this is the low power requirements of CMOS circuits which only consume power in the switching mode and dissipation is often a major factor in determining chip complexities.

3.1 CMOS Technology

The cross section of the Plessey one micron CMOS process is shown in Fig 1. It is a twin well process with trench isolation and up to four layers of metallisation. 7 mask layers are required to fabricate a circuit in this technology prior to metallisation.

In this generation of technology a number of new features have been adopted such as trench isolation, silicided contacts and multi layer metals. These will make it easier to move to submicron dimensions and give significant performance improvements, as illustrated in Table 1 which gives various comparisons between 1.5, 1 and 0.7 micron technologies.

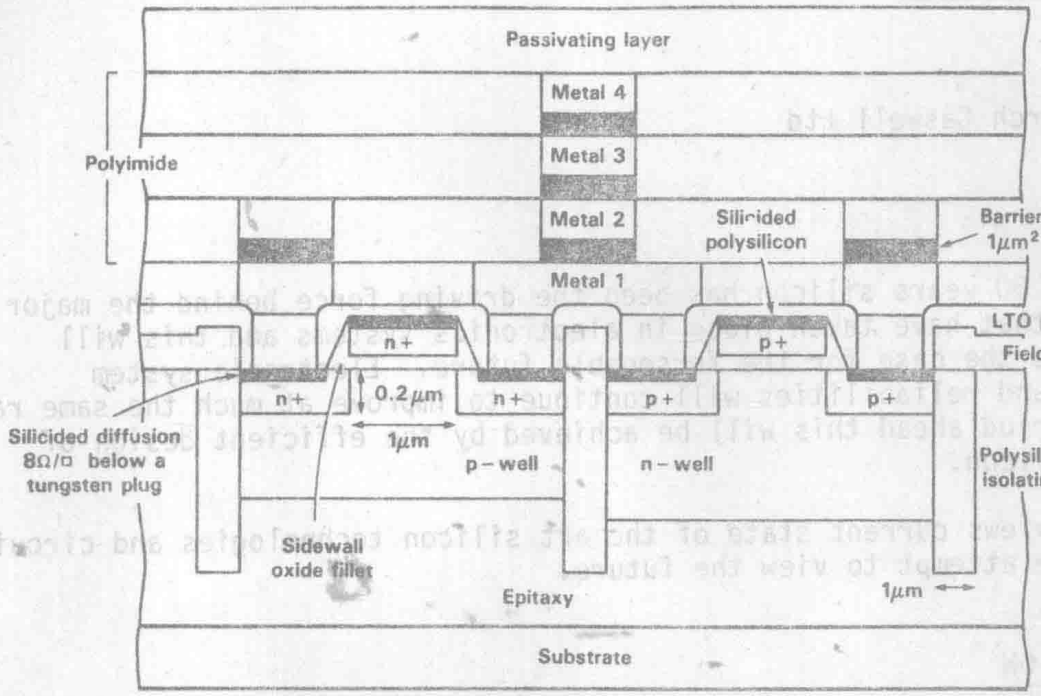


Fig 1. Cross section of one micron CMOS technology

A complete summary of all the new technology features is given in Table 2 which gives a good indication of the efforts required to keep pace with the continuing evolution of silicon technology.

There has also been growing a growing interest in BICMOS in recent times. This provides a bipolar capability within a CMOS technology and is particularly useful for improving the performance of CMOS circuits by providing a high speed interface circuitry both within and external to the chip and a better analogue capability.

1	Minimum feature size	1.5	1.0	0.7	μm
2	Number of metal layers	2	up to 4	up to 4	
3	Multi – layer metal pitch	5.5	3	2	μm
4	Logic gate packing density	760	4110	8400	Gates/mm²
5	Gate delay (NAND with 2 loads)	448	252	167	ps
6	SRAM cell size (6 – translators)	596	126	62	μm²
7	SRAM access time	32 (64K)	15 (0.5M)	11 (0.5M)	ns
8	Analog components	Available	Apr 89	Oct 90	
9	EPROM/EEPROM components	Apr 89	Oct 89	Oct 90	
10	Circuit availability	In volume	Samples	Studies	
11	Production	Roborough	Caswell	Oct 90	

Table 1 Comparison of CMOS technologies

Epitaxial silicon substrates to eliminate latch – up
Trench isolation for high packing density
Advanced well achitecture for improved transistor performance
Thin gate oxide for high transistor gains
Sidewall spacers along gate conductors to reduce gate – drain overlap capacitance
Silicided gate conductor for reduced RC time constants
Drain engineered diffusions to eliminate hot – electron effects
Silicided diffusions to reduce sheet resistance
Barrier metallurgy for long – life current flow
Multi – layer metallisation for high packing density

Table 2 New technology features

3.2 CMOS Circuits

We have long passed the era of simple gate functions and even the early microprocessors. With the ever increasing circuit complexities we now see in catalogues very complex processors and support circuits and also very

complex dedicated functions. In recent times there has also been increasing use of custom circuits where volume requirements justify or where performance requirement necessitate. Custom circuits vary from simple gate arrays to complex cell based circuits.

Table 3 gives a range of custom circuits designed at Plessey Research over recent years using 2 micron CMOS technology. They are all complex digital functions primarily used in digital signal processing applications. Such circuits usually give between one and two orders of magnitude improvement in performance over the same function realised as software on a standard microprocessor. A good example of this is the Pythagoras Processor, a chip photograph of which is shown in Fig 2. This device converts Cartesian data (16 bit Real and Imaginary) into Polar form (16 bit Magnitude and 12 bit Phase) at a 10MHz rate. It is 24k gate complexity and is such a general purpose function that it is now a standard catalogue part.

Chip	Customer	Gates	Speed MHz	Status
16*12 complex number mult	PRL	10800	10	PSL product PDSP16112
16bit FFT butterfly	PRL	13000	10	Complete
Correlator*	PAv	13500	20	In service
2D edge detector	DCVD	9500	22	PSL product PDSP16401
Pythagoras* processor	DCVD	24000	10	PSL product PDSP16330
Pattern* recognition IC	DCVD	5000	1	Sampling
16*16 complex number mult	PSL	13300	10	Evaluation PDSP16116

* *Right first time*

Table 3 Range of 2 micron CMOS digital circuits

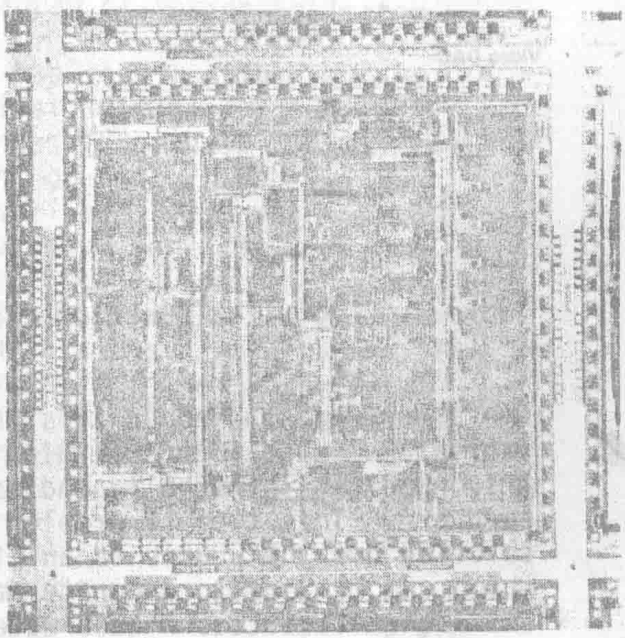


Fig 2 Pythagoras Processor

The world is not, of course, all digital and Table 4. shows some mixed analogue and digital circuits designed over the same period of time. The PSLAC is a subscriber line audio circuit used in digital telephone exchanges and the input has to handle 93dB of analogue dynamic range.

Looking to the future, as we have already seen, technology is going to offer the capability of ever more complex circuitry. If at the system level we are going to take full advantage of this, we will need ever more efficient design techniques and, in DSP for example, the development of algorithms that translate efficiently into silicon hardware.

An example of this has been the work carried out in the Alvey Dedicated VLSI Processors Project (Alvey 013) researching commonly occuring problems that can be addressed using regular array structures. Array structures have the potential for the adoption of rapid design techniques in that only a small number of processing elements need to be designed and interconnection problems can be minimised.

Chip	Customer	Gates	Speed MHz	Status
PSLAC	PSL	15000 + Analog	2	Entering production at PSL
Receptor chip B	PSL/ AT&E	7000 + Analog	0.133	In demonstrator
7bit Video ADC	PSL	650	30	Evaluation
8bit Video DAC	PSL	600	50	PSL product MV95408

Table 4. CMOS mixed function circuits

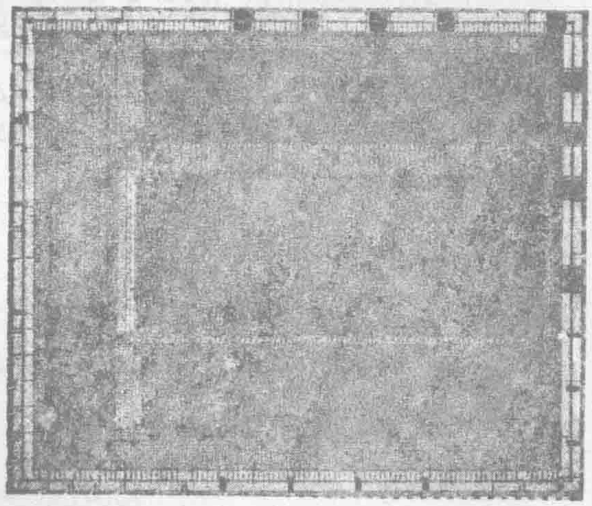
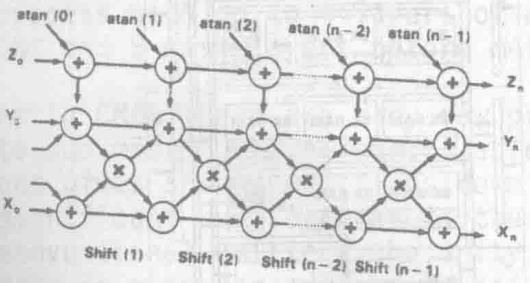


Fig 5. Chip photo of Asynchronous Time Division Switch

One algorithm studied in this programme has been a Co-ordinate Rotation Digital Computer (CORDIC) which is capable of producing a range of trigonometric, hyperbolic and exponential functions from relatively simple hardware. This type of problem does not have an intuitively regular solution but the CORDIC is an iterative algorithm based on vector rotations which can be used to generate many scientific functions and, interestingly, the mathematical techniques date back to the 17th century. The chip architecture developed is shown in Fig 3 and is, as far as is possible, a straight translation of the algorithm into silicon. Compared with conventional ways of realising similar functions, look up ROM tables, it uses less area of silicon, gives better performance and is more flexible.

One other type of algorithm studied in the same programme is a video picture motion estimator used in video codecs for bandwidth compression of video signals. Various estimation algorithms exist and the majority are based upon matching blocks of pixels between frames. This problem has considerable array properties inherent in it and the solution selected is the 'brute force' block matching algorithm which results in an architecture shown in Fig 4. This architecture makes possible real time video motion estimation on a single VLSI chip.



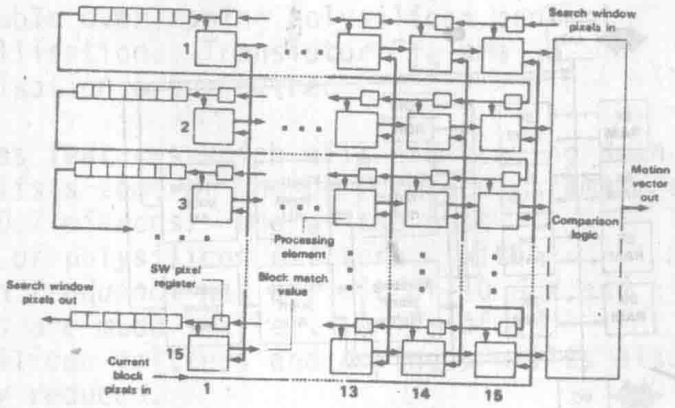


Fig 3 CORDIC architecture

Fig 4 Block diagram of Motion Estimator

Telecommunications is an application area that has seen massive changes over a relatively short period of time and digital switching is now well established. In System X, large digital exchanges (DSS) have 2048 ports operating at 2 Mb/s each carrying 32 connections of 64 kb/s. Using concentrators this will serve over 100,000 subscribers. However, looking to the future, with the predicted growth in broadband services, new switching systems will be necessary and there is growing interest in higher frequency Asynchronous Time Division (ATD) switches. In the one micron CMOS Alvey programme an ATD demonstrator switch chip has been designed (Fig 5) which handles 8 ports at 150 Mb/s, or one quarter of the System X DSS capacity, on a single chip. The chip handles packets of data containing voice, data and video information. The requirements for broadband services may as yet be uncertain but the technology will certainly be in place to provide them.

Fault tolerant techniques are also likely to grow in importance with increasing chip complexities. Such techniques can be used both to improve manufacturing yield and to provide means of in service fault detection and correction. They provide the potential to both reduce cost and increase reliability.

Fault tolerance techniques have been researched on the Alvey Architecture programme (073) where it has been demonstrated that fault tolerance can be achieved by the use of redundant hardware which can be switched in and out of the operational sections of a chip as required. Fault tolerant cells that have been designed include multipliers, RAMs and error detection and correction circuits. These have been proven in test chips and have been used in chips designed as project demonstrators. One of these is a fault tolerance DSP processor and the architecture of this is shown in Fig 6. and a floor plan of the logic showing the redundant parts is given in Fig 7.

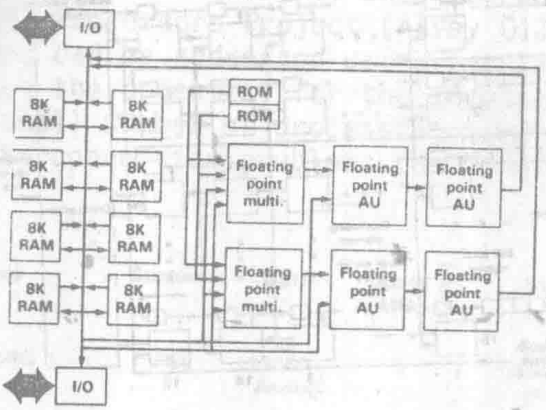


Fig 6 DSP block diagram

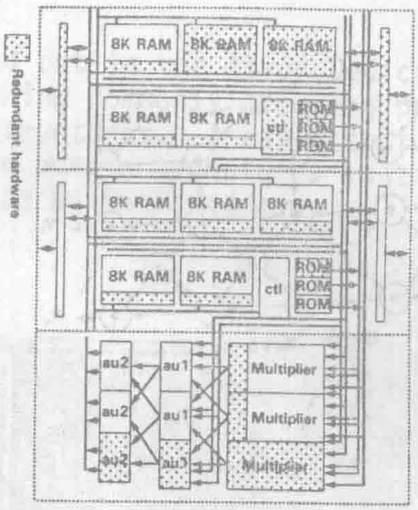


Fig 7 DSP block diagram with redundant parts

4. BIPOLAR

Bipolar has always been the high performance silicon technology in terms of both analogue and high frequency digital circuits. This is unlikely to change and GaAs will remain a complementary technology offering lower noise performance in high frequency analogue circuits and a superior microwave integrated circuit capability. In high frequency digital systems silicon bipolar technology is likely to maintain its dominant position. Over recent years the performance of high frequency digital systems has been limited by inter package interconnection delays but system performances can now be much improved if full advantage is taken of the circuit complexities achievable with state of the art bipolar technologies.

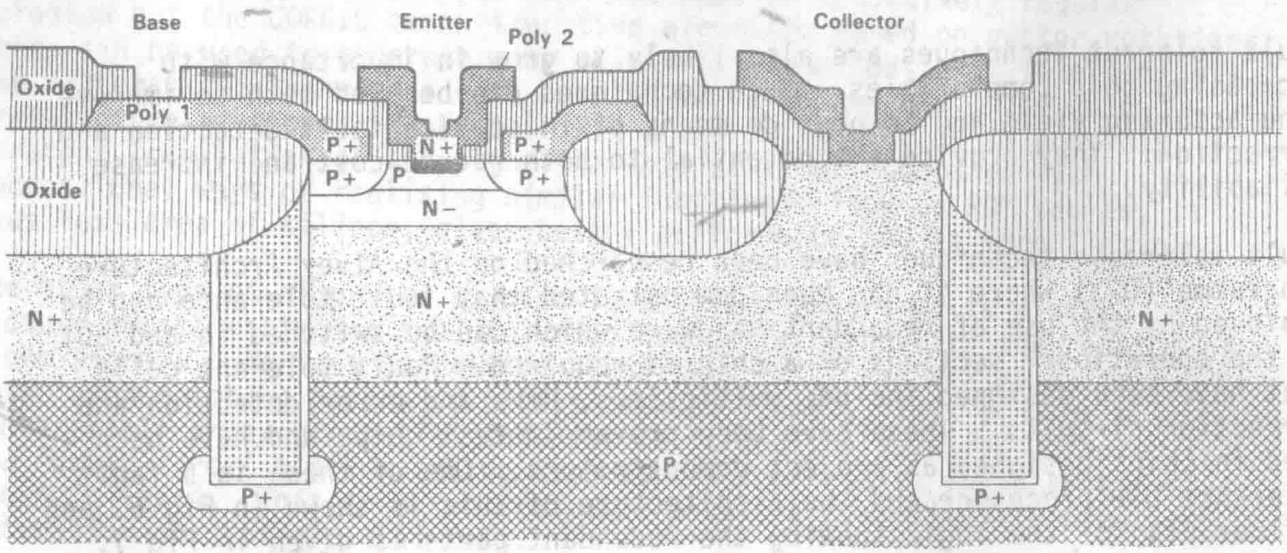


Fig 8 Cross-section of a double polysilicon trench isolated bipolar transistor

4.1 Bipolar Technology

The cross section of the Plessey one micron bipolar technology is shown in Fig 8. It is a trench isolated, double overlapping polysilicon contact process with up to 4 layers of metallisation. Transistor F_{Ts} are 18 GHz and 8 mask layers before metallisation are required.

As in CMOS there are many new process features which will aid scaling down to sub micron dimensions. Table 5 lists some of the performance parameters and gives some predictions down to 0.7 microns. One of the most significant new features is the use of polysilicon emitters. With conventional emitters the unity gain frequency has a limit of 10 GHz and this is much degraded as transistors are made smaller. An F_T of 25 GHz is readily available with polysilicon emitters and doping profiles also permit transistor sizes to be easily reduced.

A second important new feature is the use of double overlapping polysilicon contacts which reduces contact resistances and collector base capacitances significantly. The use of both these features has resulted in a performance improvement of a factor 3 over the last 5 years and circuits operating in excess of 10GHz and ring oscillator gate delays of 37.5 ps have now been achieved.

4.2 Bipolar Circuits

The combination of high frequency performance and the circuit complexities now achievable with bipolar technologies opens up new system opportunities. Already in the RACE (Research into Advanced Communications for Europe) programme research is being carried out on high performance bipolar circuits for low cost customer access at 560 M b/s and transmission systems with data rates of 10 G b/s.

In computing system speeds are being much increased by the use of complex bipolar gate arrays (up to 16 k gates) and high speed dedicated functions. The first small, 240 gates array designed on the Plessey one micron process offers gate delays of 80 ps. In fact chip complexities of 20 k - 30 k gates are now possible but in many high speed applications dissipation rather than yield will be the limiting factor. Certainly single chip bipolar RISC processors with performance capabilities well in excess of 100 MIPs are now possible.

	HE1	HE	HG	Units
Minimum feature size	1	1.0	0.7	micron
Number of metal layers	3	3 or 4	3 or 4	
Multi-layer metal pitch	5	4	3	micron
Logic gate packing density	20	30	40	K gates/chip
Ft	14	20	25	GHz
Max. toggle frequency	6.5	10.5	16	GHz
Gate delay	50	40	30	ps
Status	In development first supplies June 87	In research first samples Oct 88	Inresearch first samples Mid 90	
Production start up	Dec 88	Mar 89	Mid 90	

Table 5 Bipolar technology performance predictions

Maximum Clock Rate	>2.5GHz
Output Waveform	SINE, TRIANGULAR SQUARE
Output Phases	I and Q, TRUE AND COMPLIMENT
Output Frequency	1 Hz to 500MHz
Channel Spacing	1 Hz
Close to Carrier Noise	-135 dBc/Hz at 10 kHz

Table 6 DFS parameters

One example of a high frequency medium complexity (~ 5000 components) is a Direct Frequency Synthesiser (DFS) designed as a demonstrator circuit on the Alvey one micron bipolar technology programme. The DFS synthesises the required waveform by feeding a DAC with the digital words stored in a ROM and this allows any arbitrary periodic waveform to be generated. Waveforms can be generated easily with a fixed phase relationship and the frequency of the synthesised signal can be varied in a coherant manner over a very wide range of frequencies with a switching time between frequencies of 20 ns. A list of the major devices parameters is given in Table 6. Functioning circuits are now in evaluation and operate with a clock frequency of 2 Gb/s. A block diagram of the chip is shown in Fig. 9 and a chip photo in Fig 10. This circuit is a good example of a new type of product being introduced when technology becomes available to make the product economical and give the required performance.

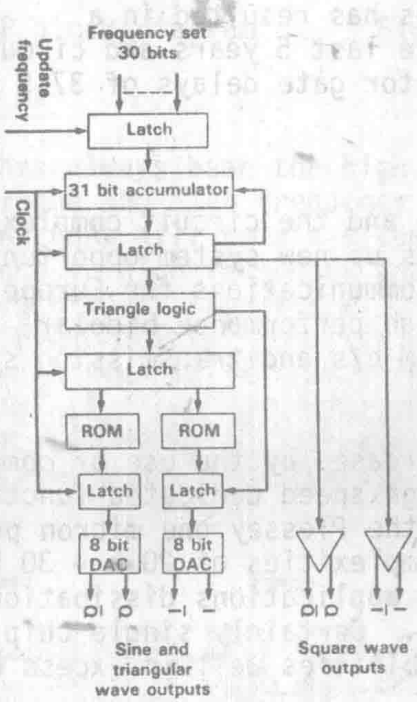


Fig 9 Block diagram digital frequency synthesiser

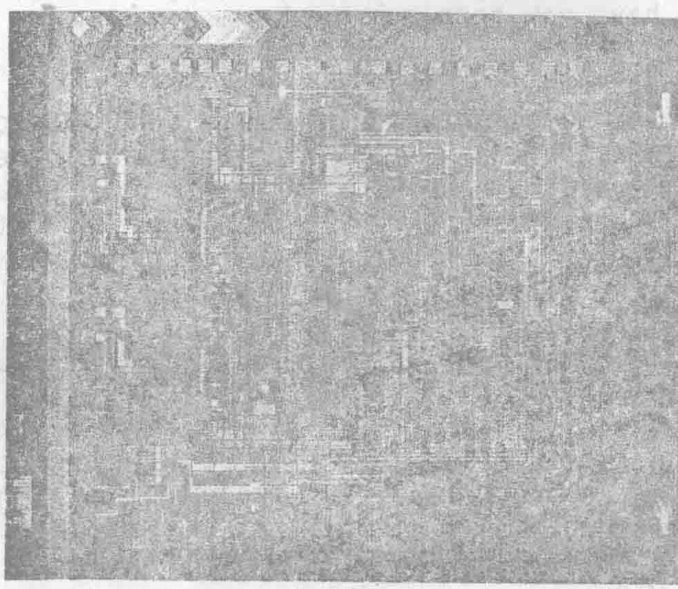


Fig 10 Chip photo digital frequency synthesiser

A number of circuits have been developed and are under development for Digital Radio Frequency Memory (DRFM) operating at 1.3 GHz. These include an 8 bit universal shift register and various memory devices where the key objective has been to meet the required speed performance with the lowest power dissipation.

Bipolar technology also makes possible high performance data conversion and analogue circuits. Circuit performances achievable include 8 bit DACs with settling time of 1 ns, 12 bit 20 MHz ADCs and wideband amplifiers with bandwidths well in excess of 2 GHz. Also demonstrated in recent years has been silicon microwave diode arrays operating in the 60 GHz region. Bipolar technology has always offered more scope for circuit innovation and this is demonstrated by the evolution of circuit techniques over the last 20 years. With sub micron technology it is likely that the scope for circuit innovation will increase with the possibilities of new device

structures. An example of this is research now being carried out at Caswell into the use of bipolar p-channel JFETS as active loads. This is not a new idea but it was not possible to fabricate JFETs with adequate performance on previous generation technologies. It now has to be establisned whether adequate devices can be made consistently but if they can it will be possible to put together on the same chip complex low power logic, similar to CMOS, with high speed digital and analogue circuits. The basic inverter is shown in Fig. 11.

5. DESIGN TECHNIQUES

There is always, and will always be, a need for more sophisticated CAD tools to ensure that design timescales keep within reasonable limits and first time working circuits are achievable. Such tools are continually in development to keep pace with technology and once proven and established in specialist silicon design environments are often added to CAD packages available to system users to facilitate the design of more sophisticated semi-custom circuits.

With increased complexity circuits at this time there is a need for more sophisticated high level CAD tools and it is likely in the future that such tools will become more application specific.

The problems of testing complex and high performance devices must also be addressed at the design phase and built in self test techniques are now in common use. All of the comolex CMOS circuits referred to in this paper use built in self test techniques which vary with chip function and architecture and some design methods provide automatic overlay of built in self test. If treated as a black box exhaustive testing can be uneconomical and built in self test usually breaks the circuits into seperate functions which can be addressed individually. The penalty paid in increased chip area, and it is in the design phase that it is necessary to address the compromises to be made between manufacturing, test and service costs. Certainly very different criteria can apply depending on the circuit application and volumes required.

Very high frequency testing of devices which are themselves close to the limit of performance will always remain difficult. Perhaps the first application of such devices is in test equipments.

6. PACKAGING AND INTERCONNECTION

Increasing chip complexities and higher system performances combine to make packaging and interconnect problems ever more difficult. Together with the availability of higher speed there is a growing requirement for packages with larger pin counts. As a rule of thumb modest complexity circuits operating at below 2 GHz can use chip carriers. With high speed RAM devices where the effective operating speed is less than 300MHz conventional D.I.L. packages have been used but approximately ¼ of the total access time can be accounted for by delays within packages. To accommodate operation at higher frequencies specialist packages will be required and high pin circuits and low thermal resistance will be necessary.

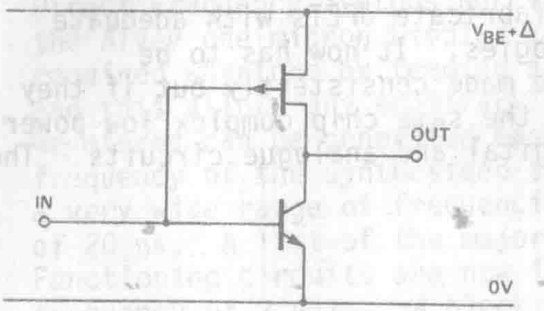


Fig 11 JFET inverter

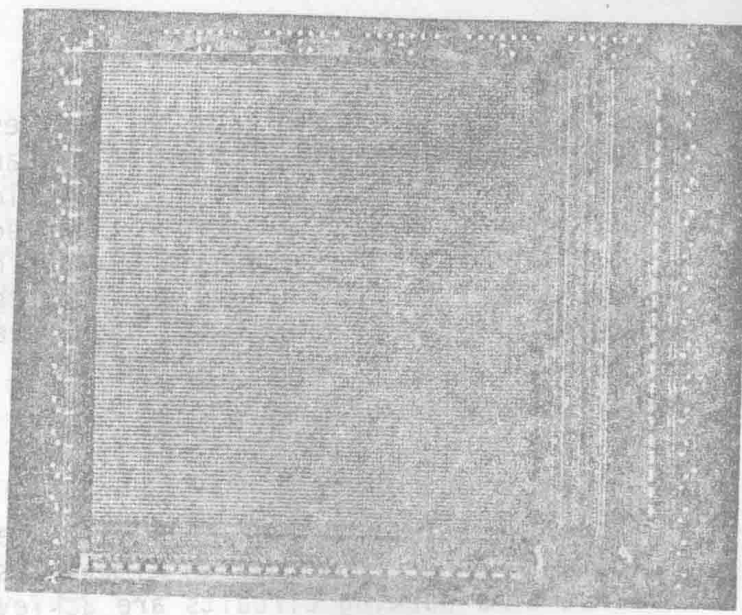


Fig 12 Chip photo of 100x100 thermal read-out array

Multi chip packaged assemblies will find greater application in the future and silicon is a potential substrate material to carry chip interconnections. At this time solder bump technology appears to hold much potential for mounting chips on substrates. The technique has been successfully demonstrated in a pyroelectric imaging system at Caswell. Fig 12 is a chip photo of a 100 X 100 read out array showing all the interconnecting pads and Fig. 13 is a photo of a assembled imager with all interconnections working. Fig. 14 illustrates the bonding process.

In large systems the use of optical interconnections, removing the problems of E/M noise and crosstalk, is common between sub-systems and is also used in some applications for inter rack wiring. Certainly optical interconnects remove any bandwidth constraints.

Even within the silicon chip interconnections will be the dominant factor in achieving higher performances and the use of multi layer interconnections with well controlled distribution of both data and power will be mandatory.

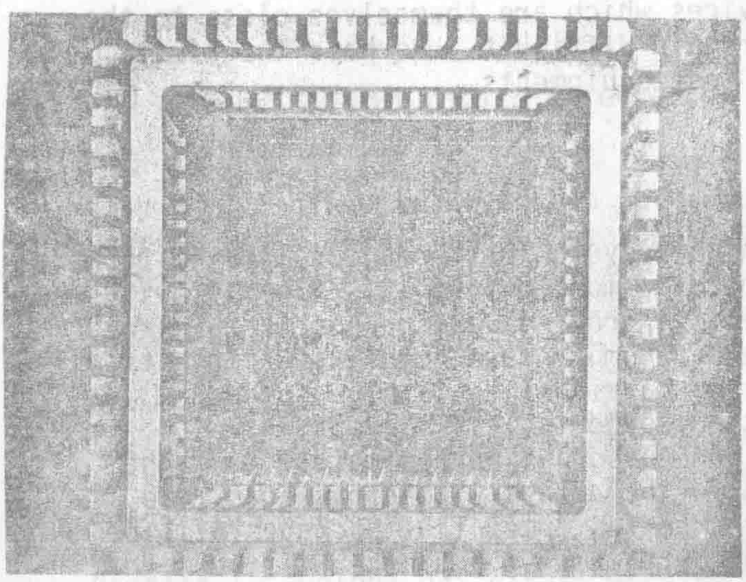


Fig 13 Thermal imager completed assembly

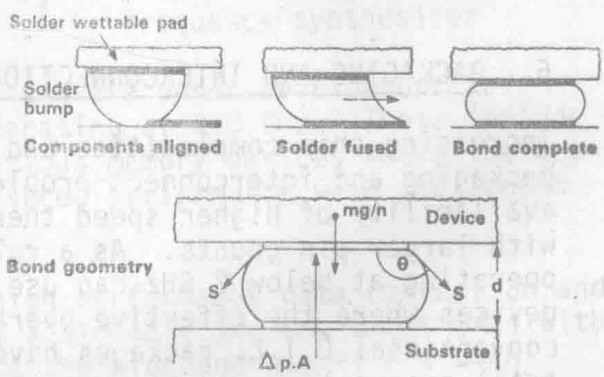


Fig 14 Solder bump technology

7. FUTURE DEVELOPMENTS

Many improvements and additions to current technologies will take place as component dimensions reduce to a fraction of a micron.

At this point in time the most promising new technique is the use of high energy oxygen implantation to produce wafers of silicon on insulator (SOI) This technique has been under investigation for some years but results reported recently are very encouraging. There have been reports of CMOS circuits operating up to 2 GHz and 16 K RAMs, with yields as high as bulk silicon. More evidence is yet needed but if these results can be achieved consistently then SOI will offer both improved performance and lower processing costs.

It is probable that photolithographic techniques will continue to be used to around 0.3 micron and below this current opinion is that electron beam direct write will be favourite. The problem here is achieving the required resolution in a time that is compatible with economic wafer processing.

In parallel with technology developments there will be continuing need for innovation at the device, circuit and chip architecture level if full exploitation of silicon technology is to be achieved. Certainly in CMOS we will see complexities well in excess of 1 million equivalent gates and in bipolar gate speeds of the order of 10 ps and chip clock frequencies in excess of 20 GHz over the next 3-5 years.

8. CONCLUSIONS

Whatever new breakthroughs lie ahead, in terms of new materials or techniques, silicon is only part way through its evolutionary development. For many years yet it will offer the potential for improved system performance and cost reductions and will continue to open up new application opportunities.

Tomorrow's equipment will be as revolutionary in today's environments as today's equipment would have been twenty years age.

9. ACKNOWLEDGEMENT

The author would like to acknowledge the efforts and achievements of all his colleagues, past and present, in the Silicon Division at Plessey Research Caswell, where nearly all of the technologies and circuits described in this paper emanate from.

Avionic Systems Architecture

Professor D K Hitchins, City University
D O'Dwyer, EASAMS Ltd