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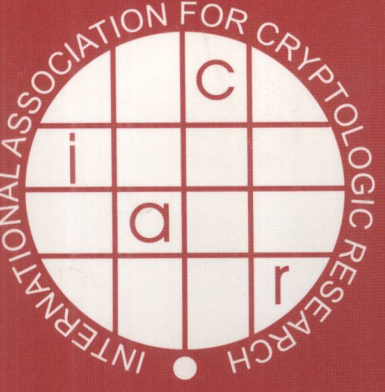

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Preface

These are the proceedings of the Eighth Workshop on Cryptographic Hardware and Embedded Systems (CHES 2006) held in Yokohama, Japan, October 10-13, 2006. The CHES workshop has been sponsored by the International Association for Cryptographic Research (IACR) since 2004. The first and the second CHES workshops were held in Worcester in 1999 and 2000, respectively, followed by Paris in 2001, San Francisco Bay Area in 2002, Cologne in 2003, Boston in 2004 and Edinburgh in 2005. This is the first CHES workshop held in Asia.

This year, a total of 112 paper submissions were received. The review process was therefore a delicate and challenging task for the Program Committee members. Each paper was carefully read by at least three reviewers, and submissions with a Program Committee member as a (co-)author by at least five reviewers. The review process concluded with a two week Web discussion process which resulted in 32 papers being selected for presentation. Unfortunately, there were a number of good papers that could not be included in the program due to a lack of space. We would like to thank all the authors who submitted papers to CHES 2006.

In addition to regular presentations, we were very fortunate to have in the program three excellent invited talks given by Kazumaro Aoki (NTT) on "Integer Factoring Utilizing PC Cluster," Ari Juels (RSA Labs) on "The Outer Limits of RFID Security" and Ahmad Sadeghi (Ruhr University Bochum) on "Challenges for Trusted Computing." The program also included a rump session, chaired by Christof Paar, featuring informal presentations on recent results.

We are very grateful to the Program Committee members and to the external reviewers for their hard work. Special thanks are also due to the members of the Local Committee: Akashi Satoh (Secretary - IBM Japan Ltd.), Toru Akishita (Sony Corporation), Tetsuya Izu (Fujitsu Laboratories Ltd.), Masanobu Koike (Toshiba Solutions Corporation), Natsume Matsuzaki (Matsushita Electric Industrial Co., Ltd.), Shiho Moriai (Sony Computer Entertainment Inc.), Sumio Morioka (NEC Corporation), Hanae Nozaki (Toshiba Corporation), Kenji Ohkuma (IPA), Katsuyuki Okeya (Hitachi Ltd.), Shunsuke Ota (Hitachi Ltd.), Yasuyuki Sakai (Mitsubishi Electric Corporation), Junji Shikata (Yokohama National University), Daisuke Suzuki (Mitsubishi Electric Corporation), Yukiyasu Tsunoo (NEC Corporation), Takanari Ueno (IPA), Takashi Watanabe (Hitachi Ltd.) and Atsuhiro Yamagishi (IPA), for their strong support.

Special thanks go to Tsutomu Matsumoto, the General Chair and local organizer for his extensive efforts to bring the workshop to the beautiful historic city of Yokohama, Japan. The Publicity Chair Çetin Kaya Koç was always very helpful and patient at all stages of the organization. Jens-Peter Kaps helped us as our dedicated webmaster for maintaining the Web review system.

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We would also thank the corporate financial supporters, Cryptography Research, Inc., RSA Security Japan Ltd., Fujitsu Limited, IBM Corporation, Information Technology Promotion Agency, Japan (IPA), Initiative for Research on Information Security, Mitsubishi Electric Corporation, NTT Corporation, Renesas Technology Corp., Toshiba Corporation and Yokohama National University. Obviously CHES2006 was not possible without these supporters.

Lastly we would like to thank the CHES Steering Committee members for their hearty support and for giving us the honor of serving at such a prestigious conference.

October 2006

Louis Goubin
Mitsuru Matsui

8th Workshop on Cryptographic Hardware and Embedded Systems

October 10 – 13, 2006, Yokohama, Japan
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Template Attacks in Principal Subspaces

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Abstract. Side-channel attacks are a serious threat to implementations of cryptographic algorithms. Secret information is recovered based on power consumption, electromagnetic emanations or any other form of physical information leakage. Template attacks are probabilistic side-channel attacks, which assume a Gaussian noise model. Using the maximum likelihood principle enables us to reveal (part of) the secret for each set of recordings (i.e., leakage trace). In practice, however, the major concerns are (i) how to select the points of interest of the traces, (ii) how to choose the minimal distance between these points, and (iii) how many points of interest are needed for attacking. So far, only heuristics were provided. In this work, we propose to perform template attacks in the principal subspace of the traces. This new type of attack addresses all practical issues in principled way and automatically. The approach is validated by attacking stream ciphers such as RC4. We also report analysis results of template style attacks against an FPGA implementation of AES Rijndael. Roughly, the template attack we carried out requires five time less encrypted messages than the best reported correlation attack against similar block cipher implementations.

1 Introduction

Since their first public appearance in 1996 [6], side-channel attacks have been intensively studied by the cryptographic community. The basic principle is to monitor one (or more) unintentional channels that leak from a device such as a smart card and to match these observations with a key-dependent leakage prediction. This channel is usually monitored thanks to an oscilloscope that samples a continuous analog signal and turns it into a discrete digitalized sequence. This sequence is often referred to as a trace.

Recently, a probabilistic side-channel attack, called the Template Attack (TA), was introduced [2]. This attack was originally mounted to target stream ciphers implementation. In this context, the attacker can only observe a single use of the key, usually during the initialization step of the cipher. As it is not possible to generate different leakages from the same secret key (e.g., corresponding to different plaintexts), TAs were purposed for a more efficient way of retrieving information from side-channel traces.

There are three main reasons that make TAs more efficient than previous approaches to exploit side-channel leakages. First, TAs usually require a profiling step, in order to build a (probabilistic) noise model of the side-channel

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that can be used to capture the secret information leaked by a running device. Second, TAs usually exploit multivariate statistics to characterize the dependencies between the different time instant in the traces. Finally, TAs use maximum likelihood as similarity measure, that can capture any type of dependency (if the probabilistic model is found to be adequate), whereas, for example correlation analysis only captures linear dependencies [1]. In general, the cost of these improvements is a reduction of the adversarial flexibility. For example, Hamming weight leakage models can generally be used for any CMOS devices while template attacks profile the leakage function for one particular device.

TA relies on the hypothesis that leakage information is located in the variability of the leakage traces. In order to recover the secret, one has thus to focus at the time instants where the variability is maximal. However, in practice it is not clear how many and which moments exactly are important. The attacks are therefore based on heuristics, which specify these quantities according to some prior belief. For example, it is common to force the successive, relevant time instants to be one clock cycle distant.

The main contribution of this work is that we take TA a step further. Instead of applying TA directly, we first transform the leakage traces such that we are able to select the relevant features (i.e. transformed time instants) and their number automatically. Meanwhile, we do not need to determine a specific feature interdistance. Of course, when performing TA after transformation, we still take the correlations between the features into account. Now, in order to find a suitable transformation consider again ordinary TA. It is assumed that the secret information leakage is mainly hidden in the local variability of the mean traces. If this hypothesis is valid, it would be more appropriate to take the optimal linear combination of the relevant time samples and perform TA in the principal subspace of the mean traces. We call this approach principal subspace-based TA (PSTA). A principal subspace can be viewed as a lower dimensional subspace embedded in the data space[1] where each coordinate axis successively indicates the direction in which the data have maximal variability (or variance).

A standard statistical tool for finding the principal subspace of a data set is principal component analysis (PCA) [5]. PCA performs an eigendecomposition of the empirical data covariance matrix in order to identify, both, the principal directions (eigenvectors) and the variance (eigenvalues) associated to each one of them. However, practical issues may arise in the context of PSTA, as the dimension of the traces is much larger, (typically $\mathcal{O}(10^5)$) than the number of traces (typically $\mathcal{O}(10^3)$). Therefore, we propose to use a variant of PCA that is more suitable in this situation (see Section 3.1 for further details).

An attractive feature of PSTA is that the projected traces are aligned with the directions of maximal variance. These directions are nothing else than a weighted sum of all the time instants, the weights being determined such that the data variability is preserved after projection. So, in contrast to TA, which selects a relevant subset of time instants according to a heuristic, PSTA determines first the optimal (in terms of maximal variance) linear combination of these time

[1] Here, the data space is the space in which the leakage traces live.

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