FORMAL VLSI SPECIFICATION AND SYNTHESIS

VLSI Design Methods-I

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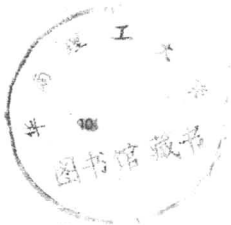
Proceedings of the IFIP WG 10.2/WG 10.5 International Workshop on
Applied Formal Methods for Correct VLSI Design
Sponsored by IMEC, Houthalen, Belgium, 13–16 November, 1989

Edited by

LUC J.M. CLAESEN
Interuniversity Micro-Electronics Center
& Katholieke Universiteit Leuven
Leuven, Belgium



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Preface

Applied Formal Methods For Correct VLSI Design.

The international workshop entitled *"Applied Formal Methods For Correct VLSI Design"* has been organized by IMEC, the Interuniversity Micro Electronics Center in Leuven (Belgium), in cooperation with IFIP (International Federation for Information Processing) working group 10.2 *"System Description and Design Tools"* and working group 10.5 *"Very Large Scale Integration"*. The workshop took place in the "Hengelhoef" Congress Village in Houthalen Belgium from 13 to 16 November 1989. The workshop has been followed by a visit to IMEC on 17 November 1989.

Functional and behavioral verification of the correctness, is the bottleneck in current VLSI design systems. For economical reasons, designs of VLSI circuits must be completely validated before manufacturing. Current VLSI validation is mainly done through extensive simulation. The emerging alternative is based on formal design and verification methods, that guarantee correctness.

At this workshop, researchers interested in formal hardware design methods that are applicable for correct VLSI design, from both industries and universities, have been brought together. Invited overview speaches, regular presentations and a poster session on recent research achievements, as well as several demonstrations of CAD-tools making use of formal methods have been organized.

The workshop has been attended by 180 participants from 18 different countries in America, Asia and Europe.

Two invited speaches have been given by prof. Randal E. Bryant *(Symbolic Analysis and Verification of MOS Circuits.)* and by prof. Warren Hunt Jr. *(The Formal Design and Verification of Hardware Based on the Boyer-Moore prover.)*.

In response to the *call for papers* 95 contributions have been received. Every contribution has been reviewed by three independent reviewers who have given their opinion on the suitability of the proposed topics for the focus of this workshop. From these, 30 have been selected for presentation in the regular sessions and 20 have been presented in a poster session.

I hereby want to thank the reviewers for their careful reviews and for the return of the review reports in time, taking into account the holiday period in which the reviews had to be carried out. The selection process has been guided by the overall recommendations of the reviewers.

The emphasis has been put on "applied" methods, methods that are illustrated with realistic design problems, methods that have large potential future application to large VLSI design, methods that are implemented in software prototypes, original and high quality contributions. Special attention has also been given to contributions that relate their work to the benchmarks that have been distributed.

Benchmark Examples.

In order to be able to compare and illustrate specific aspects of formal design systems, a set of benchmarks for formal verification and design between RTL specification and hardware implementation have been made available to interested participants.

The first common application is the design of a "Min-Max"-block[1] which has been distributed to illustrate a specific design method or formalism. The main emphasis, with the "Min-Max" application, is on using a common known problem to be used to explain specific approaches, and not so much on the complexity of the problem.

The second class of applications consists of a number of benchmarks[2] for tautology checkers as are often available in formal verification systems. These two benchmark types have been the subject of special sessions.

Demonstration Sessions

In this conference on "*Applied* Formal Methods For Correct VLSI Design" special attention has been given to demonstrations of CAD tools and prototype tools that illustrate recent research results and/or original realizations in the area of formal hardware design and verification methods. During the workshop computer workstations have been made available to the participants for demonstrations to be organized on an individual basis during free time.

Besides the continuous possibility for demonstrations, specific sessions have been organized every day from the second day on. Each demonstration session had a number of prepared demonstrations, together with a short introduction to the demonstration on posters and/or transparancies. The participants have been subdivided in groups and were able to visit all the demonstrations in a synchronized way. There have been presented 25 operational demonstrations in these sessions.

"Organized demonstrations" in special sessions is probably a new event on conferences, and requires more involvement and preparation of the presenters. The concept has been received very well by the participants. I hereby want to thank all of the participants that have presented and prepared for these demonstrations. Special thanks go to Diederik Verkest, who carefully

[1] see: D. Verkest, L. Claesen, H. De Man, "Special Benchmark Session on Formal System Design", in *Formal VLSI Specification and Synthesis*, edited by L. Claesen, North-Holland Publ. 1990.

[2] see: D. Verkest, L. Claesen "Special Benchmark Session on Tautology Checking", in *Formal VLSI Correctness Verification*, edited by L. Claesen, North-Holland Publ. 1990.

did the special arrangements and the intensive preparatory work for the successful organization of the demonstrations.

About this book: Formal VLSI Correctness Verification.

The participants proceedings for the workshop on "Applied Formal Methods For Correct VLSI Design" contained the papers in the order of the presentations. For the final version of the proceedings the decision has been made to split the topics in two parts, that are the subjects of two books published by Elsevier North-Holland Publ.:

1. Formal VLSI Specification and Synthesis.
2. Formal VLSI Correctness Verification.

The subdivision of the two topics is mainly based on a top-down (synthesis) and bottom-up (verification) approaches in VLSI design and verification.

Formal VLSI Specification and Synthesis concentrates on specification formalisms and constructive design methods that guarantee correctness of what is being designed. The papers focus either on transformational or guided synthesis design methods that start from a specification and transform the specification into implementations in a correct way. General theorem prover based methodologies, as well as dedicated algorithms for the design of regular array structures are presented.

Formal VLSI Correctness Verification highlights the methodologies for verifying the correctness of design implementations in a bottom-up way. Abstraction levels from transistor level, over sequential machines and register transfer level are presented. A specific chapter on tautology checking presents, using the same benchmarks, efficiency comparisons of eight different methods for tautology checking. Boyer-Moore and HOL theorem prover based hardware verification methods are the subject of the last two chapters.

Acknowledgements.

To conclude I want to thank everyone who has contributed to the succes of the *Applied Formal Methods For Correct VLSI Design* workshop: the paper contributors, the program committee, the local organizing committee, the sponsors, the reviewers, the participants, the IFIP WG 10.2 and 10.5 members and many others. Finally I want to give special thanks to prof. Hugo De Man and prof. Roger Van Overstraeten, for their stimulation and support in the organization of this international conference within the scope of IMEC.

Luc J.M. Claesen

Conference organization.

Workshop Organizer:

Luc Claesen
Interuniversity Micro Electronics Center
& Katholieke Universiteit Leuven
Kapeldreef 75,
B-3030 Leuven (Belgium)
e-mail: claesen@imec.be

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Apollo Computer & Hewlett-Packard
I.B.M. Belgium
Mentor Graphics
SUN Microsystems

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Apollo Computer
Digital Equipment Corporation
Hewlett-Packard
SUN Microsystems

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P. Van Bekbergen
C. Van Berkel
V. Van Dongen
J. Van Sas
D. Verkest
J. Zegers

Demonstrations at the workshop.

"LOVERT, VERTICO"
A.Bartsch, H.Eveking, H.-J. Faerber, J. Pinder, U.Schellin, T. H. Darmstadt

"Using TACHE for proving circuits."
C. Bayol, J-L. Paillet, Univ de Provence

"STAT!"
J.Benkoski, M.Chew, A.Strojwas, Carnegie Mellon Univ.

"System SWIVER for verifying asynchronous circuits."
E.Cerny, P.Rioux, C.Berthet, Univ de Montreal

"CATHEDRAL-II"
H.De Keulenaer, S. De Troch (IMEC)

"The HOP system"
G. Gopalakrishnan, Univ. of Calgary

"LAMBDA"
R. Harris, M. Fourman, Abstract Hardware Ltd.

"The Boyer-Moore Theorem Prover"
W. Hunt, B. Brock, Computational Logic Inc.

"T.U. Eindhoven Verification tools"
G. Janssen, G. de Jong, Tech. Univ. Eindhoven

"RLEXT: manual optimization program"
D. Knapp, Univ. of Illinois

"HIFI"
A. de Lange, Technical Univ. Delft

"The formal verifier PRIAM"
J-C Madre, Bull

"Functional extraction of hierarchical sequential systems."
F. Martinolle, B. Sousal, J.-C. Geffroy, Inst. Nat. Sciences Appliquées.

"Maple"
F Mavaddat, Univ. of Waterloo

"Fast Tautology Checking Using Shared Binary Decision Diagram"
S. Minato, N. Ishiura, S. Yajima, Kyoto Univ.

"The Edinburgh Concurrency Workbench"
F. Moller, University of Edinburgh

"Formal proof of "Min-max" benchmark from CASCADE in Boyer-Moore"
L Pierre, Univ de Provence

"The NODEN hardware verification suite."
C. Pygott, RSRE

"Non-standard interpretation of HDL's"
S. Singh, University of Glasgow.

"CLIO"
M.K. Srivas, Odyssey Research Associates

"Verification of VLSI Circuits using LP"
J. Staunstrup, Technical Univ. of Denmark.

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Appendix: Formal Design Benchmark Example.

Chapter 1

Guided Synthesis Methods.

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A Formalization of Correctness for Linked Representations of Datapath Hardware*

David W. Knapp and Marianne Winslett
Computer Science Department
University of Illinois
1304 W. Springfield Ave.
Urbana, IL 61801

Abstract

In this paper we present a formal representation for register-level digital designs. This is a *separated* representation in that it provides separate but linked representations for behavior, timing, and structure. This representation has the advantage of being at once rich, formal, redundant, and prescriptive. Because it is rich, it covers many aspects of design correctness and completeness. Because it is formal, several well-characterized tests can be applied to a design to determine its well-formedness. Because it is redundant, internal consistency checks can be used to test its internal semantic integrity. And finally, because it is prescriptive, a violated constraint is closely linked to actions can remove or ameliorate the violation. Specifically, it is possible to represent the structure of a design, the behavior desired of that structure, and the relationship between the two; by enforcing internal consistency constraints, we can force the structure to be capable of the behavior, and if the structure is incapable then analysis of the ways in which consistency constraints are violated provides a direct statement of what must be accomplished to make it capable.

We also present a program, RLEXT (Register Level EXploration Tool), that uses this representation. RLEXT accepts as input a description of a register-level datapath, and outputs another description of the design resulting from user commands from the regular expression `(((add | delete) (box | wire | connection))* fixit)*`. When the user invokes `fixit` RLEXT tests the integrity constraints of our representation, and repairs any violations automatically. Because the representation is not consistent unless the structure can express the behavior, the design is correct after the invocation of `fixit`. `Fixit` repairs an incorrect design by means of procedures attached to correctness constraints; the directness of the linkage between diagnosis and correction is a major advantage demonstrated by RLEXT.

1 Motivation

In this paper we present research directed at the problem of formal representation of digital electronic designs at the register level. We have restricted ourselves to designs that have a single common clock. We also assume a datapath/controller style of implementation; that is, a design consists of hardware that manipulates data, plus hardware that delivers control signals to the datapath. We do not consider the problem of nested loops. Subject to the aforementioned restrictions, our goal is to represent digital designs in terms of behavior and structure. We want to represent behavior so that the desired behavior of a target machine can be 'understood' by a program, and we want to represent structure so that a prog am can (a) test the structure against the behavior, (b) analyze and operate upon the structure to complete or transform it, and (c) use the structure as a specification for downstream design tasks.

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