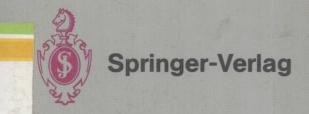
Fault Diagnosis and Fault Tolerance

A Systematic Approach to Special Topics



TP306

Tinghuai Chen



Fault Diagnosis and Fault Tolerance

A Systematic Approach to Special Topics

With 120 Figures and 23 Tables



Springer-Verlag

Berlin Heidelberg New York London Paris Tokyo Hong Kong Barcelona Budapest Prof. Tinghuai Chen

Computer Research Institute Chongqing University Chongqing, PR China 630044

ISBN 3-540-54962-5 Springer-Verlag Berlin Heidelberg New York ISBN 0-387-54962-5 Springer-Verlag New York Berlin Heidelberg

This work is subject to copyright. All rights are reserved, whether the whole or part of the material is concerned, specifically the rights of translation, reprinting, re-use of illustrations, recitation, broadcasting, reproduction on microfilm or in any other way, and storage in data banks. Duplication of this publication or parts thereof is permitted only under the provisions of the German Copyright Law of September 9, 1965, in its current version, and permission for use must always be obtained from Springer-Verlag. Violations are liable for prosecution under the German Copyright Law.

© Springer-Verlag Berlin Heidelberg 1992 Printed in Germany

Typesetting: camera ready by author

45/3140-543210 - Printed on acid-free paper

Preface

With the rapid growth of integration scale of VLSI chips and the present need for reliable computers in space exploration, fault diagnosis and fault tolerance have become more important than before, and hence reveal a lot of interesting topics which attract many researchers to make a great number of contributions to this field. In recent years, many new and significant results have been achieved. A quick scan over the proceedings of the conferences on fault-tolerant computing and design automation as well as on testing will convince the reader of that. But unfortunately these achievements have not been entirely reflected in the textbooks, so that there seems to be a gap for the new researcher who already has the basic knowledge and wants to begin research in this area. As a remedy for this deficiency, this book is intended for beginners, especially graduate students, as a textbook which will lead them to the frontier of some branches of the fault-tolerant computing field.

The first chapter introduces the four-valued logic B_4 and its applications. In 1966 Roth first proposed this four-valued logic as a technique to generate tests for logical circuits, but this work did not concern the mathematical basis of B_4 itself. Here in this book it is considered in an abstract way, related to the representations of boolean functions in B_4 , the computation of the four components of the functions, called the STAR algorithm, which plays the same role as boolean differentials and boolean differences, and also solving equations in B_4 . The applications depend upon the explanations of these four elements: The first explanation can be used to derive the test set for combinational and sequential circuits, which has some advantages over existing techniques. The second explanation leads to hazard identification and then to dynamic test generation, which can detect most of the statically undetectable faults. The third explanation is the transition logic concerning the propositional and predicate calculus, as well as logical inferences, which can more or less reflect the dynamic logical behavior of the objective world.

The fault-diagnosis problem at the system level was formulated by Preparata, Metze and Chien in 1967. Since then a lot of work has been done for different models. This is summarized in Chap. 2 in the extensions along four directions. In particular, this theory is generalized to society diagnosis, i.e., to distinguish the guilty persons from the innocent and the unintentional liars by analysing their mutual testimonies. Some of these models are studied in detail as examples to show the scheme of proofs. Further, a simple analog circuit is taken as an example to illustrate how the system diagnosis theory has been applied to analog networks in recent years, and this will inspire people to apply this theory to the problem of multiple-fault diagnosis in logical circuits as well.

Design for testability is a hot project in the testing field, which can alleviate test generation and hence save computer time. But how to define the testability measure is still a problem. Chapter 3 lists the postulates for an ideal definition of testability measure and gives an evaluation of some existing definitions. It then introduces the synthesis problem for testability, which is more important in the designing phase. The automatic design for testability via testability measures is studied in detail at gate level, and the design at module level is also outlined.

The NMR (N Modular Redundancy) technique is widely used in fault-tolerant design. A new technique, NMRC (NMR with comparing), is introduced in Chap. 4, which contains the other NMR techniques as its special cases. Three optimal designs (Vertex-Edge, Edge-Vertex and Tm optimal) are studied in detail.

In recent years, multiprocessor systems and computer networks have become widely used, in which processors or computers are connected by buses with or without common memories, dedicated communication channels, crossbar networks or switching networks; their reliability problem should be well considered.

Chapter 5 studies the fault tolerance of an interconnection switching network formed by β -elements and other elements. Two special types, i.e., ISE and $C_{1,t}^n$, which provide the dynamic full access property, are taken into account. The number of faulty elements tolerated by the network can be increased by modifying the design without any penalty of additional hardware or time-delay. In addition an RFT network which provides the full access property and tolerates a larger class of fault models is also studied.

For multibus-multiprocessor systems, there seems to be lacking a unified mathematical tool which can be used to study them in depth. In Chap. 6, hypergraphs are used to represent multibus systems, so that the fault tolerance problem of the system corresponds to the connectivity problem of a hypergraph. An important inequality for the connectivities is proved and the best connectivity problem is solved with the aid of Balanced Incomplete Block (BIB) designs of combinatorics. This BIB design is generalized to Weak Balanced Incomplete Block designs (WBIB), which are new in combinatorics. Thus many optimal fault-tolerant system designs are obtained which are better than the previous ones. Based on this theory, a lot of work could be done in the future; this is laid before the reader.

TMR (Triple Modular Redundancy) system are widely used to achieve fault tolerance for single faults. If single faults occur successively in a system, there exists a fault-tolerant center with the fault-tolerant degree which is the maximum number of sequential faults tolerated. Hence the sufficient conditions of the optimal design for sequential faults are introduced.

References are listed, and some long proofs as well as tedious techniques are moved to the appendices after the chapters.

All the chapters are independent, and each chapter is self-contained, so the reader can read the book in any order. But it is necessary to have some basic knowledge of boolean algebra, graph theory, linear integer programming, testing and fault tolerance. Of course the reader should also be acquainted with the ideas of complexity of algorithms and NP-completeness.

This book can be regarded as the summary of the work done during the last ten years in the research group on fault tolerance in Chongqing University, the People's Republic of China. This material had been delivered twice as lectures in Chongqing University as a seminar for graduate students and also in Karlsruhe University, the Federal Republic of Germany, as a 24-hour course. This book was written based on these experiences.

The author is grateful to Prof. W. Görke and Prof. G. Hotz, who read the manuscript carefully and made some important suggestions. Also thanks are given to Dr. M. Marhöfer for his help in handling the manuscript. The author heartily thanks all colleagues in his research group; without their hard work and their original papers this book would have been impossible. Special thanks are given to Mr. Y.N. Chen who wrote the first drafts of Chap. 4 and Chap. 7, Dr. R. Yao, who wrote the final part of Chap. 6 and also Mr. F.J. Li, Mr. L.D. Zhou and Mr. Y.D. Shen for their typing. Special thanks should be given to my wife Prof. Heyue Wang for her typing the most part of this book.

Since fault tolerance is a wide research area, a lot of important contributions could not be included in one short book. Besides, there may be some mistakes or deficiencies in the book which have not been discovered by the author. If the reader would care to point these out, the author would appreciate it very much, and will make corrections in a revised version.

September 1991 Chongqing Tinghuai Chen

9301244

Contents



Chapter 1 Four-Valued Logic and Its Applications	
1.1 Introduction ····································	. 1
1.2 Mathematical Basis	. 2
1.2.1 Four-Valued Boolean Algebra B	
1.2.2 Boolean Expression·····	. :
1.9.3 Manning P ^{II} > P and Polity	
1.2.3 Mapping $B_4^n \to B_4$ and Boolean Functions	. 3
1.2.1 vector rorms	• 4
1.2.5 Canonical Forms.	. 5
1.2.6 Expressions for Boolean Functions	, 5
1.3 STAR Expansions, Boolean Difference and Boolean Differential	, 8
1.3.1 Expansion Formulae ······	. 8
1.3.2 Boolean Difference	11
1.3.3 Boolean Differential · · · · · · · · · · · · · · · · · · ·	13
1.3.4 Geometrical Interpretation	15
1.4 Combined Components	19
1.4.1 Front and Rear Values	19
1.4.2 Binary Coding·····	21
1.4.3 Interpretation for Testing	22
1.5 Boolean Equations	22
1.5.1 Basic Concepts ·····	22
1.5.2 Equations $A_1 \cdot A_2 \cdot \cdots \cdot A_n \cdot j=0$ with $j=1$, D, \overline{D} ; and $A_1 = x_1$ or $\overline{x_1} \cdot \cdots \cdot x_n \cdot j=0$	00
1.5.3 Deriving Star Expansion Via Solving Equation	23
1.6 Test Generation for Combinational Circuits	24
1.6.1 Fault and (Static) Test	27
1.6.2 The Test for Single Fault	27
1.7 Statical Test Generation for Sequential Circuits	31
1.7.1 Example to Derive Tests	39
1.7.2 Comparison with Other Method·····	39
1.8 Identification of Hazards and Dynamic Testing	40
1.8.1 The Dynamic Behavior and	42
Dynamic Tests of Combinational Circuit	
1.8.2 Identification of Hazards	42
1.8.3 Dynamic Tests and Hazardous Tests	46
1.9 Transition Logic	51
1 9 1 Proposition Colonbus and Bull.	56
1.9.1 Proposition Calculus and Predicate Calculus	56
1.9.2 Logical Inferences·····	58
1.9.3 Other Logic·····	59

Chapter 2 Computer System Diagnosis and Society Diagnosis 65 2.1.1 Self-Diagnosis of System 65 2.1.2 Basic Definitions 68 2.2 One Step System Diagnosis for PMC Model 69 2.2.1 The Characterization Problem 69 2.2.2 Diagnosing Algorithm 73 2.3.3 Optimal Design 75 2.3 The Extension of System Diagnosis 76 2.3.1 Extension along Diagnostic Goals 76 2.3.2 Extension along Models 78 2.3.3 Extension along Diagnosing Method 83 2.3.4 Extension along Diagnosing Method 83 2.3.5 The Combination of Different Extensions 84 2.4 The Application of System Diagnosis 85 2.4.1 The Diagnosis for Analog Circuits 85 2.4.2 Fault-Tolerant Computing 89 2.4.3 Society Diagnosis 90 References 93 Chapter 3 Testability Design via Testability Measures 95 3.1.1 The Problem of Testability and Its Measure 96 3.1.2 Definition of Testability and Measures 96 3.1.2 Testability Measure and Algorithm 99 3.1.5 Thoblems Studied in this Chapter 101	1.10 Comparison with Other Logics	60 60 61
Chapter 3 Testability Design via Testability Measures 3.1 Introduction	2.1 Introduction (PMC Model) 2.1.1 Self-Diagnosis of System 2.1.2 Basic Definitions 2.2 One Step System Diagnosis for PMC Model 2.2.1 The Characterization Problem 2.2.2 Diagnosing Algorithm 2.2.3 Optimal Design 2.3 The Extension of System Diagnosis 2.3.1 Extension along Diagnostic Goals 2.3.2 Extension along Models 2.3.3 Extension along Models 2.3.4 Extension along Diagnosing Method 2.3.5 The Combination of Different Extensions 2.4 The Application of System Diagnosis 2.4.1 The Diagnosis for Analog Circuits 2.4.2 Fault-Tolerant Computing 2.4.3 Society Diagnosis	65 68 69 73 75 76 78 81 83 84 85 85 89 90
3.3.1 Definition of Testability 111 3.3.2 Probability Function 111 3.3.3 Controllability Spectrum 114 3.3.4 Observability Spectrum 115	3.1 Introduction 3.1.1 The Problem of Testability and Its Measure. 3.1.2 Definition of Testability and Measures. 3.1.3 Testability in Term of Controllability and Observability. 3.1.4 Testability Measure and Algorithm. 3.1.5 J.Hayes' Suggestion. 3.1.6 Problems Studied in this Chapter. 3.2 Testability Design. 3.2.1 Testability Measure. 3.2.2 Means to Improve Testability. 3.2.3 Constraints A,B,C,D,E and Objective Function F. 3.2.4 ILP Problem for Testability. 3.2.5 Asynchronous Sequential Circuits. 3.2.6 Experimental Results. 3.3 Design for Testability at Module Level. 3.3.1 Definition of Testability. 3.3.2 Probability Function.	95 96 99 99 100 101 102 104 105 107 108 110 111 111 111

3.4 Applications ····· References ·····	
References	•••••116
	117
Chapter 4 NMRC: A Technique for Redundancy	
4.1 Introduction	
1.2 IVING DVSLEM MODEL	
7.2.1 SVSIEM Description	
4.2.2 Fault Pattern.	•••••120
4.2.3 Maximum Likelihood Selection	••••121
4.3 Analysis of Fault Tolerance Capability	••••122
T.J.I Definitions ************************************	
4.3.2 Module-FT Degree	••••123
4.3.3 Module-Comparator FT Degree	••••124
4.4 Optimal NMRC System Design	••••126
4.5 An Example for Comparison Analysis.	••••126
4.5.1 Performance Comparison.	••••129
4.5.2 Cost Comparison ••••••••••••••••••••••••••••••••••••	••••129
4.5.3 Reliability Companion	••••130
4.5.3 Reliability Comparison	••••130
4.5.4 Diagnosability Comparison	••••131
References	••••132
Appendix	••••133
4 A 1 The Proof of Theorem 4.4	••••134
4.A.1 The Proof of Theorem 4.4	••••134
4.A.2 The Proof of Lemma 2	••••134
Chapter 5 Fault Tolerance of Switching Interconnection 2 N	
Chapter 5 Fault Tolerance of Switching Interconnection β-Networks	
5.1 Introduction β-Networks	••••135
5.1.1 Multicomputer Systems	••••135
5.1.2 Connecting Capability and Structure of ICN	••••136
5.1.3 β -elements and β -network.	••••136
5.1.4 Communication Delay	••••137
5.1.5 Fault Model for a β-element	••••138
O.J. J RMISE	• • • • 144
5.4 C ⁿ _{1,t} β-networks····································	
1, t	••••146
5.4.1 Definition of C ⁿ _{1,t} Networks·····	146
5.4.2 Expressions for K and decrease.	
5.4.3 Relative Optimization	••••146
5.4.4 Maximize d	••••147
5.4.4 Maximize d······ 5.4.5 Maximize K·····	••••147
IMARIBLE N	1 47

5.5 RFT Network • • • • • • • • • • • • • • • • • • •
5.5.1 Switching Elements · · · · · · · · · · · · · · · · · · ·
5.5.2 RFT Networks
5.5.3 Routing Algorithm and Fault-Tolerance
5.6 Conclusion
References · · · · · · · · · · · · · · · · · · ·
Chapter 6 The Connectivity of Hypergraph and the Design
of Fault Tolerant Multibus Systems
6.1 Introduction •••••••••••157
6.2 Connectivity of Hypergraph
6.2.1 Definitions • • • • • • • • • • • • • • • • • • •
6.2.2 Basic Theorems ····································
6.2 3 Properties of Hypergraph with the Best Connectivity · · · · · · · · · · · 163
6.3 BIB Design and the Optimized Multibus System ······164
6.3.1 BIB Design ••••••••••••64
6.3.2 Theorems
6.3.3 Optimized Design ••••••••••••••••••••••••••••••••••••
6.4 WBIB and the Optimized Multibus System
6.4.1 Examples of WBIB······168
6.4.2 Definitions of WBIB Design · · · · · · · · · · · · · · · · · · ·
6.4.3 WBIB Design for $\delta=2\cdots$
6.4.4 WBIB Design for δ =3····································
6.4.5 WBIB Design for δ 3
6.5 Generation of WBIB to Other Networks
6.5.1 Reduced to Simple Graph ••••••••••••••••••••••••••••••••
6.5.2 Optimized Sparse Crossbar Network ················176
6.5.3 Optimized Multibus System with Common Memories
6.6 Conclusion • • • • • • • • • • • • • • • • • • •
References · · · · · · · · · · · · · · · · · · ·
Appendix: The Proof of Theorem 6.6
Chapter 7 TMR Design of Distributed System for Sequential Faults
7.1 Introduction ••••••••••••••••••••••••••••••••••••
7.2 DFT Concept
7.3 The Fault Tolerance Degree ••••••••••••••••••••••••••••••••••
7.3.1 The Operations of Graph ······188
7.3.2 The Degree of Fault Tolerance 190
7.3.3 The Center of Fault Tolerance
7.4 The Relationship Between the Architecture
and the Fault Tolerance Degree
7.5 Optimal Design ••••••••••••••••••••••••••••••••••••
7.5 Optimal Design • • • • • • • • • • • • • • • • • • •
7.5.2 T _y (G) Optimal ····································
7.6 Conclusion ••••••••••••••••••••••••••••••••••••
References · · · · · · · · · · · · · · · · · · ·
References

Chapter 1 Four-Valued Logic and Its Applications

Four-valued logic is generalized from the traditional binary logic in order to describe the dynamic logical behavior of objective phenomena. We are going to study its mathematical features, especially the so-called STAR algorithm, the technique for deriving its component expressions, then to show how it can be applied to the static and dynamic test generations for both combinational and sequential circuits as well as to transitional logics.

1.1 Introduction

The traditional binary logic B_2 is well known to every computer scientist. It contains two logic states "1" and "0" which can be used to describe the static state of objective phenomena, for example, the "true" or "false" state of a proposition, "high" or "low" voltage of a wire and "normal" or "faulty" state of a piece of equipment. But "steady" is only so in a relative sense. All objects are absolutely in a moving, changing, or transition state. In order to describe these transitional phenomena the traditional binary logic B_2 should be extended to some new logic.

In 1965 Roth proposed his well known D algorithm to generate tests for a combinational logical circuit, in which each wire is associated with one of the four values, θ ,I,D and \overline{D} ; where θ or I denotes the state that this wire takes a steady logic value "0" or "1" in the common sense; D means this wire takes the logical value "1" when the circuit is normal and value "0" when a

fault occurs in the circuit; conversely \overline{D} means it takes "0" when the circuit is normal and "1" when a fault occurs. Using this system and a table driven technique, Roth successfully derived tests of a circuit but did not take into account the mathematical foundation of the system.

We are going to study this kind of four-valued logic from an abstract point of view and find out some other potential applications of this logic.

Since four-valued logic B_4 is generalized from B_2 , we might seek inspira-

tion by reviewing how complex number theory is generalized from real number

1. **Definition:** A complex number \underline{a} is defined by an ordered pair of real numbers (a_1, a_2) . The addition and dot multiplication are operated in component—wise

$$a + \underline{b} = (a_1 + b_1, a_2 + b_2), \qquad \underline{a} \cdot \underline{b} = (a_1 \cdot b_1, a_2 \cdot b_2).$$

- 2. Vector form Each complex number can be expressed by a vector form: $a = a_1 + a_2 \cdot i$. and this form is useful in computation.
- 3. Components It is important to have a technique to derive the real part $R(a) = a_1$ and the imaginary part $I(\underline{a}) = a_2$ when \underline{a} is a complex function.

Similarly we can define B_4 in terms of B_2 , find the vector form and then propose a technique to derive the expressions of the components, which is called the STAR algorithm. This theory will be introduced in Sects. 1.2-1.5, while the applications will be handled in Sects.1.6-1.10.

1.2 Mathematical Basis

1.2.1 Four-Valued Boolean Algebra B4

Let $B_2 = \langle B_2,$ "•", "+", "-"; 0, 1> be the binary logic B_2 with three logical operations "•", "+" and "-" over two logical elements 0 and 1.

Definition 1.1 The four-valued logic B4 is defined to be the direct

(cartesian) product of B_2 , i.e.

 $B_4 = B_2 \times B_2.$

From discrete mathematics, B_4 is also a boolean algebra, and if $x, y \in B_4$, then x and y can be expressed by ordered pairs

 $x = (x_1, x_2)$ $y = (y_1, y_2),$

where x_1 , x_2 , y_1 and $y_2 \in B_2$ and the logical operations are performed component by component, i.e.

$$x \cdot y = (x_1 \cdot y_1, x_2 \cdot y_2),$$

 $x + y = (x_1 + y_1, x_2 + y_2),$
 $\overline{x} = (\overline{x}_1, \overline{x}_2).$

Since B_2 has only two elements, the four elements of B_4 are simply

$$\theta = (0,0)$$

I = (1,1)

D = (1,0)

$$\overline{D} = (0,1)$$

and the operations are shown in Table 1.1,

Table 1.1

<u>x</u> θ	<u>x</u>	•	θ	I	D	D	+	θ	I	D	$\overline{\mathbf{D}}$
		θ	θ	θ	θ	θ	θ	θ	I	D I	
I		I	θ	I	D	$\overline{\mathrm{D}}$	Ι	I	I	I	Ι
D	D	D	0	D	D	0				D	
$\overline{\mathbf{D}}$	D	$\overline{\mathtt{D}}$	0	$\overline{\mathbf{D}}$	0	$\overline{\mathrm{D}}$	$\overline{\mathbf{D}}$	$\overline{\mathtt{D}}$	I	I	$\overline{\mathbf{D}}$

1.2.2 Boolean Expressions

 $\begin{tabular}{ll} \textbf{Definition} & 1.2 \begin{tabular}{ll} \textbf{Boolean expressions are defined recursively by the following} \\ \end{tabular}$

- 1) Constants '1' and '0' are expressions;
- 2) Variables are expressions;
- The operations '+', '•' and '-' on expressions finite times are expressions;
- 4) only those defined in 1), 2) and 3) are expressions.

Boolean expressions can be used to describe the structures of combinational logical circuits and are denoted by $A(x_1, \cdots, x_n)$, $B(x_1, \cdots, x_n)$ and so on.

Definition 1.3 Two expressions A and B are equivalent, denoted by

 $A(x_1,\cdots,x_n) \doteq B(x_1,\cdots,x_n),$ if one of them can be transformed into the other by using the boolean identities finitely many times.

The following theorem can be found in any book on discrete mathematics.

Theorem 1.1 $A(x_1,\dots,x_n) \doteq B(x_1,\dots,x_n)$ iff $A(x_1,\dots,x_n) = B(x_1,\dots,x_n)$ for $\forall x_1 \in \mathcal{B}$, where \mathcal{B} is any boolean algebra.

Corollary 1.1 $A(x_1,\dots,x_n) = B(x_1,\dots,x_n)$ for $\forall x_1 \in B_4$ iff $A(x_1,\dots,x_n) = B(x_1,\dots,x_n)$ for $\forall x_1 \in B_4$ iff B_2 .

Example 1.1 Absorption Law: If $x + x \cdot y = x$ holds for $\forall x, y \in B_2$, then it also holds for $x, y \in B_4$. Therefore we have identities $D + D \cdot y = D$, and $x + x \cdot D = x$.

1.2.3 Mapping $B_{4}^{n} \rightarrow B_{4}$ and Boolean Functions

Let $F(x_1, \dots, x_n)$ be the mapping $B_4^n \to B_4$. Since there are 4^n points in B_4^n , each of them can be associated with one of the four values in B_4 , and the total

number of mappings is $|\{F(x_1,\dots,x_n)\}| = 4^{4^n}$.

If $f(x_1,\dots,x_n)$ is any boolean expression, when $\forall x_1 \in B_4$, then $f \in B_4$. $f(x_1,\dots,x_n)$ is a special mapping $B_4^n \to B_4$, called the boolean function, which can be used to describe the input-output behavior of a combinational logical

circuit. We know that the number of boolean expressions is 2^{2^n} , and hence

$$|\{f(x_1,\dots,x_n)\}| = 2^{2^n}.$$

Therefore the set of boolean functions is only a subset of the mappings B_{\perp}^{n} В4.

In order to study the property of these mappings and boolean functions, it is adequate to find some better representations for B4.

1.2.4 Vector Form

Definition 1.4

For any $x \in B_4$ there exist four variables x^0 , x^1 , x^* and $\overline{x}^* \in B_2$, that

$$\mathbf{x} = \theta$$
 in $\mathbf{B_4}$ iff $\mathbf{x}^0 = 1$ and $\mathbf{x}^1 = \mathbf{x}^* = \overline{\mathbf{x}}^* = 0$ in $\mathbf{B_2}$,
 $\mathbf{x} = \mathbf{I}$ in $\mathbf{B_4}$ iff $\mathbf{x}^1 = 1$ and $\mathbf{x}^0 = \mathbf{x}^* = \overline{\mathbf{x}}^* = 0$ in $\mathbf{B_2}$,
 $\mathbf{x} = \mathbf{D}$ in $\mathbf{B_4}$ iff $\mathbf{x}^* = 1$ and $\mathbf{x}^0 = \mathbf{x}^1 = \overline{\mathbf{x}}^* = 0$ in $\mathbf{B_2}$,
 $\mathbf{x} = \overline{\mathbf{D}}$ in $\mathbf{B_4}$ iff $\overline{\mathbf{x}}^* = 1$ and $\mathbf{x}^0 = \mathbf{x}^1 = \mathbf{x}^* = 0$ in $\mathbf{B_2}$. (1.1)

(1.1)

then $x \in B_4$ is called a vector and x^0 , x^1 , x^* and $\bar{x}^* \in B_2$ its components. Obviously these components satisfy

Completeness
$$x^0 + x^1 + x^* + \overline{x}^* = 1$$
 and (1.2)

Orthogonality $x^1 \cdot x^j = 0$ for $i \neq j$ and $x^1, x^j \in \{x^0, x^1, x^*, \overline{x}^*\}$. (1.3) Since $B_2 \subset B_4$, the following expression is legal and is equal to x in any

case:
$$x = x^0 \cdot \theta + x^1 \cdot I + x^* \cdot D + \overline{x}^* \cdot \overline{D}$$
. (1.4)

Definition 1.5 Formula (1.4) is called the vector form of x. If the coefficients in (1.4) satisfy completeness and orthogonality, (1.4) is said to be normalized.

For the non-normalized vector form we have the following

Theorem 1.2 If vector form $x = p \cdot \theta + q \cdot I + r \cdot D + s \cdot \overline{D}$ is non-normalized, then the vector form $x = P \cdot \theta + Q \cdot I + R \cdot D + S \cdot \overline{D}$, where

$$P = \overline{q \cdot r \cdot s}, \quad Q = q + r \cdot s, \quad R = \overline{q \cdot r \cdot s}, \quad S = \overline{q \cdot r} \cdot s,$$
 is the corresponding normalized vector form. (1.5)

It is easy to check the completeness and the orthogonality of this coefficient set {P,Q,R,S} and to check the equality of these vector forms.

Example 1.2 Let $x = a \cdot D + b \cdot \overline{D}$. Here p = q = 0, r = a, s = b. Using expression (1.5) to normalize it, we have

$$P = \overline{a} \cdot \overline{b},$$
 $Q = a \cdot b,$ $R = a \cdot \overline{b},$ $S = \overline{a} \cdot b.$

Thus the normalized form is $x = \overline{a \cdot b \cdot \theta} + a \cdot b \cdot I + a \cdot \overline{b \cdot \theta} + \overline{a \cdot b \cdot \overline{D}}$.

1.2.5 Canonical Forms

Let F be a mapping $B_4^n \to B_4$. We are going to find a representation form for F.

A point of the space B_4^n corresponds to an assignment of one of the values θ , I, D, and \overline{D} to the input variable x_1 , $i=1,\cdots,n$, which is equivalent to $x_1^0=1$, $x_1^1=1$, $x_1^*=1$ or $\overline{x_1^*}=1$ respectively and $i=1,\cdots,n$. In other words this space point can be represented by $x_1^{j}\cdots x_1^{j}=1$, where $j_1,\cdots,j_n\in\{0,1,*,-*\}$. This space point is mapped by F to one of the values θ , I, D, and \overline{D} . Thus F can be represented by the following logical sum

$$F = (\sum x_1^{p_1} \cdots x_n^{p_n})\theta + (\sum x_1^{q_1} \cdots x_n^{q_n})I + (\sum x_1^{r_1} \cdots x_n^{r_n})D + (\sum x_1^{s_1} \cdots x_n^{s_n})\overline{D}$$

The first sum containing the common factor θ can be ignored, and the second sum can be divided into two sums on account of $I=D+\overline{D}$. Hence we have

$$F = (\sum_{i=1}^{k_1} \cdots x_n^{k_n})D + (\sum_{i=1}^{k_1} \cdots x_n^{k_n})\overline{D}$$
 (1.6)

where the superscripts k_1 , $l_1 \in \{0, 1, *, *\}$ for $i = 1, \cdots$, n and the first Σ take over all the inputs which cause F = 1 and D, the second Σ over all the inputs which cause F = 1 and \overline{D} .

Definition 1.6 Formula (1.6) is called the canonical sum-of product form of the mapping F, and each term in (1.6) is a minterm.

We can prove that every mapping $B_4^n \to B_4$ is uniquely expressed by its canonical sum-of-product form. Using this canonical form we can also prove that the set of all mappings $B_4^n \to B_4$ forms a boolean algebra B_{4^4} n and hence all the boolean identities are applicable. Besides, the set of all the boolean functions of n variables forms a sub-boolean algebra B_{2^2} n. We leave these proofs to the readers as exercises.

1.2.6 Expressions For Boolean Functions

Suppose $x = x^{0} \cdot \theta + x^{1} \cdot I + x^{*} \cdot D + \overline{x}^{*} \cdot \overline{D}$ and $y = y^{0} \cdot \theta + y^{1} \cdot I + y^{*} \cdot D + \overline{y}^{*} \cdot \overline{D}$

are normalized vector forms which can be transformed into canonical forms

$$x = (x^{1} + x^{*}) \cdot D + (x^{1} + \overline{x}^{*}) \cdot \overline{D}$$

$$y = (y^{1} + y^{*}) \cdot D + (y^{1} + \overline{y}^{*}) \cdot \overline{D}$$

Then the AND of x and y by Table 1.1 is

$$x \cdot y = (x^{1} + x^{*}) \cdot (y^{1} + y^{*}) \cdot D + (x^{1} + \overline{x}^{*}) \cdot (y^{1} + \overline{y}^{*}) \cdot \overline{D}$$

$$= (x^{1}y^{1} + x^{1}y^{*} + x^{*}y^{1} + x^{*}y^{1} + x^{*}y^{*}) \cdot D + (x^{1}y^{*} + x^{1}\overline{y}^{*} + \overline{x}^{*}y^{1} + x^{*}\overline{y}^{*}) \cdot \overline{D}$$

Using the normalization formula (1.5) and after simplification we have the final normalized vector form

$$x \cdot y = (x^{0} + y^{0} + x^{*}\overline{y}^{*} + \overline{x}^{*}y^{*}) \cdot \theta + x^{1}y^{1} \cdot I$$
 (1.7)

+ $(x^{*}y^{1} + x^{1}y^{*} + x^{*}y^{*}) \cdot D + (\overline{x}^{*}y^{1} + x^{1}\overline{y}^{*} + \overline{x}^{*}\overline{y}^{*}) \cdot \overline{D}$

Similarly the OR of x and y is

$$x + y = x^{0}y^{0}\theta + (x^{1} + y^{1} + x^{*}y^{*} + \overline{x}^{*}y^{*}) \cdot I$$

$$+ (x^{*}y^{0} + x^{0}y^{*} + x^{*}y^{*}) \cdot D + (\overline{x}^{*}y^{0} + x^{0}\overline{y}^{*} + \overline{x}^{*}\overline{y}^{*}) \cdot \overline{D}.$$
(1.8)

The NOT of x is $\overline{x} = x^1 \cdot \theta + x^0 \cdot I + \overline{x}^* \cdot D + x^* \cdot \overline{D}$ (1.9)

From the vector forms (1.7), (1.8) and (1.9) we can list out their corresponding component forms as follows.

Theorem 1.3 The components of an AND function are

$$(x*y)^{0} = x^{0} + y^{0} + x^{*}\overline{y}^{*} + \overline{x}^{*}y^{*}$$

$$(x*y)^{1} = x^{1}y^{1}$$

$$(x*y)^{*} = x^{*}y^{1} + x^{1}y^{*} + x^{*}y^{*}$$

$$\overline{(x*y)^{*}} = \overline{x}^{*}y^{1} + x^{1}\overline{y}^{*} + \overline{x}^{*}\overline{y}^{*}$$

$$(1.10)$$

Theorem 1.4 The components of an OR function are $(x + y)^0 = x^0y^0$

$$(x + y)^{1} = x^{1} + y^{1} + x^{*}\overline{y}^{*} + \overline{x}^{*}y^{*} (x + y)^{*} = x^{*}y^{0} + x^{0}y^{*} + x^{*}y^{*} \overline{(x + y)^{*}} = \overline{x}^{*}y^{0} + x^{0}\overline{y}^{*} + \overline{x}^{*}\overline{y}^{*}$$

$$(1.11)$$

Theorem 1.5 The components of a NOT function are

$$(\overline{x})^{0} = x^{1}$$

$$(\overline{x})^{1} = x^{0}$$

$$(\overline{x})^{*} = \overline{x}^{*}$$

$$(\overline{x})^{*} = x^{*}$$

$$(1.12)$$

Since $(\overline{x})^* = \overline{x}^*$, we can take off the parenthesis, and that is why we use the notation " " for the fourth component of a vector. In order to memorize these formulae, we can interpret them as follows. $x \cdot y$, x + y, and \overline{x} are outputs of the AND, OR, NOT gates respectively with inputs x and y. w^0 , w^1 , w^* , and \overline{w}^* can be regarded as the voltage of a wire w such that, say,

w⁰: "low" voltage __ , w¹: "high" voltage __ ,

w*: "step-down transition" \(\). \(\bar{w}*: \) "step-up transition" \(\subseteq \). Thus the third formula of (1.10) can be so interpreted that the output of the AND gate is \(\subseteq \) if and only if one of the inputs x or y is \(\subseteq \), while the other is at high voltage or both of them are \(\supseteq \).

STAR Algorithm The technique for deriving the expressions of the components of a given boolean function is called the STAR algorithm. Usually there are three methods. Since a boolean function is formed by applying the operations "•", "+", "—" finitely many times, its components can be derived by using formulae (1.10), (1.11), (1.12) iteratively according to its structure. (This is the first method for deriving the expressions of the components.)

In (1.10), (1.11), (1.12) the formulae for ()* and $\overline{()}$ * are symmetric, that is, we can obtain one from the other by interchanging all "*"s and " $\overline{\ }$ "s. Theorem 1.6 (Symmetry)

If $F^* = \varphi(0,1,^*,\overline{}^*)$, then $\overline{F}^* = \varphi(0,1,\overline{}^*,^*)$ and vice versa. Example 1.3 For the boolean function $F(x_1,x_2)$ shown in Fig. 1.1 find the formula for F^* and \overline{F}^* .

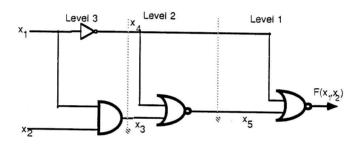


Fig. 1.1 Example

At level 1
$$F^* = (\overline{x_4} + x_5)^* = (\overline{x_4} \cdot \overline{x_5})^* = \overline{x_4}^* \ \overline{x_5}^1 + \overline{x_4}^1 \ \overline{x_5}^* + \overline{x_4}^* \ \overline{x_5}^*.$$
At level 2, $x_5 = \overline{x_3} + x_4$,
$$F^* = \overline{x_4}^* (x_3 + x_4)^1 + \overline{x_4}^1 (x_3 + x_4)^* + \overline{x_4}^* (x_3 + x_4)^*$$

$$= \overline{x_4}^* (x_3^1 + x_4^1 + x_3^* \ \overline{x_4}^* + \overline{x_3}^* \ x_4^*) + x_4^0 (x_3^* \ x_4^0 + x_3^0 \ x_4^* + x_3^* \ x_4^*)$$

$$+ \overline{x_4}^* (x_3^* \ x_4^0 + x_3^0 \ x_4^* + x_3^* \ x_4^*)$$
By orthogonality
$$x_4^1 \ x_4^* = x_4^* \ x_4^* = x_4^0 \ x_4^1 = x_4^0 \ x_4^* = 0,$$

$$F^* = x_3^1 \ x_4^* + x_3^* \ x_4^* + x_3^* \ x_4^* + x_3^* \ x_4^0.$$
At level 3
$$x_4 = \overline{x_1}. \quad x_3 = x_1 x_2,$$

$$F^* = (x_1^1 \ x_2^*) x_1^* + (x_1^* \ x_2^1 + x_1^1 \ x_2^* + x_1^* \ x_2^*) x_1^*$$

$$+ (x_1^* \ x_2^1 + x_1^1 \ x_2^* + x_1^* \ x_2^*) x_1^*$$