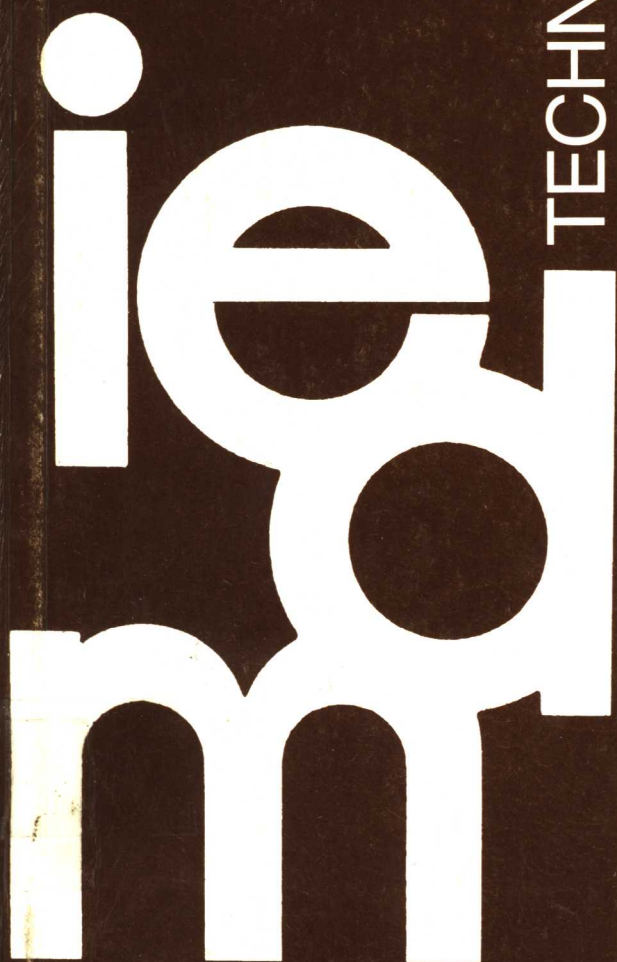


international  
**ELECTRON  
DEVICES**  
meeting

**2002**

SAN FRANCISCO, CA  
DECEMBER 8-11, 2002

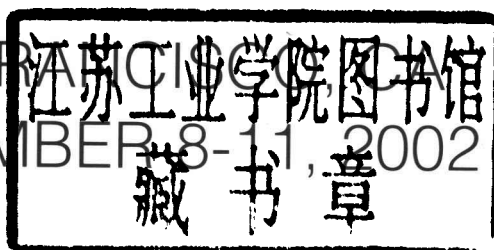
TECHNICAL DIGEST



international  
**ELECTRON  
DEVICES**  
meeting

**2002**

SAN FRANCISCO  
DECEMBER 8-11, 2002



# **2002 International Electron Devices Meeting TECHNICAL DIGEST**

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## WELCOME FROM THE GENERAL CHAIR

On behalf of the IEDM Committee, I would like to welcome you to the 2002 IEEE International Electron Devices Meeting. This year the conference returns to San Francisco and continues a long tradition as the leading forum for the presentation of research and development in the area of electron devices and their applications. The strong international nature of our industry and the broad range of topics are evident, with invited speakers and contributed papers from around the world. A total of 644 abstracts were submitted from 30 different countries, with 534 of these abstracts submitted electronically via the World Wide Web. The total number of accepted abstracts was 219. We continue to focus on accessibility to the information in the IEDM abstracts. Short summaries of each abstract are included on the IEDM home page, and we encourage everyone to visit the site at <http://www.ieee.org/conference/iedm>. This year, we will once again feature the IEDM digital projection of presentation materials at the conference.

Two short courses are scheduled for Sunday. These are designed for broad appeal to IEDM participants with material suitable for both newcomers as well as experts in the field. The courses are entitled "The Future of Semiconductor Manufacturing" and "RF Device Technologies for Communication Systems". These courses have been organized by internationally known researchers and will be presented by people active in the respective topics.

The plenary talks on Monday will feature presentations on "Lithography for Sub-90nm Applications", "Chip Technologies for Entertainment Robots: Present and Future", and "Photonic Bandgap Based Designs for Photonic Integrated Circuits". Speakers from Europe, Asia and North America will be featured.

The IEDM Luncheon speaker this year will be Andrew S. Grove of Intel. He will be speaking on "Changing Vectors of Moore's Law". Dr. Grove is Chairman of the Board of Intel Corp.

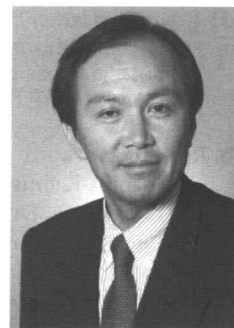
The Emerging Technologies session this year is entitled "Bio-Electronic Devices," and consists of invited talks from experts in the field. The talks will cover electronic sensors for biological pharmaceutical and medical applications.

On Tuesday night, a panel session is planned on two important and potentially controversial topics: "Will SOI Ever Become a Mainstream Technology?" and "Embedded Memories, What Makes Sense, Cents?".

On behalf of the IEEE Electron Devices Society, which sponsors the IEDM, Leda Lunardi, Technical Program Chair and Jeff Welser, Technical Program Vice Chair, I wish to express my sincere appreciation and congratulations to the members of the IEDM committee for the outstanding job they have done in planning and organizing the 2002 meeting. The authors are to be commended for their efforts in preparing and presenting the high-quality papers that form the foundation of the IEDM.

It is with great pleasure that I extend a warm welcome to everyone attending the 2002 IEEE International Electron Devices Meeting.

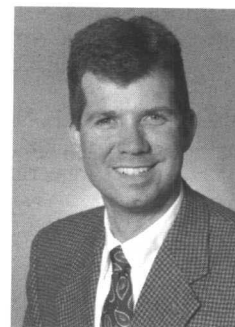
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**Shuji Ikeda**  
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**Jeff Welser**  
Technical Program  
Vice Chair

# AWARD PRESENTATIONS

## PLENARY SESSION

Monday, December 9

2001 Roger A. Haken Best Student Paper Award

To: Hideaki Majima, University of Tokyo  
For the paper entitled: "Impact of Quantum Mechanical Effects on Design of Nanoscale Narrow Channel n- and p-type MOSFETs"

Paul Rappaport Award

To: Ioannis Kymissis, Massachusetts Institute of Technology,  
Christos D. Dimitrakopoulos and Sampath Purushothaman, IBM T.J. Watson Research Center  
For the paper entitled: "High-Performance Bottom Electrode Organic Thin-Film Transistors"

EDS Chapter of the Year Award

To: EDS Taipei Chapter  
"To an EDS chapter based on the quantity and quality of the activities and programs implemented by the chapter."

EDS Graduate Fellowships

To: Yung Fu Chong, National University of Singapore, Jack Chen, University of Illinois, David Fried, Cornell University, Ofir Bochobza-Degani, Technion-Israel Institute of Technology  
"To promote, recognize, and support graduate level study and research within the Electron Devices Society's field of interest"

EDS Distinguished Service Award

To: Lucian A. Kasprzak  
"To recognize and honor outstanding service to the Electron Devices Society"

J.J. Ebers Award

To: Lester F. Eastman, Cornell University  
"For sustained technical contributions and leadership in the development of high frequency heterostructure transistors"

## IEDM LUNCHEON

Tuesday, December 10

2002 Clelio Brunetti Award

To: Mark Lundstrom and Supriyo Datta, Purdue University  
"For significant contributions to the understanding and innovative simulation of nano-scale electronic devices"

2002 IEEE Andrew S. Grove Award

To: Dimitri A. Antoniadis, Massachusetts Institute of Technology  
"For seminal contributions to field-effect devices and silicon process modeling"

2002 IEEE Daniel E. Noble Award

To: Masataka Nakazawa, Tohoku University  
"For pioneering development of 1.48  $\mu\text{m}$  InGaAsP laser-diode pumping of erbium-doped fiber amplifiers (EDFA)"

## LUNCHEON PRESENTATION

"Changing Vectors of Moore's Law," Andrew S. Grove, Intel Corporation

## CONFERENCE HIGHLIGHTS

| <u>Date</u> | <u>Time</u>            | <u>Room</u>                     | <u>Event</u>    |
|-------------|------------------------|---------------------------------|-----------------|
| 12/8        | 9:00 a.m. – 5:30 p.m.  | Continental Ballrooms 1-4 & 6-9 | Short Courses   |
| 12/9        | 9:00 a.m. – 12:00 p.m. | Grand Ballroom B                | Plenary Session |
| 12/9        | 6:00 p.m. – 7:30 p.m.  | Grand Ballroom B                | Reception       |
| 12/10       | 12:20 p.m. – 2:00 p.m. | Grand Ballroom B                | Luncheon        |
| 12/10       | 8:00 p.m. – 10:00 p.m. | Grand Ballroom A & B            | Panel Sessions  |

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Grand Ballroom A

*Co-Chairs:* Malgorzata Jurczak, IMEC  
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- |           |                                                                                                                                                                                                                                                                                             |    |
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4:30 p.m.

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## SESSION 3: Integrated Circuits and Manufacturing — Sub-100nm Logic Technology

Monday, December 9, 1:30 p.m.  
Grand Ballroom B

*Co-Chairs:* S.C. Sun, Chartered Semiconductor  
Witek Maszara, AMD

1:35 p.m.

- |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |    |
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| 3.1 | <b>65nm CMOS Technology (CMOS5) with High Density Embedded Memories for Broadband Microprocessor Applications</b> , N. Yanagiya, S. Matsuda, S. Inaba, M. Takayanagi, I. Mizushima, K. Ohuchi, K. Okano, K. Takahashi, E. Morifuji, M. Kanda, Y. Matsubara, M. Habu, M. Nishigoori, K. Honda, H. Tsuno, K. Yasumoto, T. Yamamoto, K. Hiayama, K. Kokubun, T. Suzuki, J. Yoshikawa, T. Sakurai, T. Ishizuka, Y. Shoda, M. Moriuchi, M. Kishida, H. Matsumori, H. Harakawa, H. Oyamatsu, N. Nagashima*, S. Yamada, T. Noguchi, H. Okamoto* and M. Kakumu, Toshiba Corp, Yokohama, Japan and *Sony Corp, Yokohama, Japan | 57 |
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| 3.2 | <b>A 90 nm Logic Technology Featuring 50 nm Strained Silicon Channel Transistors, 7 Layers of Cu Interconnects, Low k ILD, and 1 <math>\mu\text{m}^2</math> SRAM Cell</b> , S. Thompson, N. Anand, M. Armstrong, C. Auth, B. Arcot, M. Alavi, P. Bai, J. Bielefeld, R. Bigwood, J. Brandenburg, M. Buehler, S. Cea, V. Chikarmane, C. Choi, R. Frankovic, T. Ghani, G. Glass, W. Han, T. Hoffmann, M. Hussein, P. Jacob, A. Jain, C. Jan, S. Joshi, C. Kenyon, J. Klaus, S. Klopchic, J. Luce, Z. Ma, B. McIntyre, K. Mistry, A. Murthy, P. Nguyen, H. Pearson, T. Sandford, R. Schweinfurth, R. Shaheed, S. Sivakumar, M. Taylor, B. Tufts, C. Wallace, P. Wang, C. Weber and M. Bohr, Intel Corp., Hillsboro, OR | 61 |
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| 3.3 | <b>A 90-nm CMOS Device Technology with High-Speed, General-Purpose, and Low-Leakage Transistors for System on Chip Applications</b> , C.C. Wu, Y.K. Leung, C.S. Chang, M.H. Tsai, H.T. Huang, D.W. Lin, Y.M. Sheu, C.H. Hsieh, W.J. Liang, L.K. Han, W.M. Chen, S.Z. Chang, S.Y. Wu, S.S. Lin, H.C. Lin, C.H. Wang, P.W. Wang, T.L. Lee, C.Y. Fu, C.W. Chang, S.C. Chen, S.M. Jang, S.L. Shue, H.T. Lin, Y.C. See, Y.J. Mii, C.H. Diaz, B.J. Lin, M.S. Liang and Y.C. Sun, TSMC, Taiwan, ROC | 65 |
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| 3.4 | <b>50nm Gate Length Logic Technology with 9-Layer Cu Interconnects for 90nm Node SoC Applications</b> , Y.W. Kim, C.B. Oh, Y.G. Ko, K.T. Lee, J.H. Ahn, T.S. Park, H.S. Kang, D.H. Lee, M.K. Jung, H.J. Yu, K.S. Jung, S.H. Liu, B.J. Oh, K.S. Kim, N.I. Lee, M.H. Park, G.J. Bae, S.G. Lee, W.S. Song, Y.G. Wee, C.H. Jeon and K.P. Suh, Samsung Electronics, Kyonggi-Do, Korea | 69 |
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- 3.5 **A 90 nm Communication Technology Featuring SiGe HBT Transistors, RF CMOS, Precision R-L-C RF Elements and 1  $\mu\text{m}^2$  6-T SRAM Cell**, K. Kuhn, M. Agostinelli, S. Ahmed, S. Chambers, S. Cea, S. Christensen, P. Fischer, J. Gong, C. Kardas, T. Letson, L. Henning, A. Murthy, H. Muthali, B. Obradovic, P. Packan, S.W. Pae, I. Post, S. Putna, K. Raol, A. Roskowski, R. Soman, T. Thomas, P. Vandervoorn, M. Weiss and I. Young, Intel Corporation, Hillsboro, OR 73

3:40 p.m.

- 3.6 **High Performance Copper and Low-k Interconnect Technology Fully Compatible to 90nm-node SOC Application (CMOS4)**, M. Inohara, I. Tamura, T. Yamaguchi, H. Koike, Y. Enomoto\*, S. Arakawa, T. Watanabe, E. Ide, S. Kadomura\* and K. Sunouchi, Toshiba Corporation, Kanagawa, Japan and \*Sony Corporation, Atsugi, Japan 77

## SESSION 4: Quantum Electronics and Compound Semiconductors — High Speed, Quantum, and Opto-Electronics

Monday, December 9, 1:30 p.m.

Continental Ballrooms 1-3

Co-Chairs: Barbara Landini, Kopin Corporation  
Michael Schlechtweg, Fraunhofer Institute IAF

1:35 p.m.

- 4.1 **High Speed InP-based HBTs and OEICs (Invited)**, H. Jäckel, U. Hammer, J. Ruiz, I. Schnyder, V. Schwarz, M. Gaspar\*, D. Huber\*, M. Rohner\*\* and A. Huber\*\*\*, Swiss Federal Institute of Technology, Zurich, Switzerland, \*Optospeed SA, Rüschlikon, Switzerland, \*\*Leica Geosystems, Heerbrugg, Switzerland and \*\*\*Zentrum für Mikroelektronik, Windisch, Switzerland 83

2:00 p.m.

- 4.2 **Single Photons and Entangled Photons from a Quantum Dot (Invited)**, J. Vuckovic, C. Santori, D. Fattal, M. Pelton, G. Solomon, B. Zhang, J. Plant and Y. Yamamoto, Stanford University, Stanford, CA 87

2:25 p.m.

- 4.3 **High Efficient 820 nm MOS Ge Quantum Dot Photodetectors for Short-Reach Integrated Optical Receivers with 1300 and 1550 nm Sensitivity**, B.-C. Hsu, S.T. Chang, C.-R. Shie, C.-C. Lai, P.S. Chen\* and C.W. Liu, National Taiwan University, Taiwan, R.O.C and \*ERSO/ITRI, Taiwan, R.O.C. 91

2:50 p.m.

- 4.4 **Experimental Demonstration of a QCA Shift Register and Analysis of Errors**, R. Kummamuru, A. Orlov, R. Ramasubramaniam, C. Lent, G. Bernstein and G. Snider, University of Notre Dame, Notre Dame, IN 95

3:15 p.m.

- 4.5 **Novel Light Emitting Device with Ultrafast Color Switching**, R. Koudelka, J. Woodall and E. Harmon\*, Yale University, New Haven, CT and \*LightSpin Technologies, Inc., Bethesda, MD 99

3:40 p.m.

- 4.6 **Degradation Mechanisms of GaN-Based LEDs After Accelerated DC Current Aging**, G. Meneghesso, S. Levada, R. Pierobon, F. Rampazzo, E. Zanoni, A. Cavallini\*, A. Castaldini\*, G. Scamarcio\*\*, S. Du\*\*\* and I. Eliashevich\*\*\*, University of Padova, Padova, Italy, \*University of Bologna, Bologna, Italy, \*\*University of Bari, Bari, Italy and \*\*\*GELcore LLC, Valley View, OH 103

## SESSION 5: Modeling and Simulation — Compact Modeling

Monday, December 9, 1:30 p.m.

Continental Ballroom 4

Co-Chairs: Ronald van Langevelde, Philips Research Labs  
Rafael Rios, Intel Corporation

1:35 p.m.

- 5.1 **HiSIM: A MOSFET Model for Circuit Simulation Connecting Circuit Performance with Technology (Invited)**, M. Miura-Mattausch, H. Ueno, M. Tanaka, H. J. Mattausch, S. Kumashiro\*, T. Yamaguchi\*, K. Yamashita\* and N. Nakayama\*, Hiroshima University, Higashi-Hiroshima, Japan and \*Semiconductor Technology Academic Research Center, Kanagawa, Japan 109

2:00 p.m.

- 5.2 **A Three-Transistor Threshold Voltage Model for Halo Processes**, R. Rios, W.-K. Shih, A. Shah, S. Mudanai, P. Packan, T. Sandford and K. Mistry, Intel Corp., Hillsboro, OR 113

2:25 p.m.

- 5.3 **Accurate Modeling of Trench Isolation Induced Mechanical Stress Effects on MOSFET Electrical Performance**, R.A. Bianchi, G. Bouche and O. Roux-dit-Buisson, STMicroelectronics, Crolles, France 117

2:50 p.m.

- 5.4 **The Effective Drive Current in CMOS Inverters**, M.H. Na, E. Nowak, W. Haensch\* and J. Cai\*, IBM Corporation, Essex Junction, VT and \*IBM T.J. Watson Research Center, Yorktown Heights, NY 121

3:15 p.m.

- 5.5 **Scattering Matrix Based Compact MOSFET Model**, H. Wang and G. Gildenblat, The Pennsylvania State University, University Park, PA 125

3:40 p.m.

- 5.6 **Compact Modeling of Drain and Gate Current Noise for RF CMOS**, A. Scholten, L. Tiemeijer, R. van Langevelde, R. Havens, V. Venezia\*, A. Zegers-van Duijnhoven, B. Neinhüs\*, C. Jungemann\* and D. Klaassen, Philips Research Labs, Eindhoven, Netherlands and \*University of Bremen, Bremen, Germany 129

4:05 p.m.

- 5.7 **Compact Modelling of Cyclostationary Noise in Semiconductor Devices: A Critical Discussion**, F. Bonani, S. Donati Guerrieri and G. Ghione, Politecnico di Torino, Torino, Italy 133

4:30 p.m.

- 5.8 **A New, Closed-Form Compact Model for the Cyclostationary Noise and LS Conversion Behaviour of RF Junction Diodes**, F. Bonani, S. Donati Guerrieri and G. Ghione, Politecnico di Torino, Torino, Italy 137

## SESSION 6: CMOS and Interconnect Reliability — Dielectric Degradation and Breakdown

Monday, December 9, 1:30 p.m.

Continental Ballroom 5

Co-Chairs: Robin Degraeve, IMEC  
Kenji Okada, Matsushita Electric Industrial Co.

1:35 p.m.

- 6.1 **Correlated Defect Generation in Thin Oxides and Its Impact on Flash Reliability**, D. Ielmini, A. Spinelli\*, A. Lacaita and M. van Duuren\*\*, Politecnico di Milano, Milano, Italy and \*Università degli Studi dell'Insubria, Como, Italy and \*\*Philips Research Leuven, Leuven, Belgium 143

- 2:00 p.m.
- 6.2 Statistics of Successive Breakdown Events for Ultra-thin Gate Oxides**, J. Suñé and E. Wu\*, Universitat Autònoma de Barcelona, Bellaterra, Spain and \*IBM Microelectronics Division, Essex Junction, VT **147**
- 2:25 p.m.
- 6.3 Statistically Independent Soft Breakdowns Redefine Oxide Reliability Specifications**, M. Alam, R. Smith, B. Weir and P. Silverman, Agere Systems, Murray Hill, NJ **151**
- 2:50 p.m.
- 6.4 A New Model of Time Evolution of Gate Leakage Current after Soft Breakdown in Ultra-Thin Gate Oxides**, T. Hosoi, P.L. Ré, Y. Kamakura and K. Taniguchi, Osaka University, Osaka, Japan **155**
- 3:15 p.m.
- 6.5 Spectroscopic Analysis of Trap Assisted Tunneling in Thin Oxides by Means of Substrate Hot Electron Injection Experiments**, F. Driussi, R. Iob, D. Esseni, L. Selmi, R. van Schaijk\* and F. Widdershoven\*, DIEGM, Udine, Italy and \*Philips Research Leuven, Leuven, Belgium **159**
- 3:40 p.m.
- 6.6 Dielectric Breakdown Induced Epitaxy in Ultrathin Gate Oxide – A Reliability Concern**, K. Pey, C.H. Tung\*, M. Radhakrishnan\*\*, L.J. Tang\* and W.H. Lin\*\*\*, Nanyang Technological University, Singapore and \*Institute of Microelectronics, Singapore, \*\*Philips Electronics, Singapore and \*\*\*Chartered Semiconductor Manufacturing Ltd., Singapore **163**
- 4:05 p.m.
- 6.7 Drain-Accelerated Degradation of Tunnel Oxides in Flash Memories**, A. Chimenton, A. Spinelli\*, D. Ielmini\*\*, A. Lacaita\*\*, A. Visconti\*\*\* and P. Olivo, Università degli Studi de Ferrara, Ferrara, Italy, \*Università degli Studi dell'Insubria, Como, Italy, \*\*Politecnico di Milano, Milano, Italy and \*\*\*STMicroelectronics, Agrate Brianza, Italy **167**
- 4:30 p.m.
- 6.8 Observation of Hot-Carrier-Induced nFET Gate-Oxide Breakdown in Dynamically Stressed CMOS Circuits**, B. Kaczer, F. Crupi\*, R. Degraeve, P. Roussel, C. Ciofi\* and G. Groeseneken, IMEC, Leuven, Belgium and \*Università degli Studi di Messina, Messina, Italy **171**

## SESSION 7: Solid State Devices — Nanoelectronics and Novel Memories

Monday, December 9, 1:30 p.m.  
Continental Ballroom 6

Co-Chairs: Sandip Tiwari, Cornell University  
Junji Koga, Toshiba Corporation

- 1:35 p.m.
- 7.1 Single-Electron Random-Number Generator (RNG) for Highly Secure Ubiquitous Computing Applications**, K. Uchida, T. Tanamoto, R. Ohba, S. Yasuda and S. Fujita, Toshiba Corporation, Yokohama, Japan **177**
- 2:00 p.m.
- 7.2 Effects of Ultra-Narrow Channel on Characteristics of MOSFET Memory with Silicon Nanocrystals Floating Gates**, M. Saitoh, E. Nagata and T. Hiramoto, University of Tokyo, Tokyo, Japan **181**
- 2:25 p.m.
- 7.3 Quantum-Well Memory Device (QWMD) with Extremely Good Charge Retention**, Z. Krivokapic, T. Krishnamohan\*, A. Halliyal, A. Jafarpour, S. Cherian, A. Holbrook, W. Zheng, M. Randolph and M.-R. Lin, AMD, Sunnyvale, CA and \*Stanford University, Stanford, CA **185**

- 2:50 p.m.
- 7.4 Silicon-Rich-Oxides as an Alternative Charge-Trapping Medium in Fowler-Nordheim and Hot Carrier Type Non-Volatile-Memory Cells**, M. Rosmeulen\*, E. Slesckx and K. De Meyer\*, IMEC, Leuven, Belgium and \*IMEC and KU Leuven, Leuven, Belgium **189**

- 3:15 p.m.
- 7.5 Novell Colossal Magnetoresistive Thin Film Nonvolatile Resistance Random Access Memory (RRAM)**, W. W. Zhuang, W. Pan, B.D. Ulrich, J.J. Lee, L. Stecker, A. Burmaster, D.R. Evans, S.T. Hsu, M. Tajiri\*, A. Shimaoka\*, K. Inoue\*, T. Naka\*, N. Awaya\*, K. Sakiyama\*, Y. Wang\*\*, S.Q. Liu\*\*, N.J. Wu\*\*, and A. Ignatiev\*\*, Sharp Laboratories of America, Camas, WA and \*Sharp Corporation, Nara, Japan and \*\*University of Houston, Houston, TX **193**

## SESSION 8: Detectors, Sensors and Displays — Recent Advances in Inertial and Biological MEMs

Monday, December 9, 1:30 p.m.  
Continental Ballrooms 7-9

Co-Chairs: Jack Judy, UCLA  
Benedetto Vigna, STMicroelectronics

- 1:35 p.m.
- 8.1 Recent Progress in Modularly Integrated MEMS Technologies (Invited)**, T.-J. King, R. Howe, S. Sedky\*, G. Liu, B. Lin, M. Wasilik and C. Duenn\*\*, University of California, Berkeley, CA, \*The American University in Cairo, Cairo, Egypt and \*\*Robert Bosch Corporation, Palo Alto, CA **199**
- 2:00 p.m.
- 8.2 Integrated Surface-Micromachined Z-axis Frame Microgyroscope**, M. Palaniapan, R. Howe and J. Yasaitis\*, University of California, Berkeley, CA and \*Analog Devices, Inc., Cambridge, MA **203**
- 2:25 p.m.
- 8.3 A Self-Assembly Conductive Device for Direct DNA Identification in Integrated Microarray Based System**, M. Xue, J. Li\*, W. Xu, Z. Lu\*, K.L. Wang, P.K. Ko and M. Chan, Hong Kong University of Science and Technology, Hong Kong and \*Southeast University, Nanjing, China PR **207**
- 2:50 p.m.
- 8.4 A DNA Prism: The Physical Principles for Optimizing a Microfabricated DNA Separation Device**, L.R. Huang, J. Tegenfeldt, J. Sturm, R. Austin and E.C. Cox, Princeton University, Princeton, NJ **211**
- 3:15 p.m.
- 8.5 Amorphous Silicon Pixel Amplifier with  $\Delta V_T$  Compensation for Low Noise Digital Fluoroscopy**, K.S. Karim, A. Nathan and J. Rowlands\*, University of Waterloo, Ont., Canada and \*University of Toronto, Ont., Canada **215**

## SESSION 9: Process Technology — Memories and Passive Components

Monday, December 9, 1:30 p.m.  
Imperial Room

Co-Chairs: U-In Chung, Samsung Electronics Co. Ltd.  
Pierre Bouillon, STMicroelectronics

- 1:35 p.m.
- 9.1 Mass Production Worthy  $\text{HfO}_2\text{-Al}_2\text{O}_3$  Laminate Capacitor Technology using Hf Liquid Precursor for Sub-100nm DRAMs**, J.-H. Lee, J.P. Kim, J.-H. Lee, Y.-S. Kim, H.-S. Jung, N.-I. Lee, H.-K. Kang, K.-P. Suh, M.-M. Jeong, K.-T. Hyun, H.-S. Baik, Y.-S. Chung, X. Liu\*, S. Ramanathan\*, T. Seidel\*, J. Winkler\*, A. Londergan\*, H.Y. Kim\*, J.M. Ha\* and N.K. Lee\*, Samsung Electronics Co., Ltd., Kyunggi-Do, Korea and \*Genus, Inc., Sunnyvale, CA **221**

- 2:00 p.m.
- 9.2 Niobia-Stabilized Tantalum Pentoxide (NST) - Novel High-k Dielectrics for Low-Temperature Process of MIM Capacitors**, Y. Matsui, M. Hiratani, I. Asano\* and S. Kimura, Hitachi, Ltd., Tokyo, Japan and \*Elpida Memory, Inc., Kanagawa, Japan **225**
- 2:25 p.m.
- 9.3 Mass-Productive Ultra-Low Temperature ALD SiO<sub>2</sub> Process Promising for Sub-90nm Memory and Logic Devices**, J.-E. Park, J.-H. Ku, J.-W. Lee, J.-H. Yang, K.-S. Chu, S.-H. Lee, M.-H. Park, N.-I. Lee, H.-K. Kang, K.-P. Suh, B.-H. Cho\*, B.-C. Kim\* and C.-H. Shin\*, Samsung Electronics Co., Ltd., Kyunggi-Do, Korea, \*Moohan, Inc., Chungchongnam-Do, Korea **229**
- 2:50 p.m.
- 9.4 Novel Shallow Trench Isolation Process Using Flowable Oxide CVD for Sub-100nm DRAM**, S.-W. Chung, S.-T. Ahn, H.-C. Sohn, J. Ku, S. Park, Y.-W. Song, H.-S. Park and S.-D. Lee, Hynix Semiconductor Inc., Kyounggi-do, Korea **233**
- 3:15 p.m.
- 9.5 Highly Reliable MONOS Devices with Optimized Silicon Nitride Film Having Deuterium Terminated Charge Traps**, M. Tanaka, S. Saida, Y. Mitani, I. Mizushima and Y. Tsunashima, Toshiba Corporation, Kanagawa, Japan **237**
- 3:40 p.m.
- 9.6 Characterization and Comparison of Two Metal-Insulator-Metal Capacitor Schemes in 0.13  $\mu$ m Copper Dual Damascene Metallization Process for Mixed-Mode and RF Applications**, C.H. Ng, K.W. Chew, J.X. Li, T.T. Tjoa, L.N. Goh and S.-F. Chu, Chartered Semiconductor Manufacturing Ltd., Singapore **241**
- SESSION 10: CMOS Devices — Advanced Ultrathin-Body Devices**
- Tuesday, December 10, 9:00 a.m.  
*Grand Ballroom A*
- Co-Chairs:* Jack Hergenrother, Agere Systems  
Yasuo Yamaguchi, Mitsubishi Electric Corp.
- 9:05 a.m.
- 10.1 Metal-Gate FinFET and Fully-Depleted SOI Devices Using Total Gate Silicidation**, J. Kedzierski, E. Nowak\*, T. Kanarsky\*\*, Y. Zhang, D. Boyd\*\*, R. Carruthers, C. Cabral, R. Amos, C. Lavoie, R. Roy, J. Newbury, E. Sullivan, J. Benedict, P. Saunders, K. Wong\*\*, D. Canaperi, M. Krishnan, K.-L. Lee, B.A. Rainey\*, D. Fried\*, P. Cottrell\*, H.-S.P. Wong, M. leong\*\* and W. Haensch, IBM SRDC, Yorktown Heights, NY, \*IBM Microelectronics, Essex Junction, VT and \*\* IBM Microelectronics, Hopewell Junction, NY **247**
- 9:30 a.m.
- 10.2 FinFET Scaling to 10nm Gate Length**, B. Yu, L. Chang\*, S. Ahmed, H. Wang, S. Bell, C.-Y. Yang, C. Tabery, C. Ho, Q. Xiang, T.-J. King\*, J. Bokor\*, C. Hu\*, M.-R. Lin and D. Kyser, AMD, Inc., Sunnyvale, CA and \*University of California, Berkeley, CA **251**
- 9:55 a.m.
- 10.3 25nm CMOS Omega FETs**, F.-L. Yang, H.-Y. Chen, F.-C. Chen, C.-C. Huang, C.-Y. Chang, H.-K. Chiu, C.-C. Lee, C.-C. Chen, H.-T. Huang, C.-J. Chen, H.-J. Tao, Y.-C. Yeo, M.-S. Liang and C. Hu, Taiwan Semiconductor Manufacturing Company, Ltd., Taiwan, ROC **255**
- 10:20 a.m.
- 10.4 FinFET Process Refinements for Improved Mobility and Gate Work Function Engineering**, Y.-K. Choi, L. Chang, P. Ranade, J.-S. Lee, D. Ha, S. Balasubramanian, A. Agarwal\*, M. Ameen\*, T.-J. King and J. Bokor, University of California, Berkeley, CA and \*Axcelis Technologies, Beverly, MA **259**
- 10:45 a.m.
- 10.5 SON (Silicon-On-Nothing) P-MOSFETs with Totally Silicided (CoSi<sub>2</sub>) Polysilicon on 5nm-Thick Si-Films: The Simplest Way to Integration of Metal Gates on Thin FD Channels**, S. Monfray\*, T. Skotnicki, B. Tavel\*, Y. Morand, S. Descombes, A. Talbot, D. Dutartre, C. Jenny, P. Mazoyer, R. Palla, F. Leverd, Y. Le Friec, R. Pantel, M. Haond, C. Charbuillet, C. Vizioz\*\*, D. Louis\*\* and N. Buffet\*\*, STMicroelectronics, Crolles, France and \*STMicroelectronics, Crolles, France and France Telecom, Meylan, France and \*\*CEA LETI, Grenoble, France **263**
- 11:10 a.m.
- 10.6 Extreme Scaling With Ultra-Thin Silicon Channel MOSFET's (XFET)**, B. Doris, M. leong, T. Kanarsky, Y. Zhang\*, R.A. Roy\*, O. Dokumaci, Z. Ren, F.-F. Jamin, L. Shi\*, W. Natzle, H.-J. Huang, J. Mezzapelle, A. Mocuta, S. Womack, M. Gribelyuk, E.C. Jones\*, R.J. Miller\*, H.-S.P. Wong\* and W. Haensch\*, IBM Microelectronics, Hopewell Junction, NY and \*IBM T.J. Watson Research Center, Yorktown Heights, NY **267**
- 11:35 a.m.
- 10.7 Nickel Silicide Metal Gate FDSOI Devices with Improved Gate Oxide Leakage**, Z. Krivokapic, W. Maszara, K. Achutan, P. King, J. Gray, E. Zhao, J. Zhang, J. Chan, A. Marathe and M.-R. Lin, AMD, Sunnyvale, CA **271**
- 12:00 p.m.
- 10.8 Fully Depleted Surrounding Gate Transistor (SGT) for 70nm DRAM and Beyond**, B. Goebel, J. Lützen, D. Manger, P. Moll, K. Mümmeler, M. Popp, U. Scheler, T. Schlösser, H. Seidl, M. Sesterhenn, S. Slesazek and S. Tegen, Infineon Technologies, Dresden, Germany **275**
- SESSION 11: Solid State Devices — Novel Devices**
- Tuesday, December 10, 9:00 a.m.  
*Continental Ballrooms 1-3*
- Co-Chairs:* Thomas Skotnicki, STMicroelectronics  
Andrea Lacaita, Politecnico di Milano
- 9:05 a.m.
- 11.1 Carbon Nanotube Electronics (Invited)**, P. Avouris, J. Appenzeller, V. Derycke, R. Martel and S. Wind, IBM T.J. Watson Research Center, Yorktown Heights, NY **281**
- 9:30 a.m.
- 11.2 Short-Channel Like Effects in Schottky Barrier Carbon Nanotube Field-Effect Transistors**, J. Appenzeller, J. Knoch\*, R. Martel, V. Derycke, S. Wind and P. Avouris, IBM T.J. Watson Research Center, Yorktown Heights, NY and \*Massachusetts Institute of Technology, Cambridge, MA **285**
- 9:55 a.m.
- 11.3 I-MOS: A Novel Semiconductor Device with a Subthreshold Slope Lower than  $kT/q$** , K. Gopalakrishnan, P.B. Griffin and J. Plummer, Stanford University, Stanford, CA **289**
- 10:20 a.m.
- 11.4 Polymeric Integrated Circuits: Fabrication and First Characterisation (Invited)**, D.M. de Leeuw, G. Gelinck, T. Geuns, E. van Veenendaal, E. Cantatore and B. Huisman, Philips Research Laboratories, Eindhoven, The Netherlands **293**