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Preface

We are proud to introduce the proceedings of the 7th International Conference on Evolvable Systems: From Biology to Hardware (ICES 2007) held in Wuhan, China, September 21–23, 2007. ICES 2007 successfully attracted 123 submissions. After rigorous reviews, 41 high-quality papers were included in the proceedings of ICES 2007, representing an acceptance rate of 33%.

ICES conferences are the first series of international conferences on evolvable systems. The idea of evolvable systems, whose origins can be traced back to the cybernetics movement of the 1940s and the 1950s, has recently led to bio-inspired systems with self-reproduction or self-repair of the original hardware structures, and evolvable hardware with the autonomous reconfiguration of hardware structures by evolutionary algorithms.

Following the workshop Towards Evolvable Hardware taking place in Lausanne, Switzerland, in October 1995, the 1st International Conference on Evolvable Systems: From Biology to Hardware (ICES 1996) was held in Tsukuba, Japan (1996). Subsequent ICES conferences were held in Lausanne, Switzerland (1998), Edinburgh, UK (2000), Tokyo, Japan (2001), Trondheim, Norway (2003), and Barcelona, Spain (2005) where it was decided that China University of Geosciences, Wuhan, would be the location of ICES 2007 with Lishan Kang as the General Chair.

ICES 2007 addressed the theme "From Laboratory to Real World" by explaining how to shorten the gap between evolvable hardware research and design for real-world applications in semiconductor engineering and mechanical engineering. ICES 2007 featured the most up-to-date research and applications in digital hardware evolution, analog hardware evolution, bio-inspired systems, mechanical hardware evolution, evolutionary algorithms in hardware design, and hardware implementations of evolutionary algorithms. ICES 2007 also provided a venue to foster technical exchanges, renew everlasting friendships, establish new connections, and presented the Chinese cultural traditions to overcome cultural barriers.

On behalf of the Organizing Committee, we would like to thank warmly the sponsors, China University of Geosciences and Chinese Society of Astronautics, who helped in one way or another to achieve our goals for the conference. We wish to express our appreciation to Springer, for publishing the proceedings of ICES 2007 in the *Lecture Notes in Computer Science*. We would also like to thank also the authors for submitting their work, as well as the Program Committee members and reviewers for their enthusiasm, time and expertise.

The invaluable help of active members of the Organizing Committee, including Xuesong Yan, Qiuming Zhang, Yan Guo, Siqing Xue, Ziyi Chen, Xiang Li, Guang Chen, Rui Wang, Hui Wang, and Hui Shi, in setting up and maintaining the online submission systems, assigning the papers to the reviewers, and

preparing the camera-ready version of the proceedings was highly appreciated and we would like to thank them personally for their efforts to make ICES 2007 a success.

September 2007

Lishan Kang
Yong Liu
Sanyou Zeng

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ICES 2007 was organized by the School of Computer Science and Research Center for Space Science and Technology, China University of Geosciences, sponsored by China University of Geosciences and Chinese Society of Astronautics.

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An Online EHW Pattern Recognition System Applied to Sonar Spectrum Classification

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Abstract. An evolvable hardware (EHW) system for high-speed sonar return classification has been proposed. The system demonstrates an average accuracy of 91.4% on a sonar spectrum data set. This is better than a feed-forward neural network and previously proposed EHW architectures. Furthermore, this system is designed for online evolution. Incremental evolution, data buses and high level modules have been utilized in order to make the evolution of the 480 bit-input classifier feasible. The classification has been implemented for a Xilinx XC2VP30 FPGA with a resource utilization of 81% and a classification time of 0.5μs.

1 Introduction

High-speed pattern recognition systems applied in time-varying environments, and thus needing adaptability, could benefit from an online evolvable hardware (EHW) approach [1]. One EHW approach to online reconfigurability is the Virtual Reconfigurable Circuit (VRC) method proposed by Sekanina in [2]. This method does not change the bitstream to the FPGA itself, rather it changes the register values of a circuit already implemented on the FPGA, and obtains virtual reconfigurability. This approach has a speed advantage over reconfiguring the FPGA itself, and it is also more feasible because of proprietary formats preventing direct FPGA bitstream manipulation. However, the method requires much logic resources.

An EHW pattern recognition system, Logic Design using Evolved Truth Tables (LoDETT), has been presented by Yasunaga et al. Applications include face image and sonar target recognition [3,4]. This architecture is capable of classifying large input vectors (512 bits) into several categories. The classifier function is directly coded in large AND gates. The category module with the highest number of activated AND gates determines the classification. Incremental evolution is utilized such that each category is evolved separately. The average recognition accuracy for this system, applied to the sonar target task, is 83.0%. However, evolution is performed *offline* and the final system is synthesized. This approach

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gives rapid (< 150ns) classification in a compact circuit, but lacks run-time reconfigurability.

A system proposed earlier by the authors addresses the reconfigurability by employing a VRC-like array of high-level functions [5]. Online/on-chip evolution is attained, and therefore the system seems suited to applications with changes in the training set. However, the system is limited to recognizing one category out of ten possible input categories.

A new architecture was then proposed by the authors to allow for the high classification capabilities of the LoDETT system, while maintaining the online evolution features from [5]. This was applied to multiple-category face image recognition and a slightly higher recognition accuracy than the LoDETT system was achieved [6]. While in LoDETT a large number of inputs to the AND gates can be optimized away during circuit synthesis, the run-time reconfiguration aspect of the online architecture has led to a different approach employing fewer elements. The evolution part of this system has been implemented on an FPGA in [7]. Fitness evaluation is carried out in hardware, while the evolutionary algorithm runs on an on-chip processor.

In this paper the architecture, previously applied to face image recognition, has been applied to the sonar target recognition task. The nature of this application has led to differences in the architecture parameters. Changes in the fitness function were necessary to deal with the higher difficulty of this problem.

The sonar target dataset was presented by Gorman and Sejnowski in [8]. A feed-forward neural network was presented, which contained 12 hidden units and was trained using the back-propagation algorithm. A classification accuracy of 90.4% was reported. Later, better results have been achieved on the same data set, using variants of the Support Vector Machine (SVM) method. An accuracy of 95.2% was obtained in a software implementation presented in [9]. There also exists some hardware implementations of SVMs, such as [10], which performs biometric classification in 0.66ms using an FPGA.

The next section introduces the architecture of the evolvable hardware system. Then, the sonar return-specific implementation is detailed in section 3. Aspects of evolution are discussed in section 4. Results from the experiments are given and discussed in sections 5. Finally, section 6 concludes the paper.

2 The Online EHW Architecture

The EHW architecture is implemented as a circuit whose behaviour and connections can be controlled through configuration registers. By writing the genome bitstream from the genetic algorithm (GA) to these registers, one obtains the phenotype circuit which can then be evaluated. This approach is related to the VRC technique, as well as to the architectures in our previous works [11,5].

2.1 System Overview

A high-level view of the system can be seen in figure 1. The system consists of three main parts – the classification module, the evaluation module, and the