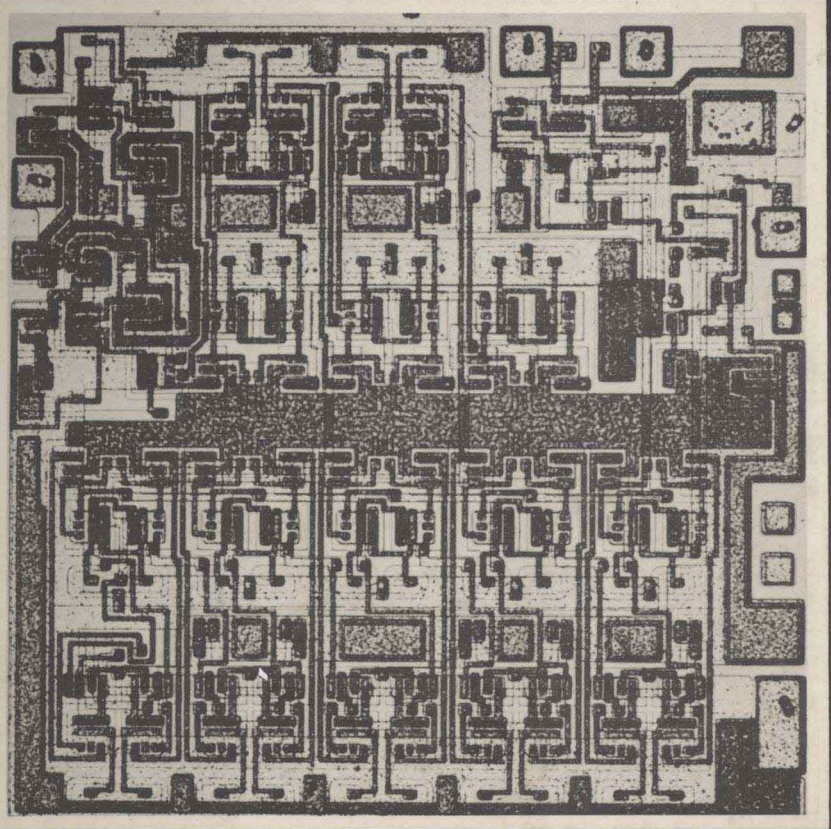
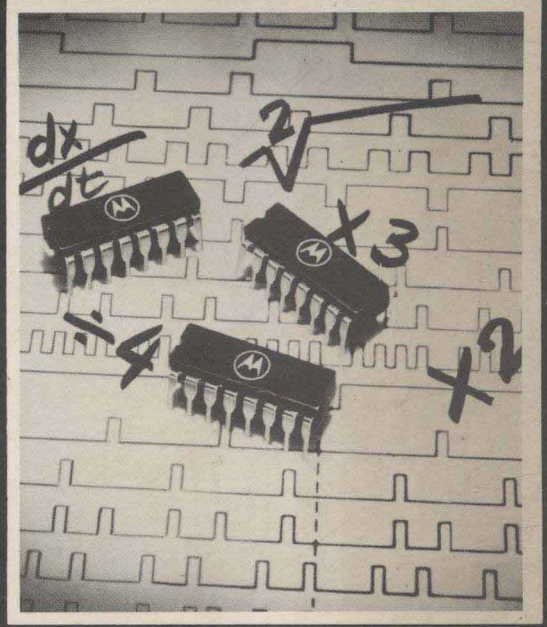
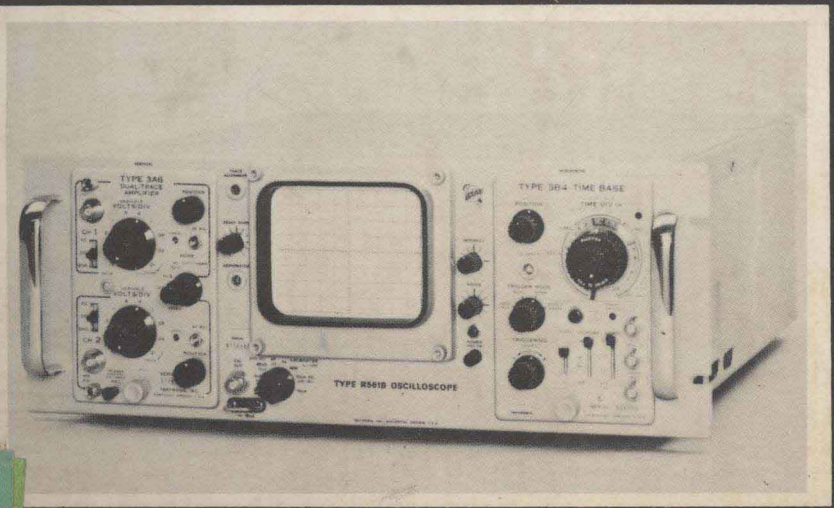
DIGITAL THEORY AND EXPERIMENTATION USING INTEGRATED CIRCUITS

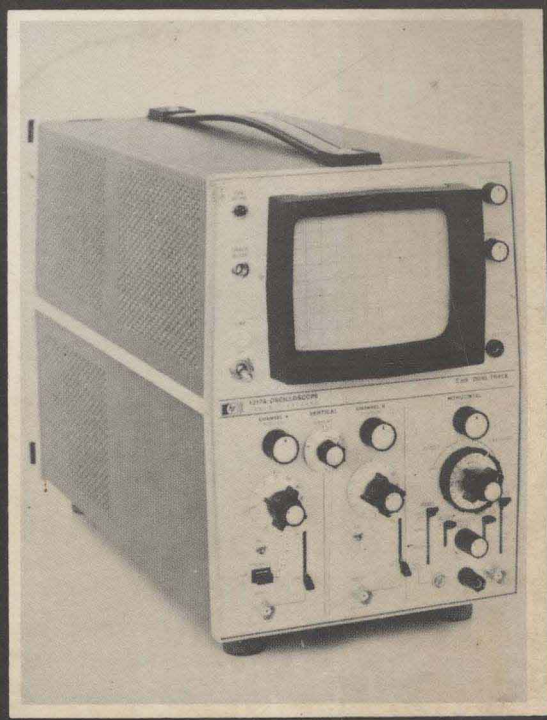
REVISED AND ENLARGED

Morris E. Levine









DIGITAL THEORY AND EXPERIMENTATION USING INTEGRATED CIRCUITS

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Preface

Since the publication of the first edition of this manual, the companion textbook, *Digital Theory and Practice Using Integrated Circuits*, has been published. When the textbook was written, it was organized and coordinated with the laboratory manual to form one integrated course of study in digital electronics with the textbook theoretical development and laboratory experiments following in the same order. In this second edition of the laboratory manual, this organization and coordination has been continued. The laboratory experiments and the text develop the building blocks in the same order with each reinforcing the other.

This laboratory manual has been developed to provide laboratory training and experience in digital electronics using integrated circuits in the laboratory environment of the industrial electronics laboratory. As in the industrial electronics laboratory, all the measurements (with very minor exceptions) are made using the cathode-ray oscilloscope. This manual therefore serves two purposes. Besides providing the digital techniques experience, it also provides intensive and thorough training in the use of the CRO as a universal tool for the measurement and analysis of digital circuits.

There are five primary techniques used for the analysis of digital circuits and theory. They are:

1. Voltage levels
2. Logic levels; 1 or 0, T or F, H or L, ON or OFF
3. Logic diagrams
4. Mapping methods
5. Sequential operations. The CRO is used to demonstrate and perform the analysis. Timing is of extreme importance in sequential digital systems.

The experimental measurements of this manual develop the technique of using the CRO to analyze the timing of sequential systems. All five methods are integrated to advance understanding of digital principles.

Eighteen experiments are included in this manual to provide thorough coverage of digital principles. They begin with a series of experiments on the principles of logic. These are followed with experiments on arithmetic operations. Several experiments cover the material on counters, counter techniques, the binary number system, decoding–encoding, memory techniques, and pulse

generation and pulse shaping and the IC Schmitt trigger. The operational amplifier has become of great importance in digital techniques. Two experiments develop the principles and applications of the op-amp in D/A and A/D conversion. Two experiments with CMOS develop the principles and characteristics of this logic family.

New in this second edition are the following:

1. A section "To the Student" has been added.
2. Experiment 1. The AND and OR gates using diodes have been eliminated. Added is a section using an AND-OR-INVERT gate.
3. Experiment 6. A 4-bit MSI full-adder is used to illustrate how MSI simplifies logic circuity. This IC is used to perform addition and complementary subtraction. LEDs are used to show the logic levels.
4. Experiment 10. A 5-bit MSI shift register is used to simplify the wiring. To provide a visual display of data movement in a shift register, LEDs are used to show the logic levels.
5. Experiment 11. This now combines two experiments from the first edition into one experiment on pulse forming and shaping and the Schmitt trigger.
6. Experiment 12. This is entirely new and discusses integrated-circuit timers: types 74121, 74122, and the 555.
7. Experiment 13. Adds a seven-segment LED display to the experiment on decoding and encoding.
8. Experiment 14. A 64-bit RAM replaces the 16-bit RAM and shows how LSI memories can be used for code conversion.
9. Experiments 17 and 18. These are new and are on CMOS logic. Experiment 17 is on CMOS principles, noise immunity, and high-frequency dissipation. Experiment 18 covers the interface between CMOS and TTL. Although numbered 17 and 18, if one desires to discuss CMOS early in the semester, these experiments can be performed after Experiment 4.

Experiments follow a uniform format and are divided into three sections:

1. The experimental laboratory data. Data tables are marked with the letter E.
2. Required results. The experimental data are analyzed and converted to general logic levels. Corresponding tables are marked R.
3. Discussion. In this section the student is required to answer a series of questions which are based upon the experimental results and which integrate the data and digital theory. Corresponding tables are marked with the letter D.

Many types of IC logic families have been developed. Any one family could be used to provide a complete set of experiments. This manual provides experience with TTL, the operational amplifier, and CMOS.

Whenever possible, an experiment starts with the basic building of a logic operation. Once the principle has been developed, it is replaced by an MSI unit. This provides students with an understanding of the logic and gives them a feeling for the trend in integrated circuits toward MSI and LSI and, in addition, simplifies the wiring of more complex circuits.

All the ICs used in this manual are of the 14-pin or 16-pin dual-in-line (DIP) construction. Appendix G gives constructional details of a laboratory IC socket and switch bank arrangement which readily lends itself to the wiring and breadboarding needs of a laboratory and to squad organization and participation. The IC socket is mounted on a $\frac{1}{8}$ in. aluminum channel and the pins are connected to universal 5-way binding posts. This permits the use of stackable banana plug leads for interconnection.

I wish to express my appreciation to Richard Brown, John Gappa, and Gilbert Bank, laboratory technicians at the College of Staten Island, for their suggestions and assistance, particularly with respect to the socket and switch bank construction; to the students at the College of Staten Island for their help; to Professor Jack Waintraub of Middlesex County College for his suggestions and assistance in the revision of the first edition; to Dr. Irving Kosow, with respect to the format; and to Mrs. Jean Johnson for her assistance, excellent typing, and proofreading of the manuscript.

To the Instructor

The ICs used in the experiments are all in the dual-in-line 14-pin or 16-pin configuration. A convenient method of storage is in the plastic shipping container used by the IC manufacturers for shipping production quantities of ICs to the users.

The ICs used in the experiments (as is true for semiconductors in general) do not have a great overvoltage tolerance before their dissipation is exceeded. The procedure suggested in Appendix A, of calibrating the CRO and checking the power supply voltage against it, if carefully followed at the beginning of each experiment, will protect the ICs against overvoltage and at the same time provide some additional CRO experience.

Voltage measurements should be made to within 0.1 V.

The ICs used have short internal connections and high F_T. If allowed to remain in the active region, there is a great possibility of parasitic oscillation. This can occur in obtaining the transfer characteristics in Experiment 4. The bypass capacitor at the gate input is a parasitic oscillation suppressor. For the same reason, a pulse generator should have a short rise and fall time, especially when toggle flip-flops are being used, to prevent the buildup of oscillations and a resultant false count. Should there be any such suspicion, Schmitt trigger IC types 7413 or 7414 can be used to reduce rise and fall times of pulse generators.

If the pulse generator is square-wave-centered around zero voltage, it cannot be used with the ICs, since they will not accept negative-going gate input voltages. A small-signal diode can be used across the pulse generator to clip the negative-going portion of the wave.

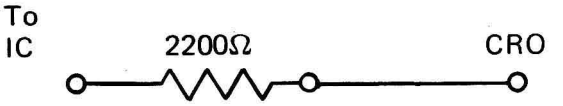
Although the wiring in some of the experiments is somewhat complex, a wiring layout as close as possible to the circuit drawing will help in troubleshooting.

Students should be encouraged to write the values of the logic variables at each point of the logic diagrams in the manual.

If a dual-beam or dual-trace CRO is available, the bistable action of Experiment 8 can best be demonstrated if the beams are displaced horizontally from each other or one beam is operated with a lower brightness.

FLIP-FLOP OUTPUT MEASUREMENTS: A PRECAUTION–CRO ISOLATION

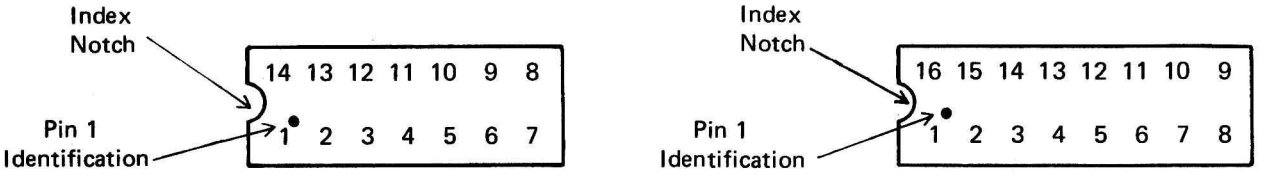
A long lead from a bistable, or counter, or intermediate outputs of a counter, or monostable multivibrator may cause undesired loading and prevent the bistable from toggling or dividing properly, or the monostable from functioning properly. If such difficulties are encountered, a composition 2200-Ω decoupling resistor at the IC end of the lead can eliminate the loading problems. The lead length from the 2200-Ω resistor to the IC should be kept short. This decoupling may be needed both for the CRO vertical input and for external triggering.



IC PIN CONNECTIONS AND IDENTIFICATION

The ICs used in this manual are made in the dual-in-line case. The IC pin terminals progress in a counterclockwise direction as seen from the top side away from the pins. The ICs are in either 14-pin TO-116 (EIA designation) or 16-pin configurations. In these ICs pin 1 is located by an identifying symbol, or the location of pins 1 and 14 (14 pin IC) or pins 1 and 16 (16 pin IC) are identified by an index notch at the end of the case where these pins are located. This is illustrated in the figure below.

Top View (away from pins)



(a) 14-pin TO-116 (b) 16-pin

Dual in-line pin location.

To the Student

Digital electronics has become the most important field in electronics and one of the most important technological fields today. It is involved in all aspects of modern technology, such as data processing, data transmission, radio, TV, timekeeping, industrial control, and instrumentation for many fields of science. Digital electronic circuits and systems are becoming increasingly more complex, yet analysis of such systems will reveal that they are all combinations of simple and basic building blocks.

This laboratory manual was developed to provide you with laboratory experiments and experience to let you more easily understand the theoretical material covered in the classroom, and to provide practical illustrations of how combinations of these simple building blocks can yield complex and useful systems. In addition, the experiments and laboratory experience will provide you with experience in fault analysis and equipment maintenance.

To analyze the performance of these digital blocks, the most useful measuring tool is the cathode-ray oscilloscope (CRO) because it not only measures voltage but it can measure time, displaying both the waveforms of digital electronics and their relative time of occurrence. Almost all of the measurements in this manual are performed using the CRO.

In later experiments the wiring becomes complex. Try to wire them so that the wiring is organized by placing the ICs and switch banks to look like the circuit diagram of the manual. Wire using as short leads as conveniently possible. Leads that are too long introduce capacitive loading and may introduce spurious pulses and glitches, which may give incorrect results in sequential circuits such as counters and shift registers. If trouble occurs, neat and orderly wiring will make it easier to locate the fault.

If trouble does occur, rewire only as a last resort. Try to determine what logic levels should occur at points in the circuit as a result of the input levels. If they do not occur as predicted, slowly disassemble the circuit at that point until you obtain an expected result. The circuit can then be gradually reassembled until the fault reoccurs. Marking the circuit diagram with the Boolean expressions in terms of the logic inputs is of great usefulness.

	555	741C	4001	4007	4050	7400	7402	7403	7404	7405	7406	7410	7414	7420	7432	7441A/141A	7447	7451	7472	7476	7483	7486	7489	7490	7496	74121	74122
1. Basic Logic Functions						1	1		1				1	1			1										
2. Boolean Algebra						1			1	1				1													
3. DeMorgan's Theorem						1	1		1	1			1														
4. TTL NAND/NOR Gates						1		1																			
5. Exclusive OR						1	1		1					1							1						
6. Full Adder/Full Subtractor						1	1		1			1		1							1	1					
7. Bistable						1	1											1									
8. Binary Counters						1							1					3									
9. Divide by N Counters																		4					1				
10. Shift Registers						1													3					1			
11. Pulse Forming/Shaping: Schmitt Trigger						1		1				1															
12. Integrated Circuit Timers: 74122, 74121, 555	1								1																	1	1
13. Decoding/Encoding									1				1		1	1			1				1				
14. Random Access Memories (RAM)						1		1														1					
15. Operational Amplifier		2																									
16. D/A and A/D Conversion		2							1	1													1				
17. CMOS Principles and Characteristics				1																							
18. CMOS – TTL Interface			1		1						1																

Integrated-Circuit Types and Experiments in Which They Are Used

Measure voltages as accurately as possible. Be sure that the CRO is measuring voltage correctly. You can do this by using the CRO internal calibrator. You should be able to measure voltages to within 0.1 V. If you do not need this precision later, you can discard it.

Some of the experiments require graphs. **Plot these as you take the data.** This will reveal data errors and inadequate data.

When CRO sketches are required, they should be drawn carefully on your laboratory manual graphs. They should be drawn accurately enough so that you can read voltage and time from them at any point. Generator waveforms should be displayed on the CRO with respect to the graticule as closely as possible to those shown in the manual. The timing of relative waveforms in a digital system cannot be displayed correctly without external triggering.

Data obtained experimentally with the CRO are in volts. The required (R) section translates these into logic levels 1 and 0. In the discussion (D) section these R logic levels are analyzed. Careful study of the R data and of your textbook will enable you to answer these questions.

Contents

Experiment 1

Basic Logic Functions

OBJECT

1. To study the basic logic functions AND, OR, INVERT, NAND, and NOR.
2. To study the representation of these functions by truth tables, logic diagrams, and Boolean algebra.

INTRODUCTORY THEORY

In electronic logic circuits inputs and outputs occur as voltage levels. These inputs and outputs are dual valued or dual leveled. To provide a common basis for comparison it has become usual to represent the two levels symbolically as 1 or 0. In one circuit the 1 might be +20 V and the 0 might be -10 V. In some other circuit the 1 might be +15 V and the 0 might be +1 V. Despite the difference in voltage levels, a basic operation will be the same using either pair of voltages.

AND: A multi-input circuit in which the output is a 1 only if all inputs are 1.

OR: A multi-input circuit in which the output is a 1 when any input is a 1.

INVERT: The output is 0 when the input is 1, and the output is 1 when the input is 0.

NAND: AND followed by INVERT.

NOR: OR followed by INVERT.

Truth table: Representation of the output logic levels of a logic circuit for every possible combination of levels of the inputs. This is best done by means of a systematic tabulation.

EQUIPMENT REQUIRED

CRO, dc coupled and calibrated
dc power supply, +5 V at 50 mA
IC type 7400 quad 2-input NAND gate
IC type 7402 quad 2-input NOR gate
IC type 7404 hex inverter
IC type 7420 dual 4-input NAND gate
IC type 7432 quad 2-input OR gate
IC type 7451 dual 2-wide, 2-input AND-OR-INVERT gate
Switch bank, 5 switches per bank

IC manufacturers' part numbers.

Type	*Motorola*	*Fairchild*	*Texas Instruments*	*National Semiconductor*
7400	MC7400P MC7400L	7400PC 7400DC	SN7400N SN7400J	DM7400N
7402	MC7402P MC7402L	7402PC 7402DC	SN7402N SN7402J	DM7402N
7404	MC7404P MC7404L	7404PC 7404DC	SN7404N SN7404J	DM7404N
7420	MC7420P MC7420L	7420PC 7420DC	SN7420P SN7420J	DM7420N
7432		7432PC 7432DC	SN7432P SN7432J	DM7432N
7451		7451PC 7451DC	SN7451P SN7451J	DM7451N

IC PIN CONNECTIONS

Each of these ICs are in a 14-pin dual-in-line case. The base pins progress in a counterclockwise direction as seen from the side away from the pins, as shown in Fig. 1-1. Pin 1 is located by an identifying symbol, or the location of pins 1 and 14 are identified by an index notch at the end of the case where pins 1 and 14 are located.

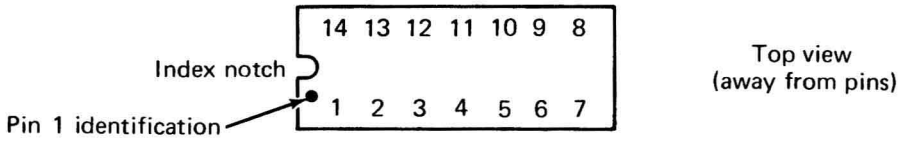


Fig. 1-1. IC pin location, 14-pin dual-in-line (TO-116) case.

PRELIMINARY PRECAUTIONS

The ICs used in this experiment are fragile and have a small voltage overload margin. It is extremely important that the exact required voltage be applied. The power supply voltage should be the last connection made. Before connections to the power supply are made, its voltage should be checked both against its own voltmeter and against the calibrated CRO.

All measurements in this experiment are made with a calibrated CRO. *Before making any measurements, calibrate the CRO* (see Appendix A). After the CRO is calibrated, use it to check the power supply voltage. If a disagreement occurs between the power supply voltmeter reading and the CRO measurement, call the instructor.

EXPERIMENTAL PROCEDURE

For each part of the experiment apply the indicated voltage and make voltage measurements at the points indicated to complete the tables. Use the CRO to measure the voltage. Use a sensitivity of 1 V/div and make measurements to within 0.1 V.

1. IC OR Gate

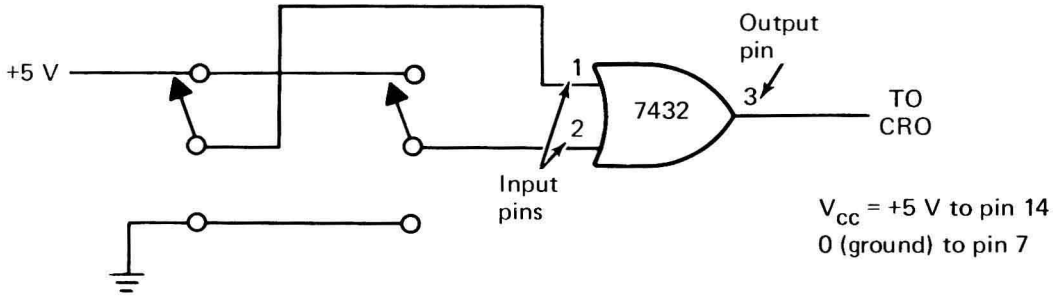


Fig. 1-2. IC OR gate.

Note: The IC type 7432 has four 2-input OR gates within its package. Only one of these gates is used in this experiment. It is the gate whose input pins are pins 1 and 2 and whose output pin is pin 3. See Appendix D for complete logic diagram and pin connections.

Table 1-1E. IC OR gate.

Pin 1	*Pin 2*	*Pin 3*
0	0	
0	+5	
+5	0	
+5	+5	

2. INVERT

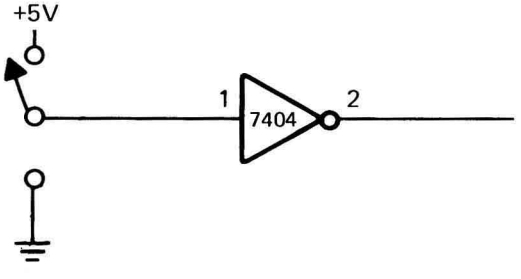


Table 1-2E. INVERT.

Pin 1	*Pin 2*
0	
+5	

Fig. 1-3. IC inverter.

3. OR + INVERT = NOR

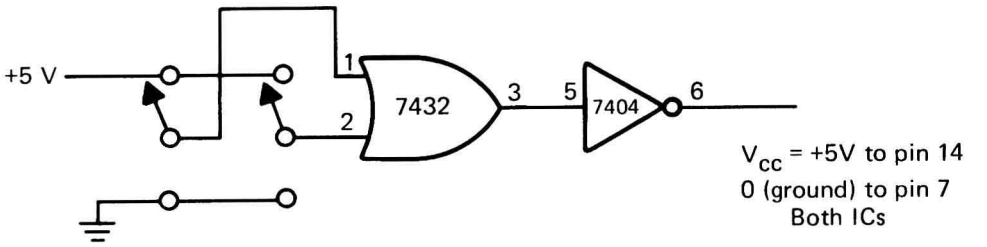


Fig. 1-4. OR + INVERT.

Table 1-3E.

7432		*7404*
Pin 1	*Pin 2*	*Pin 6*
0	0	
0	+5	
+5	0	
+5	+5	

4. NOR

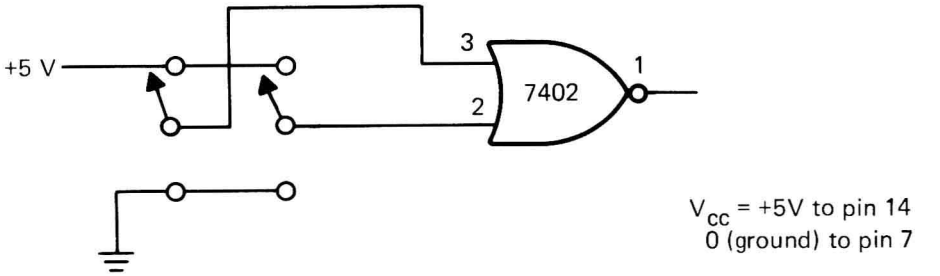


Fig. 1-5. NOR.

Table 1-4E.

Pin 3	*Pin 2*	*Pin 1*
0	0	
0	+5	
+5	0	
+5	+5	