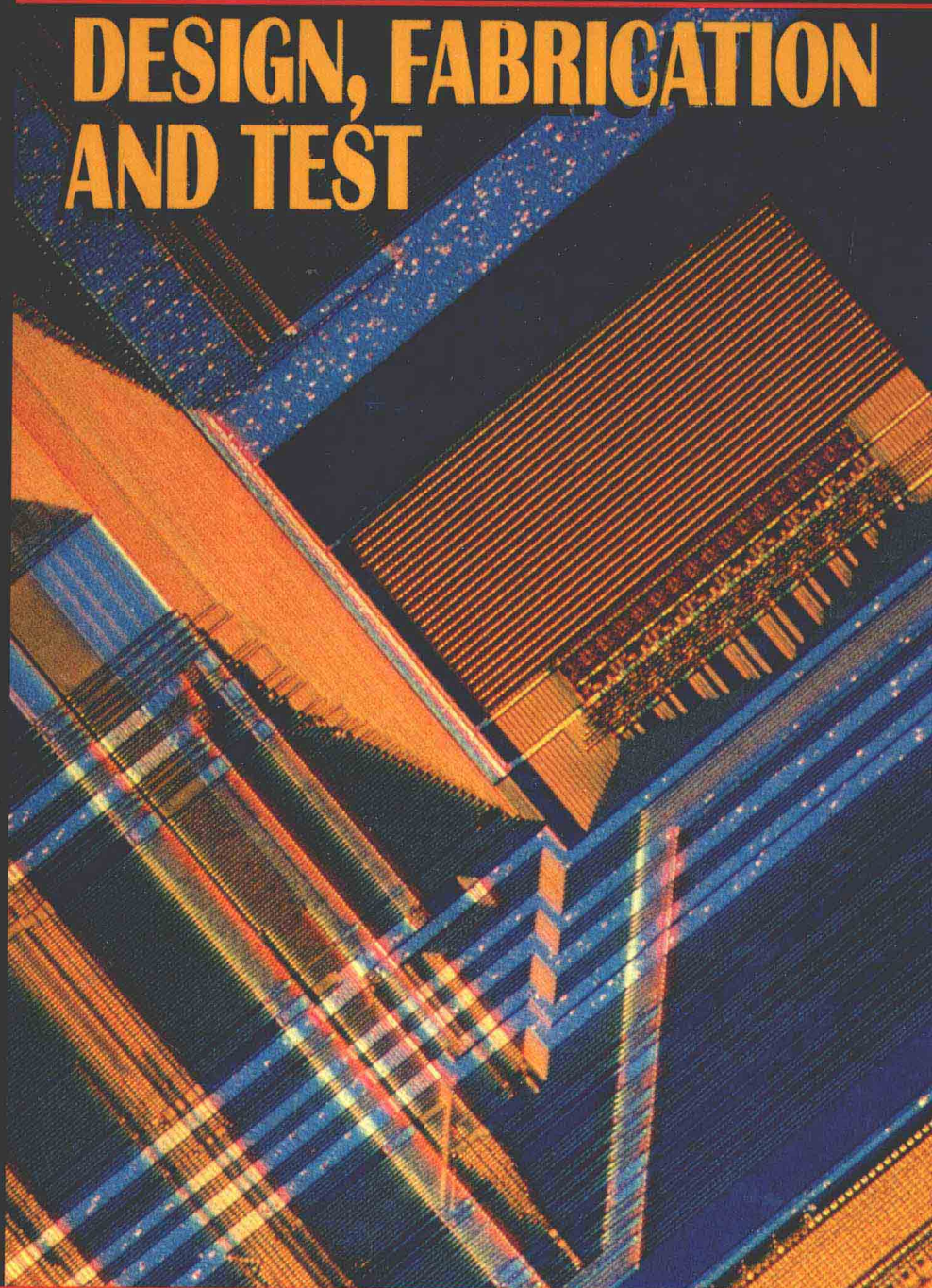
INTEGRATED CIRCUIT DESIGN, FABRICATION AND TEST



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Integrated Circuit Design, Fabrication and Test

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Preface

The world of the monolithic integrated circuit (the 'chip') had its beginnings in the early 1960s and, over the intervening years, has seen a massive increase in the complexity of circuit, the number of chips produced, the speed of the circuits and the different applications to which they are put. It can be truly said that there has been a revolution in electronic engineering due to the chip. Corresponding with the growth of the chip market has been the number of books available that describe the various aspects of chip design, technology, manufacture and, more recently, computer aids available to the engineer. The question you may justifiably ask as you hold this book in your hands is: why another?

The growth of available circuit complexity has remained on its exponential increase, with approximately a 100-fold increase in the number of available transistors on a chip every 10 years. This has taken the state of the art through from the initial small scale integration (SSI), about 10 devices per chip (1960), through medium scale integration (MSI), 1000 devices (1970), large scale integration (LSI), 10 000 devices (1980), to very large scale integration (VLSI), 1 million devices and beyond at the present day. However, until around 5 to 10 years ago, owing to the economics of chip design and manufacture, the only people involved in these activities were engineers employed by large electronics firms or in the IC foundries.

There has, however, been a second revolution within the chip technology area. With the more readily available computer aids, and IC foundries offering custom fabrication in multi-project wafers (MPWs) at affordable prices, the number of chip designers has increased out of all proportion to the general growth in the chip market. The field is now open to small companies to incorporate application-specific ICs (ASICs), which have been custom designed in-house, into their products. Research workers, academics and even undergraduate students are acquiring experience of the software tools, design techniques and manufacturing and testing processes. It is to this new breed of chip engineers that this book is directed.

The book is designed as an introduction to *all* the aspects of chip realization. As has already been noted, there are numerous books on the market that cover many of the aspects of IC engineering to varying degrees of depth. This book however discusses all aspects – design, manufacture and test of both digital and analogue circuits. It will help the engineer or student who is faced with the task of chip design for the first time and who requires some help

through the mystifying maze of tools, technologies and techniques available. These aspects make the book unique.

As the book covers so many aspects and is designed at an affordable price, the depth of coverage is not great, but there is an extensive Bibliography at the end of each main chapter which the enthusiastic reader can use to pursue particular aspects to any required depth. These lists of further reading include books that the author has found to be of use in preparing the chapter material, and other relevant titles. References are given at the end of each chapter, if relevant.

Chapter 1 is an introduction to ICs, a summary of the design process and some of the considerations that must be made when a new IC is proposed. These include the choice of the appropriate technology and circuit architecture, planning the design, power considerations, testing and the economics of the product. The remaining chapters expand on these various aspects.

Chapter 2 describes the various families of technologies that are available for IC realization, detailing the properties of each and highlighting their various advantages and disadvantages.

Chapter 3 is involved in the detailed circuit design of the basic building blocks for each technology and covers both analogue and digital circuits.

In Chapter 4 the various architectures of the ICs are described, again detailing the advantages and disadvantages of each and when each should be used in preference to the others.

Chapter 5 is concerned with the computer tools that are available to the engineer in order to make the realization of an IC possible. The different function of each type of tool and the role it plays in the overall design process are detailed.

Chapter 6 describes the techniques for testing the devices, including the aspects of design for testability that must be incorporated into the design process from the start.

Appendix 1 covers the aspects of IC fabrication. Although it is not essential for the engineer to have a detailed knowledge of these processes to design an IC successfully (hence the positioning of this material outside the main text), these aspects do impinge on many of the design and test considerations. It is therefore strongly recommended to readers that if they have little or no knowledge of these aspects, then Appendix 1 material should be referred to before reading the main part of the book.

Appendix 2 describes an example of a simple IC design, covering virtually all of the aspects described in the main chapters. This IC is the product of a Final Year Design Study undertaken by students on the BEng Electronics and Communication Engineering Course at the University of Bath.

A small number of questions are included at the end of each chapter. The amount of mathematics used in the book has deliberately been kept to a minimum, but these exercises will give readers a chance to apply some of the

ideas described in the text and to extend their insight into some of the concepts and problems.

I would like to thank John Martin of the University of Bath for his collaboration in the Final Year Design Project and for other useful conversations. Also Ian Walton and Richard Parkinson, the students who designed the example IC, for their permission to use the circuit description and results. I am grateful to European Silicon Structures for their permission to publish some of the details of the SOLO 1400 software and the IC fabrication route. I would also like to thank Mahmoud Al-Qutayri of DeMontfort University for permission to use some testing examples from his PhD thesis.

This book is dedicated to Barbara, who has made my life complete.

PETER SHEPHERD

Glossary of Abbreviations

a.c.	alternating current
ADC	Analogue–Digital Converter
ALSTTL	Advanced Low Power Schottky TTL
ALU	Arithmetic Logic Unit
ASIC	Application Specific Integrated Circuit
ASTTL	Advanced Schottky TTL
ATE	Automatic Test Equipment
ATPG	Automatic Test Pattern Generation
BILBO	Built-In Logic Block Observer
BIST	Built-In Self-Test
BJT	Bipolar Junction Transistor
BSDL	Boundary Scan Description Language
CAD	Computer-Aided Design
CAE	Computer-Aided Engineering
CAT	Computer-Aided Test
CIF	Caltech Intermediate Format
CMOS	Complementary Metal–Oxide Semiconductor
CMRR	Common Mode Rejection Ratio
CVD	Chemical Vapour Deposition
DAC	Digital–Analogue Converter
d.c.	direct current
DFT	Design For Testability
DIL	Dual-In-Line
DRAM	Dynamic RAM
DSP	Digital Signal Processing
DTL	Diode Transistor Logic
ECAD	Electronic Computer-Aided Design
ECL	Emitter Coupled Logic
EDIF	Electronic Design Interchange Format
EEPROM	Electronically Erasable Programmable ROM
EPROM	Erasable Programmable ROM

FET	Field Effect Transistor
FFT	Fast Fourier Transform
FPGA	Field Programmable Gate Array
FSM	Finite State Machine
GaAs	Gallium Arsenide
GOS	Gate Oxide Short
HBT	Heterojunction Bipolar Transistor
HDL	Hardware Description Language
IC	Integrated Circuit
IEEE	Institute of Electrical and Electronic Engineers
InP	Indium Phosphide
I/O	Input–Output
JFET	Junction Field Effect Transistor
JTAG	Joint Test Action Group
LFSR	Linear Feedback Shift Register
LPE	Liquid Phase Epitaxy
LSB	Least Significant Bit
LSI	Large Scale Integration
LSR	Linear Shift Register
LSSD	Level Sensitive Scan Design
LSTTL	Low Power Schottky TTL
MBE	Molecular Beam Epitaxy
MCM	Multi-Chip Module
MESFET	MEtal–Semiconductor FET
MOCVD	Metal Organic Chemical Vapour Deposition
MOS	Metal–Oxide–Semiconductor
MPW	Multi-Project Wafer
MSB	Most Significant Bit
MSI	Medium Scale Integration
nMOS	n-channel MOS
PAL	Programmable Array Logic
PCB	Printed Circuit Board
PLA	Programmable Logic Array
PLD	Programmable Logic Device
pMOS	p-channel MOS
PRBS	Pseudo Random Binary Sequence

PROM	Programmable ROM
PSRR	Power Supply Rejection Ratio
QTAG	Quality Test Action Group
RAM	Random Access Memory
r.f.	radio frequency
RIBE	Reactive Ion Beam Etching
RIE	Reactive Ion Etching
ROM	Read Only Memory
RTL	Resistor Transistor Logic (Chapter 2)
RTL	Register Transfer Level (Chapter 5)
s-c	switched-capacitor
SDI	Scan Data Input
SDO	Scan Data Output
SI	Semi-Insulating
SPICE	Simulation Program with Integrated Circuit Emphasis
SRAM	Static RAM
SRL	Shift Register Latch
SSI	Small Scale Integration
STTL	Schottky TTL
TC	Temperature Coefficient
TTL	Transistor Transistor Logic
ULM	Universal Logic Module
ULSI	Ultra Large Scale Integration
VHDL	VHSIC Hardware Description Language
VHSIC	Very High Speed Integrated Circuit
VLSI	Very Large Scale Integration
VPE	Vapour Phase Epitaxy
WSI	Wafer Scale Integration

Contents

1 The IC Design Process Where do we start?

1.1 Introduction – a brief history of ICs

Integrated circuits (ICs) have their origin in the development of the solid-state equivalent of the thermionic valve – the transistor. Bipolar junction transistors (BJTs) were first developed in the late 1940s by Brattin, Bardeen and Schockley at Bell Laboratories, although point contact diodes ('cats whiskers') were in use before the Second World War, and the field effect transistor had been proposed but not successfully realized in the early 1930s.

Transistors continued to develop during the 1950s, originally based on germanium, and by the early 1960s cheap, reliable, silicon-based devices were commonly in use. These devices were all discrete, packaged individually, and then had to be mounted on circuit boards with other discrete components such as resistors and capacitors. The use of active devices in the realization of digital logic gates for computing processes had been employed for some time, based on valve circuits. The resulting computers were huge in size, and very inefficient, and the advantages of solid-state devices in terms of size and power consumption were soon to be appreciated. The integration of more than one component into a self-contained circuit was driven forward by this need. In fact, two forms of IC developed: the hybrid circuit, where the passive components and interconnections are manufactured using a 'thick-film' technique on a dielectric (usually alumina) substrate, the active devices being attached in their unpackaged 'chip' form to complete the circuit; and the alternative monolithic IC, where all the circuit components are generated in a 'thin-film' technique in which all the components and interconnections are on the semiconductor substrate. The latter has advantages in size and reliability and the hybrid IC is now very rare except for specialized applications, such as microwave integrated circuits.

So the first monolithic ICs, which emerged around 1960, consisted of just a few transistors, realizing individual logic gate functions or analogue amplifier circuits. Such circuits are termed small scale integration (SSI). As the process reliability and computer design tools developed, so the integration levels, in terms of the number of transistors per IC, have grown almost exponentially with time, as illustrated in Figure 1.1. With each decade of transistor numbers, there came a new term for the level of integration, as summarized below:

Nomenclature	*No. of transistors*
Small scale integration (SSI)	1–100
Medium scale integration (MSI)	100–1 000
Large scale integration (LSI)	1000–10 000
Very large scale integration (VLSI)	10 000–100 000
Ultra large scale integration (ULSI)	100 000–1 000 000
Wafer scale integration (WSI)	over 1 000 000

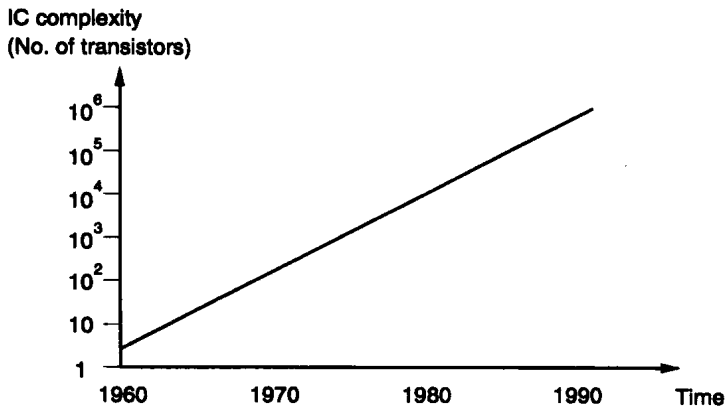

Figure 1.1 Growth in IC complexity with time

Note that technically the term VLSI is applied to circuits with transistor counts between ten thousand and a hundred thousand; but in practice the term has come into common use for virtually any monolithic IC, digital or analogue, and it is not unusual to see it applied to circuits that are MSI in complexity!

1.2 The design cycle

The design of a circuit comprising a million plus active devices is a daunting task. The complete design process from specification to IC realization has generally been beyond the scope of a single designer, as the total work load involved has often been of the order of several man-years. Teams of designers working together meant that new products could be completed within a year of real time. As competition for new markets and new products has accelerated in recent years, the complexity and power of the computer aids to design have reduced the work load to the order of man-months, and it is now within the scope of a single (very skilled!) designer to generate a complete IC within a reasonable time. However, to ensure quality of the product the design process must be well specified, with rigorous checks at each stage to ensure, as far as is practical, freedom from errors which would be expensive and time consuming to correct at a later stage of the process. This section briefly