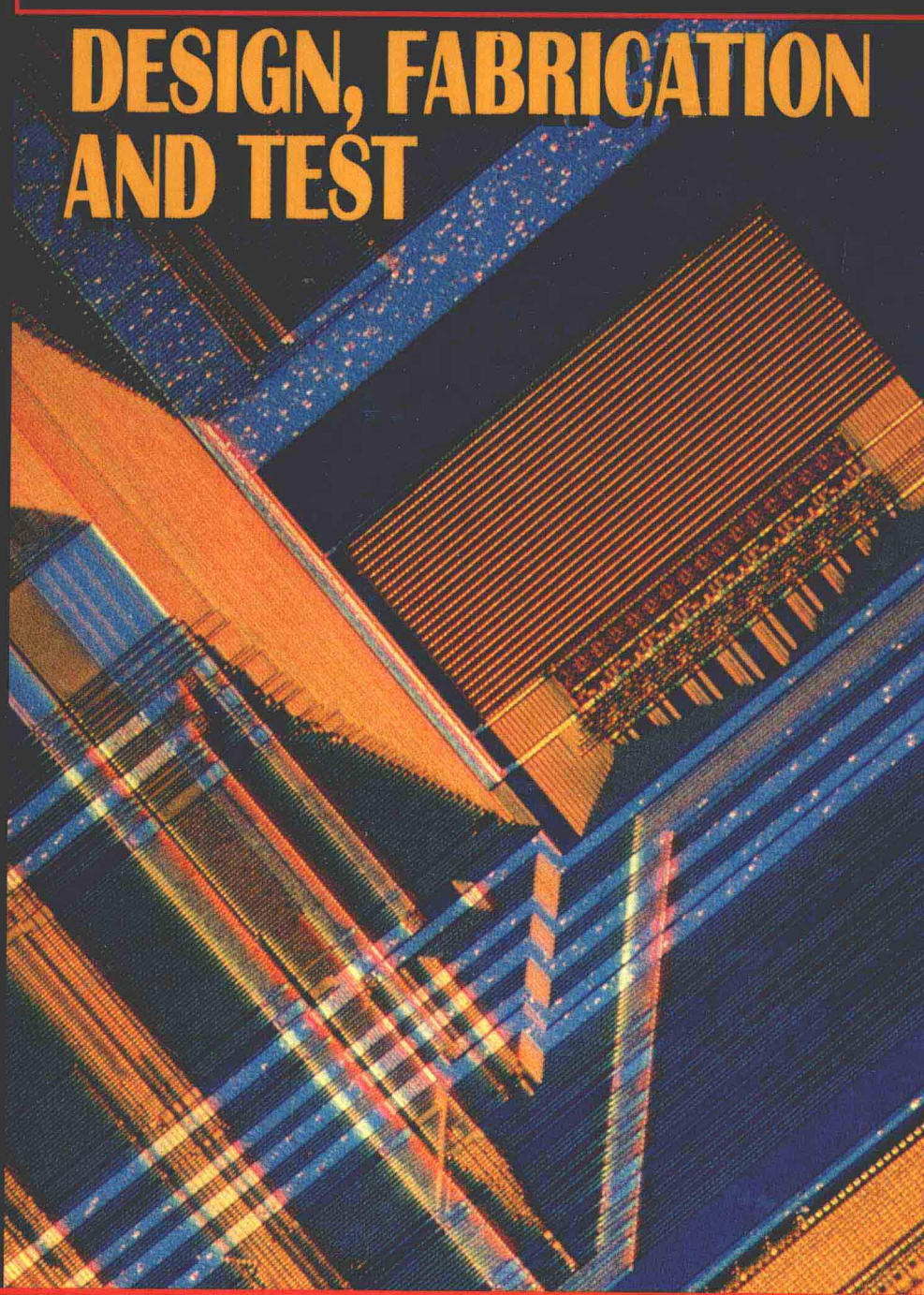


# **INTEGRATED CIRCUIT**

# **DESIGN, FABRICATION AND TEST**



**PETER R. SHEPHERD**

# **Integrated Circuit Design, Fabrication and Test**

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**Integrated Circuit  
Design, Fabrication and Test**

# Preface

The world of the monolithic integrated circuit (the 'chip') had its beginnings in the early 1960s and, over the intervening years, has seen a massive increase in the complexity of circuit, the number of chips produced, the speed of the circuits and the different applications to which they are put. It can be truly said that there has been a revolution in electronic engineering due to the chip. Corresponding with the growth of the chip market has been the number of books available that describe the various aspects of chip design, technology, manufacture and, more recently, computer aids available to the engineer. The question you may justifiably ask as you hold this book in your hands is: why another?

The growth of available circuit complexity has remained on its exponential increase, with approximately a 100-fold increase in the number of available transistors on a chip every 10 years. This has taken the state of the art through from the initial small scale integration (SSI), about 10 devices per chip (1960), through medium scale integration (MSI), 1000 devices (1970), large scale integration (LSI), 10 000 devices (1980), to very large scale integration (VLSI), 1 million devices and beyond at the present day. However, until around 5 to 10 years ago, owing to the economics of chip design and manufacture, the only people involved in these activities were engineers employed by large electronics firms or in the IC foundries.

There has, however, been a second revolution within the chip technology area. With the more readily available computer aids, and IC foundries offering custom fabrication in multi-project wafers (MPWs) at affordable prices, the number of chip designers has increased out of all proportion to the general growth in the chip market. The field is now open to small companies to incorporate application-specific ICs (ASICs), which have been custom designed in-house, into their products. Research workers, academics and even undergraduate students are acquiring experience of the software tools, design techniques and manufacturing and testing processes. It is to this new breed of chip engineers that this book is directed.

The book is designed as an introduction to *all* the aspects of chip realization. As has already been noted, there are numerous books on the market that cover many of the aspects of IC engineering to varying degrees of depth. This book however discusses all aspects – design, manufacture and test of both digital and analogue circuits. It will help the engineer or student who is faced with the task of chip design for the first time and who requires some help

through the mystifying maze of tools, technologies and techniques available. These aspects make the book unique.

As the book covers so many aspects and is designed at an affordable price, the depth of coverage is not great, but there is an extensive Bibliography at the end of each main chapter which the enthusiastic reader can use to pursue particular aspects to any required depth. These lists of further reading include books that the author has found to be of use in preparing the chapter material, and other relevant titles. References are given at the end of each chapter, if relevant.

Chapter 1 is an introduction to ICs, a summary of the design process and some of the considerations that must be made when a new IC is proposed. These include the choice of the appropriate technology and circuit architecture, planning the design, power considerations, testing and the economics of the product. The remaining chapters expand on these various aspects.

Chapter 2 describes the various families of technologies that are available for IC realization, detailing the properties of each and highlighting their various advantages and disadvantages.

Chapter 3 is involved in the detailed circuit design of the basic building blocks for each technology and covers both analogue and digital circuits.

In Chapter 4 the various architectures of the ICs are described, again detailing the advantages and disadvantages of each and when each should be used in preference to the others.

Chapter 5 is concerned with the computer tools that are available to the engineer in order to make the realization of an IC possible. The different function of each type of tool and the role it plays in the overall design process are detailed.

Chapter 6 describes the techniques for testing the devices, including the aspects of design for testability that must be incorporated into the design process from the start.

Appendix 1 covers the aspects of IC fabrication. Although it is not essential for the engineer to have a detailed knowledge of these processes to design an IC successfully (hence the positioning of this material outside the main text), these aspects do impinge on many of the design and test considerations. It is therefore strongly recommended to readers that if they have little or no knowledge of these aspects, then Appendix 1 material should be referred to before reading the main part of the book.

Appendix 2 describes an example of a simple IC design, covering virtually all of the aspects described in the main chapters. This IC is the product of a Final Year Design Study undertaken by students on the BEng Electronics and Communication Engineering Course at the University of Bath.

A small number of questions are included at the end of each chapter. The amount of mathematics used in the book has deliberately been kept to a minimum, but these exercises will give readers a chance to apply some of the

ideas described in the text and to extend their insight into some of the concepts and problems.

I would like to thank John Martin of the University of Bath for his collaboration in the Final Year Design Project and for other useful conversations. Also Ian Walton and Richard Parkinson, the students who designed the example IC, for their permission to use the circuit description and results. I am grateful to European Silicon Structures for their permission to publish some of the details of the SOLO 1400 software and the IC fabrication route. I would also like to thank Mahmoud Al-Qutayri of DeMontfort University for permission to use some testing examples from his PhD thesis.

This book is dedicated to Barbara, who has made my life complete.

**PETER SHEPHERD**

# Glossary of Abbreviations

a.c.	alternating current
ADC	Analogue–Digital Converter
ALSTTL	Advanced Low Power Schottky TTL
ALU	Arithmetic Logic Unit
ASIC	Application Specific Integrated Circuit
ASTTL	Advanced Schottky TTL
ATE	Automatic Test Equipment
ATPG	Automatic Test Pattern Generation
BILBO	Built-In Logic Block Observer
BIST	Built-In Self-Test
BJT	Bipolar Junction Transistor
BSDL	Boundary Scan Description Language
CAD	Computer-Aided Design
CAE	Computer-Aided Engineering
CAT	Computer-Aided Test
CIF	Caltech Intermediate Format
CMOS	Complementary Metal–Oxide Semiconductor
CMRR	Common Mode Rejection Ratio
CVD	Chemical Vapour Deposition
DAC	Digital–Analogue Converter
d.c.	direct current
DFT	Design For Testability
DIL	Dual-In-Line
DRAM	Dynamic RAM
DSP	Digital Signal Processing
DTL	Diode Transistor Logic
ECAD	Electronic Computer-Aided Design
ECL	Emitter Coupled Logic
EDIF	Electronic Design Interchange Format
EEPROM	Electrically Erasable Programmable ROM
EPROM	Erasable Programmable ROM



<b>FET</b>	<b>Field Effect Transistor</b>
<b>FFT</b>	<b>Fast Fourier Transform</b>
<b>FPGA</b>	<b>Field Programmable Gate Array</b>
<b>FSM</b>	<b>Finite State Machine</b>
<b>GaAs</b>	<b>Gallium Arsenide</b>
<b>GOS</b>	<b>Gate Oxide Short</b>
<b>HBT</b>	<b>Heterojunction Bipolar Transistor</b>
<b>HDL</b>	<b>Hardware Description Language</b>
<b>IC</b>	<b>Integrated Circuit</b>
<b>IEEE</b>	<b>Institute of Electrical and Electronic Engineers</b>
<b>InP</b>	<b>Indium Phosphide</b>
<b>I/O</b>	<b>Input–Output</b>
<b>JFET</b>	<b>Junction Field Effect Transistor</b>
<b>JTAG</b>	<b>Joint Test Action Group</b>
<b>LFSR</b>	<b>Linear Feedback Shift Register</b>
<b>LPE</b>	<b>Liquid Phase Epitaxy</b>
<b>LSB</b>	<b>Least Significant Bit</b>
<b>LSI</b>	<b>Large Scale Integration</b>
<b>LSR</b>	<b>Linear Shift Register</b>
<b>LSSD</b>	<b>Level Sensitive Scan Design</b>
<b>LSTTL</b>	<b>Low Power Schottky TTL</b>
<b>MBE</b>	<b>Molecular Beam Epitaxy</b>
<b>MCM</b>	<b>Multi-Chip Module</b>
<b>MESFET</b>	<b>MEtal–Semiconductor FET</b>
<b>MOCVD</b>	<b>Metal Organic Chemical Vapour Deposition</b>
<b>MOS</b>	<b>Metal–Oxide–Semiconductor</b>
<b>MPW</b>	<b>Multi-Project Wafer</b>
<b>MSB</b>	<b>Most Significant Bit</b>
<b>MSI</b>	<b>Medium Scale Integration</b>
<b>nMOS</b>	<b>n-channel MOS</b>
<b>PAL</b>	<b>Programmable Array Logic</b>
<b>PCB</b>	<b>Printed Circuit Board</b>
<b>PLA</b>	<b>Programmable Logic Array</b>
<b>PLD</b>	<b>Programmable Logic Device</b>
<b>pMOS</b>	<b>p-channel MOS</b>
<b>PRBS</b>	<b>Pseudo Random Binary Sequence</b>

<b>PROM</b>	<b>Programmable ROM</b>
<b>PSRR</b>	<b>Power Supply Rejection Ratio</b>
<b>QTAG</b>	<b>Quality Test Action Group</b>
<b>RAM</b>	<b>Random Access Memory</b>
<b>r.f.</b>	<b>radio frequency</b>
<b>RIBE</b>	<b>Reactive Ion Beam Etching</b>
<b>RIE</b>	<b>Reactive Ion Etching</b>
<b>ROM</b>	<b>Read Only Memory</b>
<b>RTL</b>	<b>Resistor Transistor Logic (Chapter 2)</b>
<b>RTL</b>	<b>Register Transfer Level (Chapter 5)</b>
<b>s-c</b>	<b>switched-capacitor</b>
<b>SDI</b>	<b>Scan Data Input</b>
<b>SDO</b>	<b>Scan Data Output</b>
<b>SI</b>	<b>Semi-Insulating</b>
<b>SPICE</b>	<b>Simulation Program with Integrated Circuit Emphasis</b>
<b>SRAM</b>	<b>Static RAM</b>
<b>SRL</b>	<b>Shift Register Latch</b>
<b>SSI</b>	<b>Small Scale Integration</b>
<b>STTL</b>	<b>Schottky TTL</b>
<b>TC</b>	<b>Temperature Coefficient</b>
<b>TTL</b>	<b>Transistor Transistor Logic</b>
<b>ULM</b>	<b>Universal Logic Module</b>
<b>ULSI</b>	<b>Ultra Large Scale Integration</b>
<b>VHDL</b>	<b>VHSIC Hardware Description Language</b>
<b>VHSIC</b>	<b>Very High Speed Integrated Circuit</b>
<b>VLSI</b>	<b>Very Large Scale Integration</b>
<b>VPE</b>	<b>Vapour Phase Epitaxy</b>
<b>WSI</b>	<b>Wafer Scale Integration</b>

# Contents

<i>Preface</i>	x
<i>Glossary of Abbreviations</i>	xiii
<b>1 The IC Design Process – Where do we start?</b>	<b>1</b>
1.1 Introduction – a brief history of ICs	1
1.2 The design cycle	2
1.3 Design considerations	5
1.3.1 Technology and architecture	5
1.3.2 Top-down or bottom-up?	7
1.3.3 Packaging and floorplanning	8
1.3.4 Power considerations	9
1.4 Computer aids for design and manufacture	12
1.5 Testing	14
1.6 Economics	15
1.6.1 Example of an economic forecast	17
Bibliography	19
Questions	19
<b>2 IC Families – What technologies can we use?</b>	<b>21</b>
2.1 Introduction	21
2.2 Transistor types	22
2.2.1 Bipolar junction transistor	22
2.2.2 Field effect transistors	23
2.2.3 Comparison of BJT and FET devices	26
2.3 Digital circuits	27
2.3.1 TTL	27
2.3.2 ECL	31
2.3.3 MOS	32
2.3.4 CMOS	34
2.3.5 Comparison of digital technologies	35
2.4 Analogue circuits	36
2.5 Gallium arsenide and microwave circuits	38
2.5.1 Device realization	38
Bibliography	40
Questions	41

<b>3</b>	<b>Transistor-Level Design – What are the building blocks?</b>	<b>42</b>
3.1	Introduction	42
3.2	Digital circuits	42
3.3	TTL gates	43
3.4	ECL gates	46
3.5	nMOS gates	50
3.5.1	Derivation of voltage–current relationships	51
3.5.2	The nMOS inverter	53
3.5.3	Inverter transfer characteristics	57
3.5.4	Inverter switching speeds	59
3.5.5	Other nMOS gates	60
3.5.6	Pass transistors	61
3.5.7	Buffer circuits	62
3.6	CMOS gates	66
3.6.1	The CMOS inverter	66
3.6.2	Other CMOS gates	68
3.6.3	Transmission gate	69
3.7	Analogue circuits	70
3.7.1	Capacitors	70
3.7.2	Switches	71
3.7.3	Reference circuits	72
3.7.4	Operational amplifiers	76
3.7.5	Comparators	81
3.7.6	Switched capacitor circuits	85
3.7.7	Analogue-to-digital and digital-to-analogue circuits	87
	References	95
	Bibliography	95
	Questions	95
<b>4</b>	<b>IC Realization – How does it come together?</b>	<b>97</b>
4.1	Introduction	97
4.2	Universal ICs	98
4.2.1	Gate packages	98
4.2.2	Microprocessors	99
4.2.3	Memory circuits	100
4.2.4	Analogue circuits	101
4.3	Programmable logic devices	102
4.3.1	Basic PLA layout	102
4.3.2	Variations of the PLA	105
4.3.3	Sequential logic in PLAs	105
4.4	Gate arrays	106
4.4.1	Mask programmable gate arrays	107
4.4.2	Field programmable gate arrays	108
4.4.3	Primitive cell design	108

4.5	Standard cell	111
4.6	Full custom circuits	112
4.7	Analogue ASICs	113
4.8	Multi-chip modules	113
	Reference	116
	Bibliography	116
	Questions	116
<b>5</b>	<b>CAD – How can we make the tasks possible?</b>	<b>117</b>
5.1	Introduction	117
5.1.1	Hierarchical levels	117
5.2	Circuit drawing	118
5.3	Simulation	120
5.3.1	Digital simulation	121
5.3.2	Analogue simulation	122
5.3.3	SPICE	124
5.4	Hardware description languages	128
5.4.1	HDL examples	128
5.4.2	VHDL	133
5.5	Layout	137
5.5.1	Layout examples	138
5.5.2	Automatic layout and routing	140
5.6	Circuit extraction	142
5.7	Synthesis approaches – silicon compilers	143
	Reference	144
	Bibliography	144
	Questions	144
<b>6</b>	<b>Testing – How can we check it works?</b>	<b>146</b>
6.1	Introduction	146
6.2	Fault modelling and test strategies	148
6.2.1	Fault modelling	148
6.2.2	Testing strategies	149
6.2.3	‘Stuck-at’ faults	149
6.2.4	Controllability and observability	150
6.2.5	Test pattern generation techniques	151
6.2.6	D-algorithm	151
6.2.7	Boolean difference	153
6.2.8	Other fault models	154
6.3	Design for testability	156
6.3.1	Test enhancements	157
6.3.2	Scan path approaches	159
6.3.3	Built-in self-test (BIST)	163
6.4	Supply current testing	166

6.4.1	Practical implementation of IDDq	167
6.5	Analogue test	168
6.5.1	Analogue fault modelling	168
6.5.2	Analogue test strategies	170
6.6	Mixed-signal test	171
6.6.1	DSP emulation of analogue test equipment	172
6.6.2	Other approaches to mixed-signal test	173
	References	174
	Bibliography	175
	Questions	175
<b>7</b>	<b>Afterword – The future</b>	<b>176</b>
7.1	Introduction	176
7.2	Fabrication technology	176
7.2.1	Dimension reductions	176
7.2.2	Device speeds	177
7.2.3	Supply voltages	178
7.3	Technologies	178
7.4	CAD	179
7.5	Testing	180
7.6	Conclusion	181
	<b>Appendix 1: The Fabrication Process</b>	<b>182</b>
A1.1	Semiconductors	182
A1.2	Material preparation	184
A1.2.1	Epitaxial growth	186
A1.3	Photolithography	187
A1.3.1	Basic photolithographic process	187
A1.3.2	Mask alignment	188
A1.3.3	Electron beam lithography	189
A1.4	Doping and ion implantation	189
A1.4.1	Diffusion	190
A1.4.2	Practical diffusion systems	192
A1.4.3	Ion implantation	194
A1.5	Oxide and other dielectric layers	195
A1.5.1	Thermal oxidation	196
A1.5.2	Deposited oxide layers	196
A1.5.3	Nitride layers	196
A1.5.4	Polycrystalline silicon	197
A1.6	Etching	197
A1.6.1	Wet etching processes	198
A1.6.2	Dry etching	200
A1.7	Metallization	200
A1.8	Passivation and assembly	202

A1.9	Examples of basic processes	203
A1.9.1	Bipolar process	204
A1.9.2	nMOS process	205
A1.9.3	CMOS process	206
	Bibliography	208
<b>Appendix 2: IC Design Example</b>		<b>209</b>
A2.1	Introduction	209
A2.2	Design specification	209
A2.2.1	Theory	209
A2.2.2	Circuit specification	210
A2.3	Design and manufacture technologies	211
A2.4	Design approach	211
A2.5	Circuit simulation	215
A2.6	Circuit layout	216
A2.7	Post-layout simulation	216
A2.8	Design submission	217
A2.9	Post-fabrication testing	219
A2.10	Conclusion	219
<i>Index</i>		220

# 1 The IC Design Process

## Where do we start?

### 1.1 Introduction – a brief history of ICs

Integrated circuits (ICs) have their origin in the development of the solid-state equivalent of the thermionic valve – the transistor. Bipolar junction transistors (BJTs) were first developed in the late 1940s by Brattin, Bardeen and Schockley at Bell Laboratories, although point contact diodes (‘cats whiskers’) were in use before the Second World War, and the field effect transistor had been proposed but not successfully realized in the early 1930s.

Transistors continued to develop during the 1950s, originally based on germanium, and by the early 1960s cheap, reliable, silicon-based devices were commonly in use. These devices were all discrete, packaged individually, and then had to be mounted on circuit boards with other discrete components such as resistors and capacitors. The use of active devices in the realization of digital logic gates for computing processes had been employed for some time, based on valve circuits. The resulting computers were huge in size, and very inefficient, and the advantages of solid-state devices in terms of size and power consumption were soon to be appreciated. The integration of more than one component into a self-contained circuit was driven forward by this need. In fact, two forms of IC developed: the hybrid circuit, where the passive components and interconnections are manufactured using a ‘thick-film’ technique on a dielectric (usually alumina) substrate, the active devices being attached in their unpackage ‘chip’ form to complete the circuit; and the alternative monolithic IC, where all the circuit components are generated in a ‘thin-film’ technique in which all the components and interconnections are on the semiconductor substrate. The latter has advantages in size and reliability and the hybrid IC is now very rare except for specialized applications, such as microwave integrated circuits.

So the first monolithic ICs, which emerged around 1960, consisted of just a few transistors, realizing individual logic gate functions or analogue amplifier circuits. Such circuits are termed small scale integration (SSI). As the process reliability and computer design tools developed, so the integration levels, in terms of the number of transistors per IC, have grown almost exponentially with time, as illustrated in Figure 1.1. With each decade of transistor numbers, there came a new term for the level of integration, as summarized below:



<i>Nomenclature</i>	<i>No. of transistors</i>
Small scale integration (SSI)	1–100
Medium scale integration (MSI)	100–1 000
Large scale integration (LSI)	1 000–10 000
Very large scale integration (VLSI)	10 000–100 000
Ultra large scale integration (ULSI)	100 000–1 000 000
Wafer scale integration (WSI)	over 1 000 000

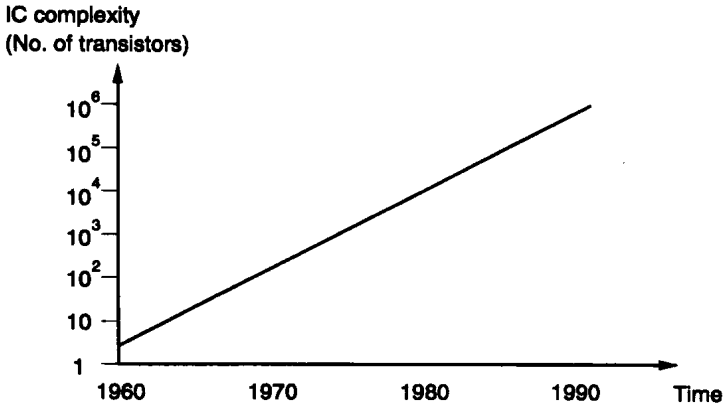


Figure 1.1 Growth in IC complexity with time

Note that technically the term VLSI is applied to circuits with transistor counts between ten thousand and a hundred thousand; but in practice the term has come into common use for virtually any monolithic IC, digital or analogue, and it is not unusual to see it applied to circuits that are MSI in complexity!

## 1.2 The design cycle

The design of a circuit comprising a million plus active devices is a daunting task. The complete design process from specification to IC realization has generally been beyond the scope of a single designer, as the total work load involved has often been of the order of several man-years. Teams of designers working together meant that new products could be completed within a year of real time. As competition for new markets and new products has accelerated in recent years, the complexity and power of the computer aids to design have reduced the work load to the order of man-months, and it is now within the scope of a single (very skilled!) designer to generate a complete IC within a reasonable time. However, to ensure quality of the product the design process must be well specified, with rigorous checks at each stage to ensure, as far as is practical, freedom from errors which would be expensive and time consuming to correct at a later stage of the process. This section briefly