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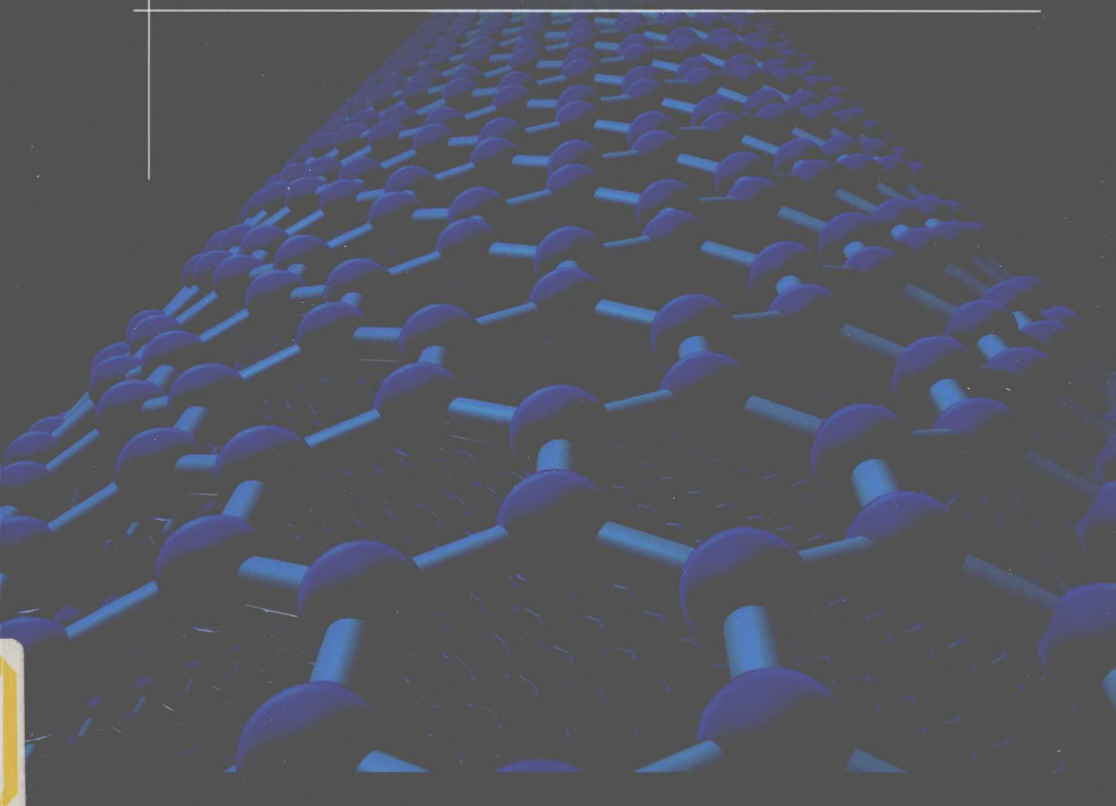
MEMS/MOEMS PACKAGING

CONCEPTS, DESIGNS, MATERIALS, AND PROCESSES



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MEMS/MOEMS Packaging

Concepts, Designs, Materials, and Processes

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CIP Data is on file with the Library of Congress

1 2 3 4 5 6 7 8 9 0 DOC/DOC 0 1 0 9 8 7 6 5

ISBN 0-07-145556-6

The sponsoring editor for this book was Kenneth P. McCombs and the production supervisor was Pamela A. Pelton. It was set in Century Schoolbook by International Typesetting and Composition. The art director for the cover was Handel Low.

Printed and bound by RR Donnelley.

This book is printed on recycled, acid-free paper containing a minimum of 50% recycled, de-inked fiber.

Preface

MEMS may well become a hallmark technology for the 21st century. The capability to sense, analyze, compute and control, all within a single chip, will provide new and powerful products during this decade and far beyond. MEMS deals with the integration of everything from motion, light, sound, molecular detection, radio waves to computation. While sensors are a large and expanding market, MEMS also brings control—electrical, mechanical, optical, fluidic, electromagnetic, and more. Merging of motion, sensing, control and computation within a very compact single system is a major leap in technology. Although there are still challenges ahead, there are no remaining problems without impending solutions. MEMS is the vital enabler where convergence of technology and science will miniaturize and unite mechanics, electronics, optics, and all other vital areas including chemistry, physics, biology, and medicine. Continued technical success is assured at the device level because MEMS is a robust and well-supported member of the huge semiconductor industry. Worldwide electronic giants, innovative start-ups, government laboratories, and hundreds of universities are strongly supporting this most valuable technology group of the 21st century.

Today, MEMS is on a solid, healthy, and accelerating growth curve after many years of hard work with high expectations. Many technology watchers recognized that MEMS was a very important field, but few realized the broad scope and extreme versatility that could be developed. The emerging view of MEMS is that it is the synergistic addition of "mechanics, motion, and light (MOEMS)" to existing electronic semiconductor devices and a focal point for the convergence of almost all of the sciences; every technology can benefit and many will be boosted significantly. Since mechanics, photonics, and electronics are already so intertwined at the macro-level, MEMS is being viewed by the electronics industry as an enhanced electronic-based device platform that can become as pervasive as the computer chip. There are already more than 250 commercial MEMS companies actively working in this field, including well-established companies like Agilent, Analog Devices, Canon, Delphi, Denso, Epson, GE

Infrastructure Sensing, Hewlett Packard, Honeywell, IBM, Intel, Kavilico, Lexmark, Motorola (Freescale), Robert Bosch, ST Microdevices, Texas Instruments, and VTI Technology. Major professional organizations have endeavored to become important MEMS resource centers. Most industrialized countries now have major government programs in MEMS. The U.S. government continues to expand MEMS development and capability primarily through Sandia National Laboratories, especially in areas that are dedicated to defense and national security; MEMS devices are now critical components for defense and security. Other active laboratories include CEA-LETI, Fraunhofer, and IMEC. Nearly every university is doing MEMS research and several are now offering MEMS engineering degrees.

But there are challenges. While much success has been achieved at the device level, packaging has lagged behind. Very little funding has been provided for package development, perhaps because of the erroneous assumption that existing technology would suffice. Most packaging experts feel that MEMS package design and manufacturing represents the greatest challenge ever for their industry. Not only are the newest MEMS devices small and complex, they must often communicate with the outside world by modes beyond just electrical input/output. The exception is motion-sensing devices like accelerometers and gyroscopes that only need electrical connections. Since these sensor chips can be capped at wafer-level, a topic covered in this book, many can be overmolded but with diminished sensitivity due to encapsulant shrinkage and stress. Since these mature MEMS products have been well publicized, many have incorrectly concluded that MEMS packaging is also established. How wrong! A packaging solution for an air bag accelerometer offers no solutions for a BioMEMS system or an air-measuring hazards sensor. Advanced MEMS, and perhaps all MOEMS chips, will require cavity type packaging and cannot generally use the overmolding process employed for most inertial sensors.

The traditional packaging strategy seeks to keep everything away from the device, except electrical power and signal. The most common electronic package, the non-hermetic plastic type, requires encapsulation materials to directly contact the chip. But the mechanical character of MEMS precludes the use of epoxy overmolding and other standard packaging processes. However, this book describes wafer-level protection schemes that may allow modified standard packaging processes to be used, including some for optical-MEMS chips. But when a cavity is essential, the MEMS specialist is left with a very limited choice of package designs, and those that can be used are not cost-effective. The forced use of overly expensive hermetic packages that were designed for military electronics and specialty telecommunications products has been detrimental. While packaging costs for electronics make up only 4 to 5 percent of the total, the MEMS package has been more costly than the device inside. Packaging costs that make up 50 to 80 percent of the product have held back the growth of MEMS by precluding some of the attractive markets that are cost-sensitive. This book offers alternatives.

The goal of this practical book is to help MEMS crafters and technologists step out of the "box" of traditional, but expensive packaging that might otherwise become the "coffin" that buries a great idea. It is absolutely essential that MEMS and MOEMS packaging moves onto a new plateau of innovation with designs specifically for these mechanical and optical devices that are so different from anything that came before. MEMS devices, especially for volume commercial applications, must not be constrained by cost and performance limitations of "off the shelf—but doesn't quite fit" products. This book methodically covers packaging principles, designs, materials, and processes. New concepts, such as the *near-hermetic package* (NHP), are introduced and discussed in detail. Thermoplastic injection molding, ideal for low-cost mass-production of cavity packages, is thoroughly described. Many new packaging ideas are presented that are intended to stimulate new approaches within this field. MEMS packaging innovation will also pave the way for *nanoelectromechanical systems* (NEMS). Nanotechnology is already being applied to MEMS products and these two powerful technologies will move closer together over time. The tools required and being developed for MEMS are the most versatile yet proposed for unconventional devices and can serve as a launch pad for nanotechnology in the future.

Ken Gilleo, Ph.D.

ABOUT THE AUTHOR

Ken Gilleo, Ph.D., is the CEO of ET-Trends, a consulting, packaging design, and IP firm specializing in emerging technologies. The firm's projects include novel materials and packages and processes for MEMS, MOEMS, and optoelectronics. Dr. Gilleo is a member of IEEE, and he is also Vice President of Technical Programs for the Surface Mount Technology Association (SMTA). He has been actively involved in the development of new products for 30 years and is an inventor in circuitry, electronics materials, and packaging. Dr. Gilleo has 30 U.S. patents, and his products have received three R&D 100 Awards. Dr. Gilleo resides in Warwick, Rhode Island.

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Chapter

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Engineering Fundamentals of MEMS and MOEMS Electronic Packaging

The electronic component package that began as a simple glass enclosure for radio vacuum tubes has evolved into a sophisticated system that is now the nucleus of a new era of technology advancement. Packaging is undergoing one more revolution, perhaps even the last, when viewed from several perspectives. Integrated circuits (ICs) continue to grow more complex and to operate at ever-higher speeds while chip dimensions get smaller as the industry perpetually pursues Moore's law, which predicts the doubling of performance every 18 months. The package must accommodate these changes in electronic devices that create an escalating challenge for connecting to printed circuit boards that evolve and advance much more slowly than semiconductors. The package is in the midst of transitioning from chip-scale to exponentially higher density multichip systems. Vertically stacked *three-dimensional* (3D) package designs are finally gaining success and now being used in most of the latest mobile phones. Some feel that 3D stacking is the final revolution in densification because this scheme produces a cubelike, volume-maximized, footprint-minimized package. This may be true for today's silicon-based electronic devices, but many new devices, including those based on Nanotechnology, are on the horizon and others are already here, like *microelectromechanical systems* (MEMS) and *micro-optoelectromechanical systems* (MOEMS).

Today, the myriad of mechanical and optomechanical devices urgently need the right package—one that may not yet exist for many of the chip designs. MEMS devices present the newest and most intriguing set of challenges for packaging developers and manufacturers. This chapter will begin by detailing and discussing the various elements and functions of the electronic package and then move to the task of identifying the unique requirements for *mechanical* chips. We will examine the most important general functions and features of the generic package before moving to the more specialized requirements for MEMS and MOEMS.

1.1 The Package as the Vital Bridge

The package may appear to be just a tiny black plastic box, gray stone-like slab, or a bright metal container that is used to hold the chip, but it is actually a sophisticated system when we carefully examine the tasks that must be accomplished under extreme and varying conditions. The package continues to be the *bridge* between the contrasting industries of semiconductors and *printed circuit boards* (PCBs). But as the chasm between chips and PCBs grows wider, the package designers' mission grows larger. Some package attributes are absolutely essential, others are beneficial, and still others are product-specific that may have no precedent. Essential requirements include providing the electrical interconnect system between the tiny semiconductor and larger scale PCB. Signal routing is essential for some applications like *flip chip* (FC) but not in every case. The package is the physical scale translator that can make the ultrafine chip features compatible with any substrate assembly pad layout. Environmental protection is almost always a requirement, but it is product-specific, and ranges from minimal protection for highly passivated and robust chips to extreme for some MEMS, MOEMS, and *optoelectronic* (OE) devices that are sensitive to almost everything in the surrounding environment. The package can also provide compatibility between chips with metal pads that are typically not solderable and PCBs that commonly employ a solder joint interconnect. And just surviving lead-free solder assembly that now raises the processing temperature by 40°C or more, is heroic. Mechanical shock resistance for the package and its connection to the PCB is often an important newer requirement for portable products like cell phones. The package should also be removable and preferably, reworkable. The finished assembly must often withstand temperature and humidity extremes throughout its long life, which is no small task. Other package attributes include testability, standardization, ease of automatic handling, miniaturization, performance enhancement, and heat management. But MEMS will add considerably more in the way of requirements and some will create a paradox. Figure 1.1 shows the relationship between package elements and the main attributes.

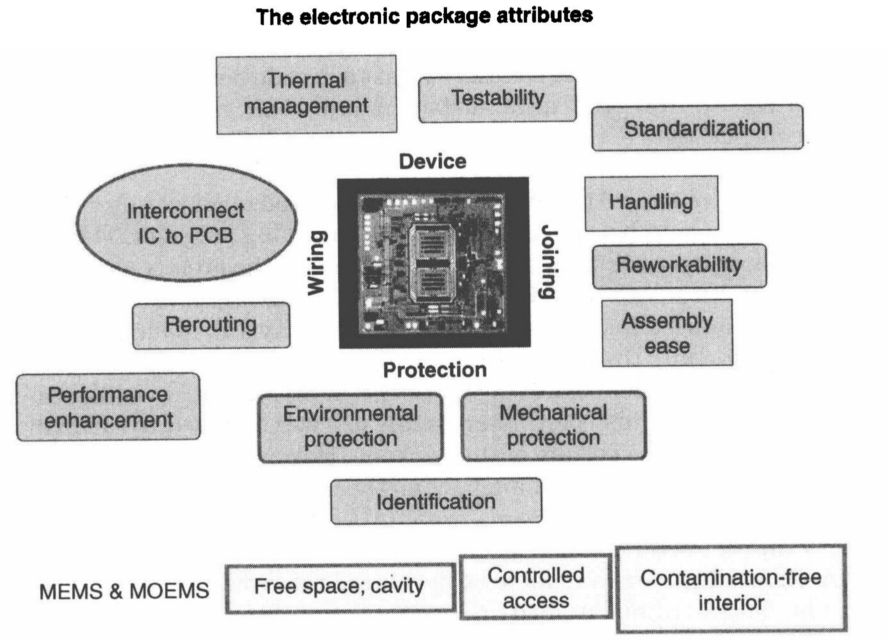

Figure 1.1 The package.

1.2 Packaging Challenges

In some ways, the component packaging industry is dynamic, but it also has enormous inertia that resists changes, especially those that can impact the long-established infrastructure. Design change often seems to run rampant so that too many package styles evolve, each with countless iteration. Even some of the *new* packages based on flexible circuitry materials can be traced back to products from the 1960s. New is old in most cases! Conversely, materials, especially for encapsulation, as well as their processes, have evolved slowly without real fundamental changes. The last important cost-cutting breakthrough for component packaging took place a half-century ago when the nonhermetic plastic package was successfully introduced. The DIP, or *dual in-line package*, became ubiquitous, and feedthrough assembly eventually became the *de facto* standard that still exists. But the DIP and other feedthrough packages eventually lost favor when a multitude of *surface mount technology* (SMT) packages were commercialized throughout the 1980s and the merits of surface mount assembly were confirmed. However, the early SMT designs were relatively simple modifications of the DIP pack. The metal leads could simply be bent outward into a "gull wing" shape that allowed the package to be bonded to metal pads on the surface of the circuit board instead of pushing through holes in the board. Early electronic calculators from Texas Instruments used bent DIPs for surface mounting onto flexible circuits at least a decade before the SMT revolution began. And IBM used surface mount, *ball grid array* (BGA), *chip-scale packages* (CSPs) in the 1960s—decades before they were reinvented. Figure 1.2 shows the DIP.

The 1990s continued to advance SMT as the need to miniaturize while boosting lead count became important for continuing progress. The area array packaging revolution[1] gained momentum as the preferred solution for size reduction with concurrent increase in *input/output* (I/O) (number of package connections). This trend continues today and roadmaps show a continuation into the future. But moving to area array was an obvious solution to the problem of adding more and more leads to a smaller and smaller package. This "perimeter paralysis" was relieved by utilizing the readily available bottom of the package. However, the move to area array required many more changes than the switch from feedthrough to surface mount. The *metal lead frame* (MLF) that had been used for nearly all perimeter packages could not effectively support area interconnection. Chip carriers had to be developed that could serve as a platform for chip bonding but also provide an array of connection points on the bottom surface. This required true circuits with both dielectric and conductors. Although the *pin grid array* (PGA) was available, high-speed assembly demanded a solderable area array concept that led to the introduction of the BGA usually formed by attaching solder balls to the metal lands on the bottom of the package chip carrier. The BGA is becoming increasingly popular even though it is a more complex and costly package than the perimeter *surface mount device* (SMD). However, the BGA continues to evolve, but primarily to reduce cost. "No lead" or leadless versions are now in use like the *quad fine pitch no lead* (QFN) that has only metal pads on the bottom. Ironically, the new QFN-style package is a *land grid array* (LGA) concept that was used before the BGA-making

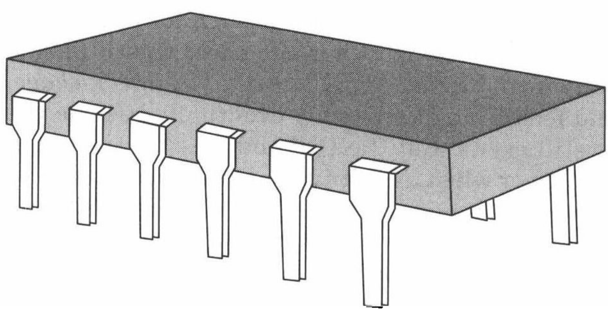

Figure 1.2 Dual in-line package.

progress, a step backwards. While solder bumps aid assembly, they are not necessary since solder paste must be screened onto PCB pads for other components. Solder paste is generally stenciled onto circuit boards using high-speed automated equipment. Figure 1.3 shows a leadframe quad pack SMD and a *plastic ball grid array* (PBGA) type package.

Electronic packaging has become an intensely energetic zone of technical development that is evolving ever faster as 3D stacked designs and *wafer level package* (WLP) processes are being implemented. The WLP is aimed at cost reduction by constructing the package on the semiconductor wafer, but some of the processes can produce unique results that are especially useful for MEMS devices and these concepts will be thoroughly described later. Now back to the issue of materials inertia.

While some of the new package designs are refreshingly novel, materials and the most basic manufacturing processes from past decades remain essentially unchanged. There are a few exceptions, of course, and most are in more specialized areas like flex-based packaging. Epoxies, used for over 50 years to mold plastic packages, are still the standard encapsulant for most of the newest designs even though this material class is plagued with intrinsic problems that are about to get worse. Epoxy, discovered in 1927, is still the "workhorse" polymer for most plastic packages.[2] But this could finally be changing. Thermoset *epoxy molding compounds* (EMCs) were once the obvious choice at a time when the plastic package was first developed. Epoxy resins were the right choice in the 1950s because they could withstand the heat of soldering and were easy to use. Epoxies are thermosets that once polymerized, don't remelt; they are permanently *set* as their name implies. Cross-links (chemical bonds) between polymer chains create a permanent 3D shape that cannot melt but can thermally decompose. The other broad class of polymers, remeltable thermoplastics, was not yet ready for high-temperature use in the 1950s and could not be a serious contender. Although epoxies have been favored by formulators for versatility and balanced properties, they are not considered to have any specific properties that are exceptional. But epoxies became part of the packaging industry's infrastructure, for better or for worse. Epoxies, like FR4, are also part of the printed circuit board infrastructure, but the industry is working

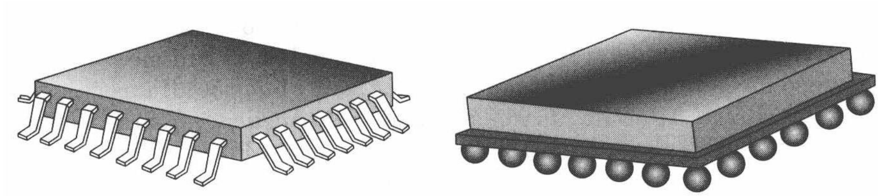

Figure 1.3 SMT quad pack and PBGA.

hard on alternative resin systems as lead-free soldering and halogen-free initiatives turn up the heat. And finally, the standard epoxy-transfer molding process is poorly suited for producing cavity-style packages that are needed for many types of MEMS devices.

Today, supply chain dynamics and aggressive outsourcing strategies are opening up a new and larger resource infrastructure that can offer newer materials and processes that have been successfully used by hundreds of industries. It's time to think outside the metal, ceramic, and epoxy boxes since the first two are priced higher and epoxy resins property and processing limitations are intrinsic. Pending regulations like *restriction of hazardous substances* (RoHS) in electrical and electronic equipment have restricted lead and are now aimed at banning most, and perhaps all, bromine-containing epoxies. Most EMCs still contain halogen, bromine compounds in particular, that are destined to be regulated into extinction just like lead in solder. Replacement of bromine with dubious choices like phosphorus, as a flame retardant, will only add more uncertainties, since phosphorus,—an element found in several *nerve gases*—will be in trouble sooner or later. A flame retardant *additive* is typically performance *subtractive*. But what if there were suitable high-temperature packaging plastics that were intrinsically flame retardant? Fortunately, there are many. One focus will be to identify such polymers with intrinsic low flammability, especially if they have other superior properties that are important for packaging.

A *perfect storm of change* has drifted across the packaging landscape that can help propel newer and better materials into the mainstream. We will compare metal, ceramic, thermoset, and thermoplastic materials for packaging to determine where each plays the best role. Thermoplastics are cheaper, environmentally acceptable, and boast near-hermetic properties superior to nonhermetic epoxies, but their performance is not as good as metals and ceramics. Thermoplastic properties are controlled and verified by the resin manufacturer who carries out the polymerization reactions. Thermosets can vary from run to run and the end user influences the final properties by carrying out *in situ* polymerization. The packager becomes the *chemist* (willing or not) and changes in the bake cycle alter cured properties like *glass transition* (Tg). More recently, bad EMC was not discovered until it was used to make millions of packages, making the final cost substantial. This situation cannot really occur with thermosets since final properties are checked and known before material is shipped. We will determine how well thermoplastics can meet a critical need for lower cost cavity packages for some, but not all mechanical devices. MEMS, MOEMS, as well as some *radio frequency* (RF) and optoelectronic devices, have created a growing market for low-cost cavity free-space enclosures that can be satisfied with new materials including thermoplastics, and fresh designs. Perhaps we will see a quiet packaging