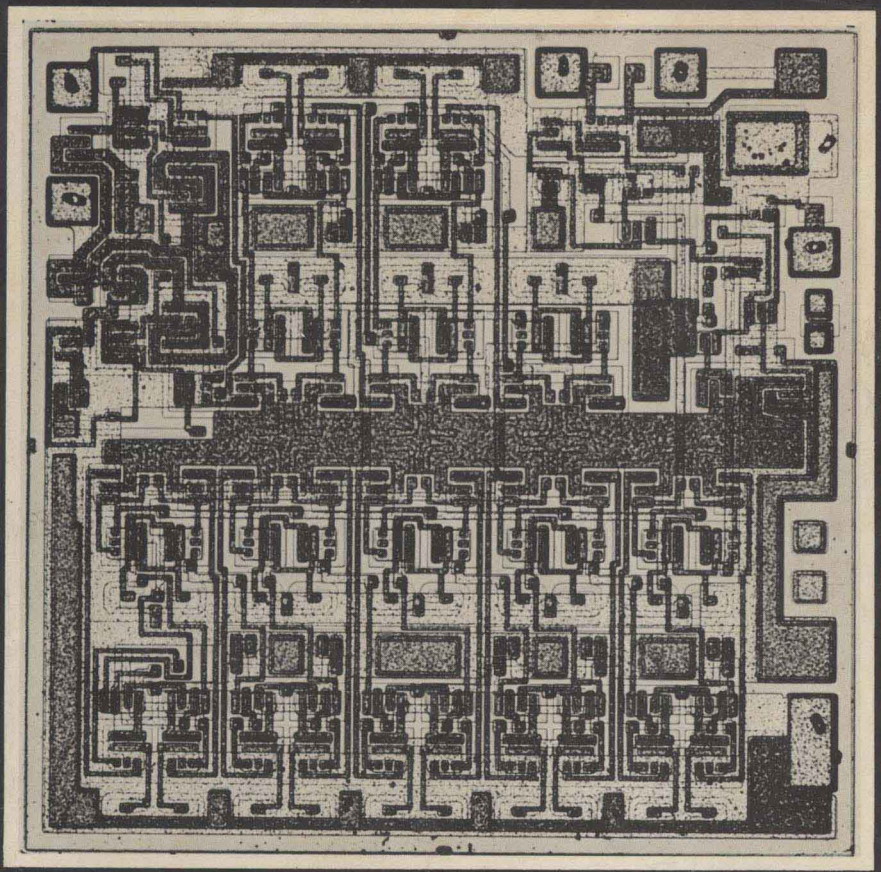
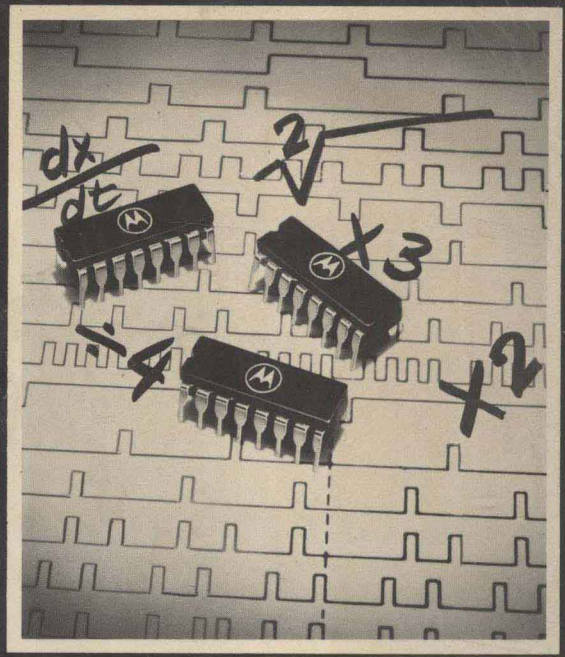
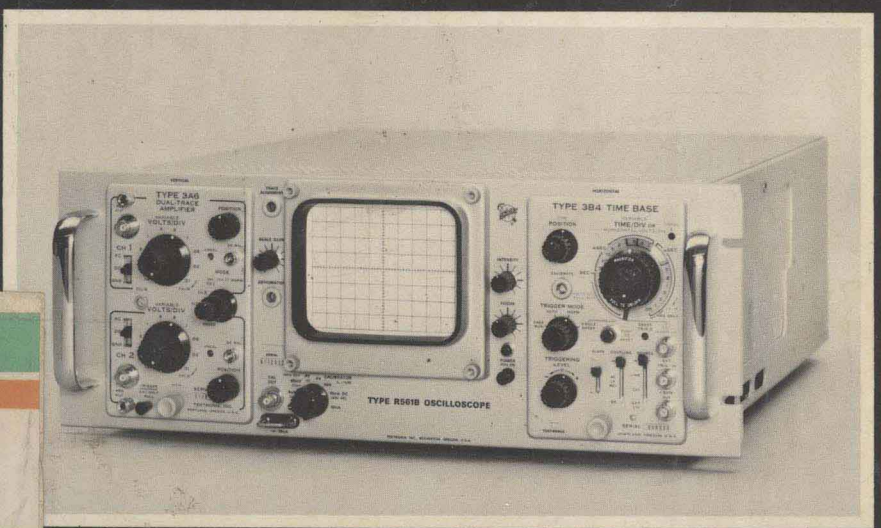
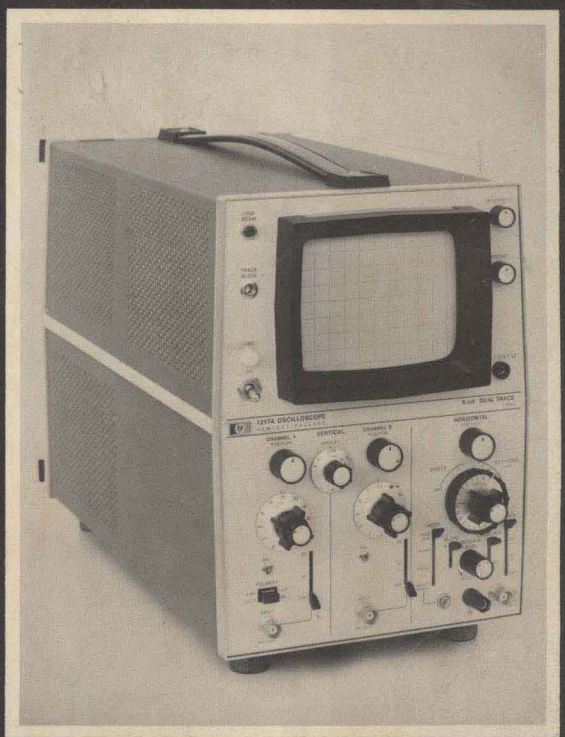
Digital Theory and Experimentation Using Integrated Circuits

MORRIS E. LEVINE









DIGITAL THEORY AND EXPERIMENTATION USING INTEGRATED CIRCUITS

Morris E. Levine

Associate Professor
Staten Island Community College
City University of New York

PRENTICE-HALL, INC., ENGLEWOOD CLIFFS, NEW JERSEY

Library of Congress Cataloging in Publication Data

Levine, Morris E

Digital theory and experimentation using integrated circuits.

(Prentice-Hall series in electronic technology)
Bibliography: p.

1. Digital electronics–Laboratory manuals.
2. Integrated circuits. I. Title.

TK7868.D5L48 621.381'73 73-12863
ISBN 0-13-212258-8

Printed in the United States of America

10 9 8

PRENTICE-HALL INTERNATIONAL, INC., London
PRENTICE-HALL OF AUSTRALIA, PTY. LTD., Sydney
PRENTICE-HALL OF CANADA, LTD., Toronto
PRENTICE-HALL OF INDIA PRIVATE LIMITED, New Delhi
PRENTICE-HALL OF JAPAN, INC., Tokyo

DIGITAL THEORY AND EXPERIMENTATION USING INTEGRATED CIRCUITS

To
Pearl, Estelle, and Carl

PREFACE

This laboratory manual has been developed to provide laboratory training and experience in digital electronics using integrated circuits in the laboratory environment of the industrial electronics laboratory. As in the industrial electronics laboratory all of the measurements (with very minor exceptions) are made using the cathode ray oscilloscope. This manual therefore serves two purposes. Besides providing the digital techniques experience, it also provides intensive and thorough training in the use of the CRO as a universal tool for the measurement and analysis of digital circuits.

There are five primary techniques used for the analysis of digital circuits and theory. They are:

A. Voltage levels
B. Logic levels; 1 or 0, T or F, H or L, ON or OFF
C. Logic diagrams
D. Mapping methods
E. Sequential operations. The CRO is used to demonstrate and perform the analysis.

All five methods are integrated to advance understanding of digital principles.

Sixteen experiments are included in this manual to provide thorough coverage of digital principles. They begin with a series of experiments on the principles of logic. These are followed with experiments on arithmetic operations. Several experiments cover the material on counters, counter techniques, the binary number system, decoding-encoding, memory techniques, pulse generation and pulse shaping/IC Schmitt Trigger. The operational amplifier has become of great importance in digital techniques. Two experiments develop the principles and applications of the OP-AMP in D/A and A/D conversion.

Experiments follow a uniform format and are divided into three sections:

1. The experimental laboratory data. Data tables are marked with the letter E.
2. Required results. The experimental data is analyzed and converted to general logic levels. Corresponding tables are marked R.
3. Discussion. In this section the student is required to answer a series of questions which are based upon the experimental results and which integrate the data and digital theory. Corresponding tables are marked with the letter D.

Many types of IC logic families have been developed. Any one family could be used to provide a complete set of experiments. This manual provides experience with TTL and the Operational Amplifier.

Whenever possible, an experiment starts with the basic building of a logic operation. Once the principle has been developed, it is replaced by an MSI unit. This provides the student with an

understanding of the logic and gives him a feeling for the trend in integrated circuits towards MSI and LSI and, in addition, simplifies the wiring of more complex circuits.

Discrete active components are used briefly in three experiments. Diodes are used in experiments 1, 11 and 12, and transistors in experiment 11 to develop some of the principles of the astable multivibrator.

All of the ICs used in this manual are in the 14 pin or 16 pin dual-in-line (DIP) construction. In appendix G are the constructional details of a laboratory IC socket and switch bank arrangement which readily lends itself to the wiring and breadboarding needs of a laboratory and to squad organization and participation. The IC socket is mounted on 1/8" aluminum channel and the pins are connected to universal 5-way binding posts. This permits the use of stackable banana plug leads for interconnection.

All of the experiments can be performed with 6 IC sockets and 2 switch banks. The cost of the material for the sockets and switch banks is approximately $100.00. At the present writing the cost of the ICs needed to perform all the experiments is less than $25.00. A complete set-up can be provided at a basic cost of less than $125.00.

I wish to express my appreciation to Richard Brown and John Gappa, laboratory technicians at the Staten Island Community College, for their suggestions and assistance, particularly with respect to the socket and switch bank construction, to the students at the SICC for their help and suggestions, to Dr. Irving Kosow, particularly with respect to the format, and to Mrs. Jean Johnson for her excellent typing and proofreading of the manuscript.

TO THE INSTRUCTOR

The ICs used in the experiments are all in the dual in-line 14 pin or 16 pin configuration. A convenient method of storage is in the plastic shipping container used by the IC manufacturers for shipping production quantities of ICs to the users.

The ICs used in the experiments (as is true for semiconductors in general) do not have a great over voltage tolerance before their dissipation is exceeded. The procedure suggested in appendix A, of calibrating the CRO and checking the power supply voltage against it, if carefully followed at the beginning of each experiment will protect the ICs against over voltage and at the same time provide some additional CRO experience.

Voltage measurements should be made to within 0.1 volt.

The ICs used have short internal connections and high F_T. If allowed to remain in the active region there is a great possibility of parasitic oscillation. This can occur in obtaining the transfer characteristics in experiment four. The by-pass capacitor at the gate input is a parasitic oscillation suppressor. For the same reason a pulse generator should have a short rise and fall time especially when toggle flip-flops are being used, to prevent the build up of oscillations and a resultant false count. Should there be any such suspicion, the Schmitt Trigger of experiment 12 can be used to shorten the rise and fall times. Schmitt Trigger IC types 7413 or 7414 can be used to reduce rise and fall times of pulse generators.

If the pulse generator is square wave centered around zero voltage it cannot be used with the ICs since they will not accept negative going gate input voltages. A small signal diode can be used across the pulse generator to clip the negative going portion of the wave.

While the wiring in some of the experiments is somewhat complex, a wiring layout as close as possible to the circuit drawing will help in trouble shooting.

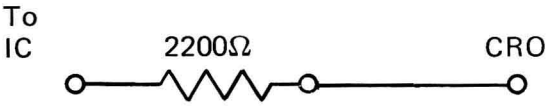
Students should be encouraged to write the values of the logic variables at each point of the logic diagrams in the manual.

If a dual beam or dual trace CRO is available, the bistable action of experiment 8 can be best demonstrated if the beams are displaced horizontally from each other or one beam is operated with a lower brightness.

Flip-Flop Output Measurements – Precaution

A long lead from a bistable, or counter, or intermediate outputs of a counter, or monostable multivibrator may cause undesired loading and prevent the bistable from toggling or dividing properly, or the monostable from functioning properly. If such difficulties are encountered, a composition 2200Ω decoupling resistor at the IC end of the lead can eliminate the loading prob-

lems. The lead length from the 2200Ω resistor should be kept reasonably short. This decoupling may be needed both for the CRO vertical input and for external triggering.



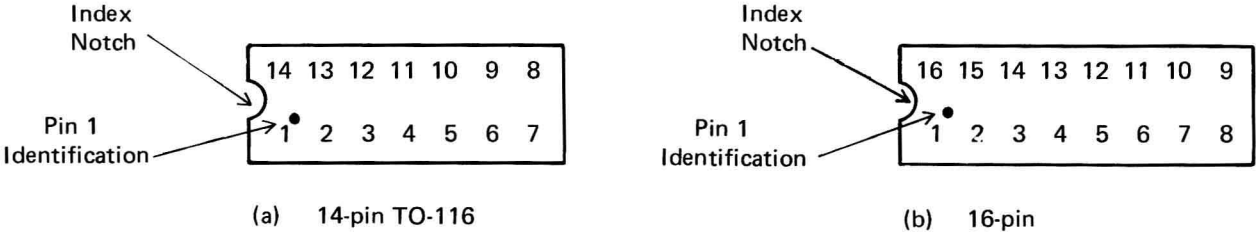
Integrated Circuit Types and Experiments in Which They Are Used

	741C	7400	7402	7403	7404	7405	7410	7420	7432	7441A	7472	7476	7481A/MC4005P	7486	7490
1. Basic Logic Functions		1	1		1			1	1						
2. Boolean Algebra		1			1	1			1						
3. DeMorgan's Theorem		1	1		1	1		1							
4. TTL NAND/NOR Gates		1		1											
5. Exclusive OR		1	1		1			1						1	
6. Full Adder/Full Subtractor		1	1		1		1	1						1	
7. Bistable		1	1							1					
8. Binary Counters		1						1		3					
9. Divide by N Counters										4					1
10. Shift Registers		1								1	3				
11. Pulse Forming		1		1											
12. Pulse Shaping/Schmitt Trigger				1											
13. Decoding/Encoding					1			2		1		1			1
14. Random Access Memories (RAM)		2		1									1		
15. Operational Amplifier	2														
16. D/A and A/D Conversion	2				1	1									1

IC PIN CONNECTIONS AND IDENTIFICATION

The ICs used in this manual are made in the dual in-line case. The IC pin terminals progress in a counterclockwise direction as seen from the top side away from the pins. The ICs are in either 14-pin TO-116 (EIA designation) or 16-pin configurations. In these ICs pin 1 is located by an identifying symbol, or the location of pins 1 and 14 (14 pin IC) or pins 1 and 16 (16 pin IC) are identified by an index notch at the end of the case where these pins are located. This is illustrated in the figure below.

Top View (away from pins)



Dual in-line pin location.

CONTENTS

PREFACE ix

TO THE INSTRUCTOR xi

Experiment 1
BASIC LOGIC FUNCTIONS 1

Experiment 2
BOOLEAN ALGEBRA AND SIMPLIFICATION OF LOGIC EQUATIONS 11

Experiment 3
DE MORGAN'S THEOREM 23

Experiment 4
TTL NAND/NOR GATES—DEFINITIONS AND OPERATION 31

Experiment 5
THE "EXCLUSIVE OR" AND ITS APPLICATIONS 47

Experiment 6
FULL ADDER/FULL SUBTRACTOR 59

Experiment 7
BISTABLE OR FLIP-FLOP (FF) 71

Experiment 8
BINARY COUNTERS/THE BINARY NUMBER SYSTEM 95

Experiment 9
DIVIDE-BY-N COUNTERS; DECADE COUNTERS 109

Experiment 10
SHIFT REGISTERS AND RING COUNTERS 125

Experiment 11
PULSE FORMING 141

Experiment 12
PULSE SHAPING/SCHMITT TRIGGER 151

Experiment 13
DECODING-ENCODING 159

Experiment 14
RANDOM ACCESS (RAM)—SCRATCH PAD MEMORIES 171

Experiment 15
THE OPERATIONAL AMPLIFIER 181

Experiment 16
DIGITAL-TO-ANALOG (D/A) AND ANALOG-TO-DIGITAL (A/D) CONVERSION 195

Appendix A
CATHODE RAY OSCILLOSCOPE (CRO)* 205

Appendix B
LOGIC SYMBOLS 207

Appendix C
THE "UNIT LOAD" CONCEPT 209

Appendix D
IC LOGIC DIAGRAMS AND PIN CONNECTIONS 211

Appendix E
GLOSSARY OF LOGIC AND INTEGRATED CIRCUIT TERMINOLOGY 217

Appendix F
REFERENCES 223

Appendix G
IC SOCKET, SWITCH BANK, AND EQUIPMENT 225

Experiment 1

BASIC LOGIC FUNCTIONS

OBJECT

(a) To study the basic logic functions AND, OR, INVERT, NAND, NOR.
(b) To study the representation of these functions by truth tables, logic diagrams, and Boolean algebra.

INTRODUCTORY THEORY

In electronic logic circuits inputs and outputs occur as voltage levels. These inputs and outputs are dual valued or dual leveled. To provide a common basis for comparison it has become usual to represent the two levels symbolically as 1 or 0. In one circuit the 1 might be +20 volts and the 0 might be −10 volts. In some other circuit the 1 might be +15 volts and the 0 might be +1 volt. Despite the difference in voltage levels, a basic operation will be the same using either pair of voltages.

AND: A multi-input circuit in which the output is a 1 only if all inputs are 1.

OR: A multi-input circuit in which the output is a 1 when any input is a 1.

INVERT: The output is 0 when the input is 1, and the output is 1 when the input is 0.

NAND: AND followed by INVERT.

NOR: OR followed by INVERT.

Truth table: Representation of the output logic levels of a logic circuit for every possible combination of levels of the inputs. This is best done by means of a systematic tabulation.

EQUIPMENT REQUIRED

CRO, dc coupled and calibrated.
dc power supply, +5 volts at 50 mA,
2 silicon small signal diodes, 1N457 or equivalent.
1 2.2 kΩ ± 10% composition resistor.
IC type 7400 quad 2-input NAND gate.
IC type 7402 quad 2 -input NOR gate.
IC type 7404 hex inverter.
IC type 7420 dual 4-input NAND gate.
IC type 7432 quad 2-input OR gate.
Switch bank, five switches per bank.

IC Manufacturers' Part Numbers.

Type	*Motorola*	*Fairchild*	*Texas Instruments*	*National Semiconductor*
7400	MC7400P MC7400L	7400PC 7400DC	SN7400N SN7400J	DM7400N
7402	MC7402P MC7402L	7402PC 7402DC	SN7402N SN7402J	DM7402N
7404	MC7404P MC7404L	7404PC 7404DC	SN7404N SN7404J	DM7404N
7420	MC7420P MC7420L	7420PC 7420DC	SN7420P SN7420J	DM7420N
7432		7432PC 7432DC	SN7432P SN7432P	DM7432N

IC PIN CONNECTIONS

Each of these ICs are in a 14-pin dual in-line case. The base pins progress in a counter-clockwise direction as seen from the side away from the pins, as shown in figure 1-1. Pin 1 is located by an identifying symbol, or the location of pins 1 and 14 are identified by an index notch at the end of the case where pins 1 and 14 are located.

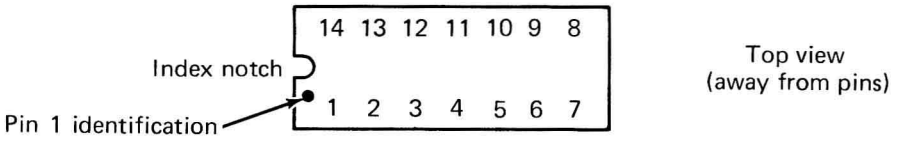


Fig. 1-1. IC pin location,
14-pin dual in-line (TO-116) case.

PRELIMINARY PRECAUTIONS

The ICs used in this experiment are fragile and have a small voltage overload margin. It is extremely important that the exact required voltage be applied. The power supply voltage should be the last connection made. Before connections to the power supply are made, its voltage should be checked both against its own voltmeter and against the calibrated CRO.

All measurements in this experiment are made with a calibrated CRO. *Before making any measurements, calibrate the CRO* (see Appendix A). After the CRO is calibrated, use it to check the power supply voltage. If a disagreement occurs between the power supply voltmeter reading and the CRO measurement, call the instructor.

EXPERIMENTAL PROCEDURE

For each part of the experiment apply the indicated voltage and make voltage measurements at the points indicated to complete the tables. Use the CRO to measure the voltage. Use a sensitivity of 1 volt/div and make measurements to within 0.1 volt.

1. AND Function with Diodes

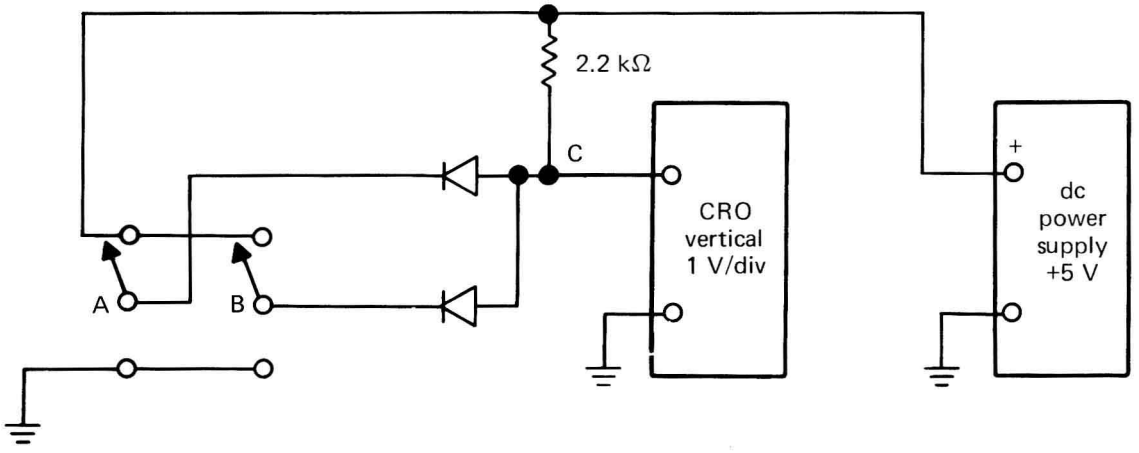


Fig. 1-2. AND gate.

Table 1-1E. Diode AND gate.

A	*B*	*C*
0	0	
0	+5	
+5	0	
+5	+5	

2. OR Function with Diodes

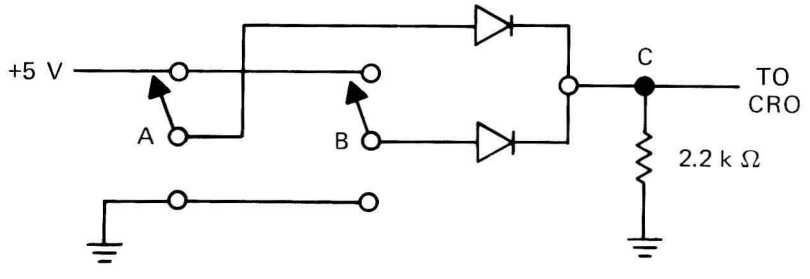


Fig. 1-3. OR gate.

Table 1-2E. Diode OR gate.

A	*B*	*C*
0	0	
0	+5	
+5	0	
+5	+5	

3. IC OR gate

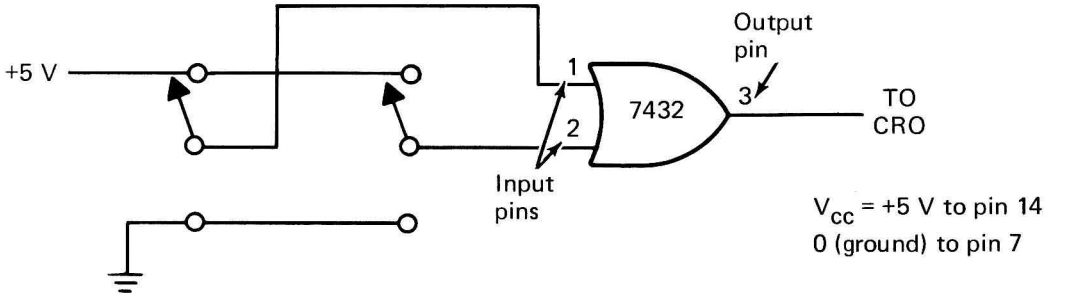


Fig. 1-4. IC OR gate.

Note: The IC type 7432 has four 2-input OR gates within its package. Only one of these gates is used in this experiment. It is the gate whose input pins are pins 1 and 2 and whose output pin is pin 3. See Appendix D for complete logic diagram and pin connections.

Table 1-3E. IC OR gate.

Pin 1	*Pin 2*	*Pin 3*
0	0	
0	+5	
+5	0	
+5	+5	

4. INVERT

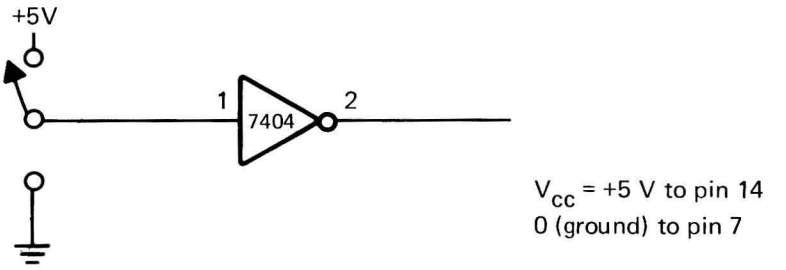


Fig. 1-5. IC inverter.

Table 1-4E. INVERT.

Pin 1	*Pin 2*
0	
+5	

5. OR + INVERT = NOR

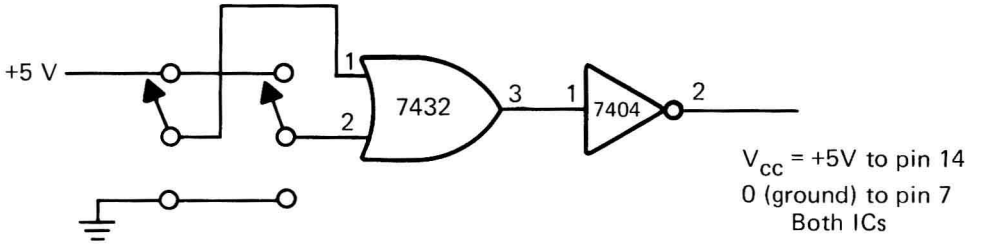


Fig. 1-6. OR + INVERT.

Table 1-5E.

7432		*7404*
Pin 1	*Pin 2*	*Pin 2*
0	0	
0	+5	
+5	0	
+5	+5	

6. NOR

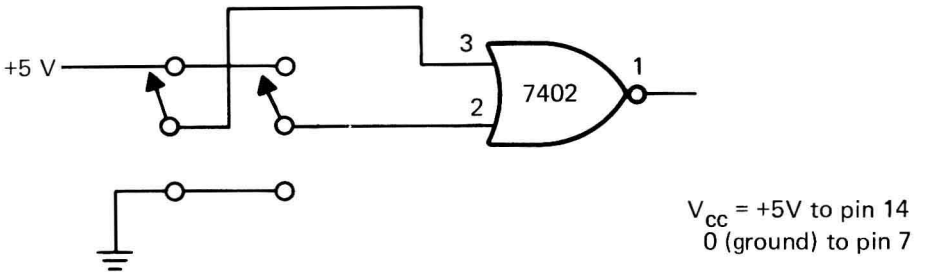


Fig. 1-7. NOR.

Table 1-6E.

Pin 3	*Pin 2*	*Pin 1*
0	0	
0	+5	
+5	0	
+5	+5	

7. 2-INPUT NAND

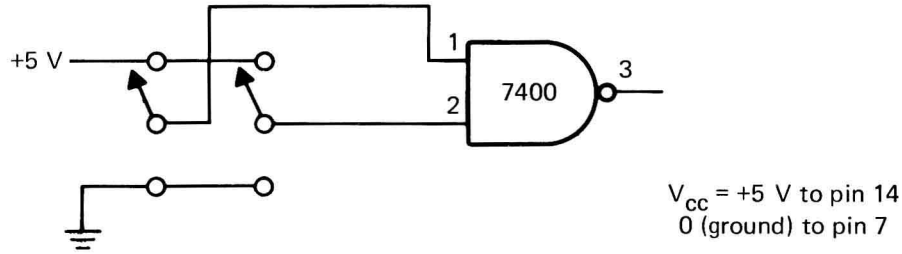


Fig. 1-8. NAND.

Table 1-7E.

Pin 1	*Pin 2*	*Pin 3*
0	0	
0	+5	
+5	0	
+5	+5	