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Annual Simulation Symposium

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Annual Simulation Symposium

PREFACE

The Annual Simulation Symposium is a non-profit corporation formed to provide a forum for the interchange of information related to digital computer simulation. Its objectives are:

- to provide a continuation of the forum for the exchange of working experiences in the field of digital computer simulation, to
- permit an opportunity to survey the state-of-the-art across a broad range of applications, to
- demonstrate the widest possible range of simulation languages, with their strengths for individual problems, and to
- furnish an opportunity for comprehensive understanding of technique through organized question and answer periods and personal contact. It also aims to
- provide potential users of simulation with first-hand exposure to methods, to
- display for library type perusal, the range of literature available in the field, to
- maintain objectivity to the art of simulation, through a non-commercial meeting without obligation to any specific language or hardware, and to,
- underwrite, through grants, the advancement of the art of simulation.

Membership is provided as a result of registration at the Annual Symposium. A Board of Directors is elected by the membership, one Director per year for a three year term.

The Symposium is indebted to those corporations and universities whose support, through their representatives, make this totally independent organization capable of serving the Art of Simulation. This year particular recognition is afforded to those organizations whose members served in offices ond on committees as shown.

The Annual Simulation Symposium is sponsored by the IEEE Computer Society, the Association for Comuting Machinery, the Society for Mathematics and Computers in Simulation.

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PERFORMANCE EVALUATION OF THE DISCRETE EVENT SIMULATION COMPUTER DESC

Meir Barel
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Abstract. The Discrete Event Simulation Computer (DESC) reported here improves simulation performance through an exploitation of parallelism inherent in simulation, with regard to list processing, random number generation, statistical analysis and program control. We have chosen SIMULA as the frame language concept. For performance evaluation a 9 stage queueing network model has been used as benchmark model. During the run time of the simulation program of this model the performance of the DESC was measured via a hardware/software monitor. With these data a queueing model of the DESC was designed, which has been implemented as a simulation program on the DESC. Changing parameters and adding several more processors to the simulation model of the DESC gave us an accurate picture of the DESC's performance under different conditions.

1. INTRODUCTION

Simulation programs often are very complex and require long and expensive run-times on today's general purpose computers in order to obtain sufficiently accurate results /BRAY 82/. Analysis of simulation methods exhibits a high degree of parallelism inherent in simulation. This parallelism can be exploited by means of a special multiprocessor architecture which may reduce run-times by concurrently carrying out the simulation on several processors. Distributed simulation on a multiprocessor architecture has been intensively studied in recent years /PEAC 79, CHAN 81, COMP 84/.

One approach to the problem of distributed simulation is to decompose the simulated system into components, and to simulate these components in a distributed manner over a network of processors. In this approach the aspect of synchronization forms the key problem. Another approach for distributed simula-

tion, which we adapted, is to recognize parallelism in existing sequential programs and then to reconstruct these programs to operate on multiple dedicated processors.

2. SYSTEM DESCRIPTION /BARE 83/

Almost every discrete event simulation program obeys the same skeleton structure:

- List processing (especially event list)
- Random number generation
- Statistical analysis
- Program control

A general approach to distributed simulation can be successfully achieved by distributing the program elements mentioned above into different processors. The primary advantage of this approach is the applicability of it to a large number of simulation packages, such as SIMULA, SIMSCRIPT II.5 and GPSS.

Figure 1 illustrates the blockdiagram of the DESC. The DESC can be viewed as a distributed computing system, matched to the afore mentioned simulation subtasks. Two communication schemes are implemented in the DESC: A Programming-Bus which is only active during the "load program" phase, and a dedicated network, of FIFO-buffered channels, through which data, control and synchronization instructions are transmitted during the simulation. This structure is flexible since the task assignment to individual processing elements is performed by software. It allows growth along any important path desired.

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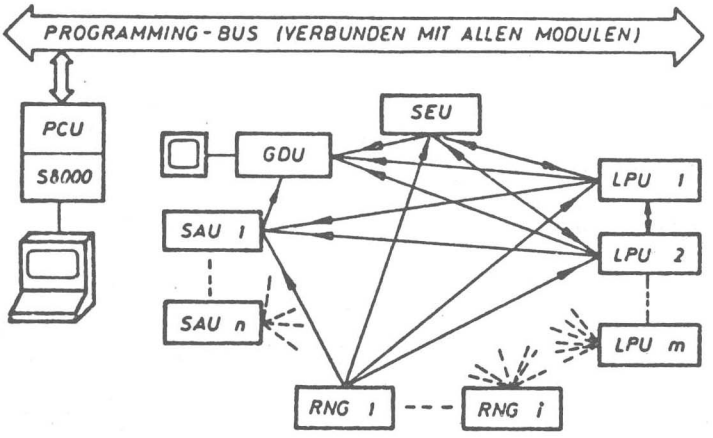

PCU = PROGRAMMING AND CONTROL UNIT
SAU = SIMULATION ANALYSIS UNIT
LPU = LIST PROCESSING UNIT
SEU = SIMULATION EXECUTION UNIT
RNG = RANDOM NUMBER GENERATOR
GDU = GRAPHIC DISPLAY UNIT

Figure 1. DESC's Blockdiagram

2.1 SIMULATION EXECUTION UNIT (SEU)

The distributed simulation concept we chose demands a simulation execution unit to guide the simulation according to the user program. The SEU is connected with each LPU by data channels through which program instructions are transmitted to the LPU's and results from conditional instructions are received by the SEU. Since most of the SEU instructions to the LPU's may result in the spanning of several new processes in the LPU's, RNG, SAU's and GDU (see Fig.1), a distributed program execution is naturally being achieved. The SEU is a 16-bit general purpose computer with Zilog Z8001 microprocessor which operates at a clock frequency of 10 MHZ. The SEU does not process data (32-bit) but instructions (16-bit).

2.2 LIST PROCESSOR UNIT (LPU)

Since many simulation programs especially queueing network models are mainly list processing programs, it is apparent that a distributed list processing concept is essential for a distributed simulation. The list processor which we developed /BARE 83a/ is a special 32-bit microprogrammed pipelined processor implemented in Bit-Slice-technology, according to the co-processor concept. The

architecture 1) is optimized for the execution of list and arithmetic operations, and 2) supports distributed list processing on several list processors. In order to accomodate a wide range of list applications a comprehensive basic instructions set has been implemented which allows the execution of many desired list operations, e.g. complex searching and sorting algorithms. The list processor executes about 0.5 million list operations per second (e.g. insert/remove an element from a list) at a clock frequency of 6 MHz.

2.3 RANDOM NUMBER GENERATOR

Any simulation that contains stochastic behavior necessarily needs programmable procedures for sampling from specified probability distributions. These procedures share a common characteristic, they are all being drawn from the uniform distribution on the unit interval. We developed a new uniform random number generator, to produce the Tausworthe sequence with a generation time independent of the number of bits per word /BARE 83b/. The sequence is available, in TTL-technology, at a speed of more than f = 20 MHz (t=50 ns). The uniform random number generator drives a 32-bit microprogrammed pipeline processor which can generate random numbers of any desired distribution. The random order of the random number generation makes the I/O-structure of the RNG units extremely simple; it enables us to use a FIFO structured memory. Due to this a single memory transaction is sufficient (200 ns) in order to fetch a new random number.

2.4 STATISTICAL ANALYSIS UNIT (SAU)

The statistical algorithms generally implemented in simulation programs demands often a larger program code than the simulation program itself. Many statistical programs take a snapshot of the model in prespecified locations from which they sequentially compute the entire statistics of the simulation. The basic idea of the method presented here is to transfer the data sequence obtained in the snapshots asynchronously to a high speed arithmetic processors. Thus the statistical analysis is carried out concurrently to the simulation program and

the simulation run time is entirely independent of the statistical algorithm implemented. The SAU is build as a 32-bit microprogrammed pipeline processor with harvard architecture having separate program and data memories. The statistical analysis programs can be implemented in microcode, thus improving the statistical computation speed. For further increase of simulation speed the DESC architecture allows the parallel operation of several identical SDU's.

2.5 GRAPHIC DISPLAY UNIT (GDU)

An on-line graphic model description (e.g. structure of queueing network) and on-line representation of statistical results enables the user to observe and judge the model behavior during the simulation run time. The implementation of data channels between several processors and the GDU (see Fig.1), allows multiple processors to send graphical and numerical information to the GDU when they are idle with respect to simulation operation. Thus the description of on-line model behavior is being processed concurrently to the simulation program.

The GDU is also being used to display debugging information during the program development phase. It receives current information such as the event list contents, simulation clock time, queue length etc., and displays this information on a graphic screen, thereby enabling the user to observe whether the program will simulate the model correctly.

Since simulation programs are generally very complex, program input by graphic means is a desired feature. We are working currently on a graphic package which allows the user to draw his model on the graphic screen using a "mouse" and a given menu of model elements on the screen. The model is then being translated into machine code and executed on the DESC.

2.6 PROGRAMMING AND CONTROL UNIT (PCU)

The programming and control unit serves as a system manager of the DESC. This front-end general purpose computer S8000 (ZILOG) with UNIX operating system provides the following:

- Programming facilities to the user of the DESC;
- Compilation of simulation programs;
- Archival storage;
- Link to other computers;
- Maintenance and development tools.

2.7 SOFTWARE STRUCTURE

The modelling concept we have chosen is called process interaction approach /FISH 78/ and is used in the simulation languages SIMULA, GPSS and SIMSSCRIPT II.5. In this modelling concept each entity of a system is modeled by a process which moves through the system and consequentially through time.

The key data structure of discrete event simultion is the event list. In process interaction approach the elements of the event list are the different processes, ordered in increasing order of the expected time of occurence. The event list and all other lists of a simulation program (e.g. queues) are accomodated in the list processor. A special "process" instruction set which is implemented in the LPU includes instructions such as: new process, activate process, passivate process, hold process etc. and allows a simple and structured manipulation of the above mentioned processes.

The SEU contains the coordination instructions consisting mainly of list or process instructions which are passed to the LPU. The SEU may send a sequence of instructions to the LPU (into the FIFO-buffer) which are being executed in a FIFO discipline. If a response is expected the SEU can return after a while to receive it, executing other instructions not depending on the results, in the meantime. The LPU are operating autonom and may request random numbers from the RNG or send sequences to the SAU or GDU as desired.

Upon being initialized, the RNG is programmed to generate random numbers that obey different distributions and to load them into specific FIFO-buffers also to the LPU. The SAU and the GDU expect in their FIFO-buffers an input sequence which they process according to a given program. Thus, during the simula-

tion run-time intertask communication is well defined and very little synchronization, if at all, is needed.

We have chosen as a frame language concept a programming language similar to SIMULA. It was possible to implement a wide class of the simulation instructions of SIMULA.

3. PERFORMANCE EVALUATION

Performance modeling is one of the key methods in the design, development, configuration, tuning and capacity planning of a computer system. Once a particular computer system has been built and is running, the performance of the system can be evaluated via measurements, using hardware and/or software monitors, either in a user environment or under controlled benchmark conditions.

For the performance evaluation DESC is described by an appropriate queueing network model. In order to determine the parameter of this DESC model we have chosen a benchmark model represented by a 9 stage queueing network, introduced by Kuehn /KUHN 79/ as depicted in Fig.2.

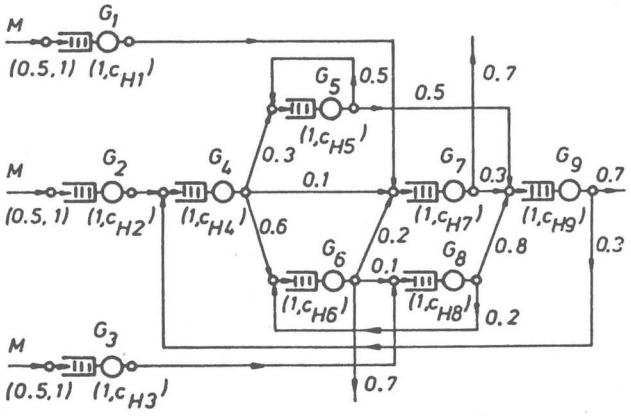

Figure 2. Queueing network model used as a benchmark model for the performance evaluation of the DESC.

The benchmark model was simulated on the DESC and analyzed with respect to the mean normalized total flow time and the mean flow time of the interior sta-

tion number 4. The arrival and service processes are neg. exponential processes with λ_{oi} = 0.5, i = 1,2,3 and μ_i = 1, i = 1,...,9m C_{Hi} = 1, i = 1,2,...,9 respectively.

3.1 PERFORMANCE MEASUREMENTS

The performance measurements of the DESC where taken during the simulation of the benchmark model by means of a hardware and software monitor being provided by the simulator ZUSI/LE. The simulation run time of the benchmark model on the DESC has been 1175 for 100.000 events. The DESC configuration during the measurements is illustrated in Fig.3.

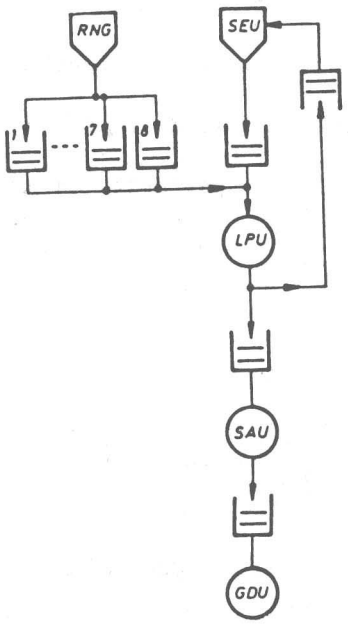

Figure 3. DESC configuration during the performance measurements.

The measurements results are as follow /BARE 83/.

3.1.1 The SEU is inactive just during the time when it is waiting for results from the LPU. The SEU utilization factor is 72% and the mean active time is 32 µs. The SEU process can be described by an exponential process with $\bar{T}$ = 32 µs.

3.1.2 The LPU receives 2.700000 list instructions from the SEU during the simula-

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