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General Chairman's Message

Welcome to San Francisco and the Cathedral Hill Hotel for the 36th Annual IEEE International Computer Conference, COMPCON Spring '91. The nature of COMPCON, this year's only broad-based general computer conference sponsored by the IEEE Computer Society, demands a good balance between depth and breadth in coverage of computer-related topics. We continue the conference format started three years ago, offering special featured sessions at the beginning of each day of the technical program to hear personal insights from industry leaders, followed by four parallel tracks, each on a special theme. The conference also has seven tutorial sessions, four on Monday and three on Friday.

The production of COMPCON is made possible by the collective effort of many volunteers, especially the members of the Steering Committee headed by Fred Buelow, and several subcommittes. Many thanks are due to Glen Langdon, Jim Dickie, Bob Fink, Andy Goforth, Rex Rice and Pam Sloan for their enormous and meticulous effort in running the publicity campaign for this year's COMPCON. Special thanks to Bob Fink for his effort and dedication in setting up the local arrangements, and to Roy Lee and Joe Fernandez for organizing the Monday and Friday tutorials. We also thank Dave Hunt, Ross Gaunt, Lori Goerz, Donna Hunt and Jim Rawlings for their administrative support in handling registration and the treasury. Jackie Olila deserves a special recognition for her perseverance and effort in putting together this Digest of Papers. We are also grateful to the members of the IEEE Computer Society's local chapter for their contributions, especially their liaison on our Steering Committee, Ken Majithia. Last, but not least, we thank Ken Miura and Sid Fernbach for their continued advice and guidance to this year's committee.

The heart of COMPCON is the technical program. This is the result of the planning, patience and hard work of our Program Co-Chairs, Michelle Aden and Creve Maples and the contributions of the distinguished members of their Program Committee. We are sure that the result of their effort is an excellent program covering a wide range of topics in the computer field. We also appreciate the effort put forth by the individual session chairpeople and all of the speakers in the conference.

We would like to bring to your attention the two social hours on Tuesday and Wednesday at 5 P.M. There you will have the opportunity to meet your fellow attendees and to meet and discuss the conference with the members of the various COMPCON committees. The entire production committees wish you an enjoyable week at COMPCON under our continued Intellectual Leverage theme!

Roger E. Anderson
General Chairman
COMPCON Spring '91

Program Chairpersons' Message

On behalf of the Program Committee, we wish to welcome you to COMPCON Spring '91, the 36th Annual IEEE International Computer Conference. COMPCON continues its tradition of providing a high-quality forum where computer professionals - engineers, designers, managers, programmers, teachers, users, etc. - can gather to report on and learn about the latest state-of-the-art developments in the broad area of computer science and engineering. In an era with an increasing emphasis on specialization, COMPCON is one of the few remaining broad-based computer conferences. The technical program of the conference is a reflection of what the Program Committee currently perceives as the important topics and significant new developments in the field of computing. The Committee has worked diligently to create a well-balanced program that emphasizes both the breadth of the field and quality of work. Leaders from academia, government, and industry will be presenting their latest results and opinions. All presentations are invited. The program utilizes sessions, tracks, featured speakers and tutorials to achieve both specific focus and breadth of coverage.

Every day begins with Featured Speakers presentations. This year our Featured Speakers will focus on the trends and technology which will shape the direction of computing into the 21st Century. These include "Towards 10^{15} MIPS", by Eric Drexler, president of the Foresight Institute; "America's Answer To Foreign Competition: The Entrepreneur And Inventor" by Gil Hyatt, an inventor recently awarded the patent for the microprocessor; "Virtual Reality: A Computer Science Perspective" by Jaron Lanier, founder and CEO of VPL Research; "Televisions of Tomorrow: Signals With A Sense Of Themselves" by Andy Lipman, associate director of the MIT Media Lab; and "GaAs Digital ICs: The Future Is Now" by Lou Tomasetto, president of Vitesse Semiconductor Corp.

Through the years COMPCON has managed to preserve its excellent technical quality through the hard work of its volunteers in both the Program and Steering Committees. We wish to thank the members of the Program Committee - Roger Anderson, Richard Belgard, Alan G. Bell, Chuck Clanton, Dave Ditzel, Mohammad Ketabchi, Robert Keller, Cary Kornfeld, Ted Laliotis, Glen Langdon, Stan Mazor, Kenichi Miura, Yale Patt, Ken Stevens, and John Wharton - for their effort. We would also like to thank the Session Chairpeople for volunteering to organize and run a session, and of course the speakers who really provide the heart of the conference. A special thanks is also extended to the Steering Committee for their support, to Roy Lee for organizing the tutorials, and to Bob Fink for handling the local arrangements and publicity. Jacquelyn Olila deserves a very special thanks for her tireless efforts in collecting the author's contributions and getting this Digest prepared on time. We also wish thank Carol Lujan for assisting us with the administrative task of puting the conference together. Finally we would like to acknowledge the cooperation and support of Sun Microsystems and Sandia National Laboratories in providing us the time and resources to bring the program together.

Creve Maples
Program Co-Chairperson
COMPCON Spring '91

Michelle Aden
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100 MIPS and Counting

Performance Enhancements in the Superscalar i960MM Embedded Microprocessor

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Intel Corporation, Hillsboro, OR

Abstract

Continued research into Intel's i960 architecture has resulted in the development of performance improvements beyond those implemented in the i960CA microprocessor. These improvements allow additional superscalar dispatch opportunities, reduce memory access delays and enhance the performance of specific instructions. The i960MM microprocessor is an implementation of these performance enhancements. Additionally, the i960MM includes an implementation of a full-function floating-point unit. Performance of 27 MFLOPS (single precision) and 16 MFLOPS (double precision) is achieved on the Linpack benchmarks at 40 MHz. This paper describes both the micro-architectural enhancements to the i960 and the new floating-point unit.

1. Introduction

In 1989 Intel introduced the i960CA, the first microprocessor capable of decoding, dispatching, executing, and returning results from more than one instruction per basic clock cycle. Evolutionary enhancements have been made to a version of the i960CA core that allow more opportunities to dispatch and execute instructions in parallel.

2. The i960 Architecture

This section provides a brief overview of the i960 architecture. More detail may be found in [McG89] and [Myers88], and reference manuals are available [960KB] and [960CA].

2.1. Instruction Set. The i960 architecture presents a simple reduced instruction set to the user. It is a three-operand load/store architecture, and most instructions operate on three register operands, two source operands and a destination, and that the only specific memory load and store instructions explicitly access memory. The architecture defines 24 basic instructions, including the normal arithmetic, logical, and memory access instructions, and 16 extended instructions, including a combined compare-and-branch instruction, subroutine call and return instructions, and atomic and synchronous memory access operations.

All i960 instructions fall into one of four main categories: Register (REG) format instructions, Memory (MEM) instructions, Control (CTRL), and Compare-and-Branch (COBR) instructions. Most general instructions are of the REG type, such as add, subtract, boolean, and bit manipulation instructions. Compare instructions are also of REG type, and are the only general-purpose instructions which set the condition codes. The COBR instructions are a variant of the REG-style compare instructions that combine a comparison operation with a conditional branch. These instructions are useful to reduce code size when a useful instruction cannot be placed in the delay slot after a comparison and prior to a branch instruction. The load, store, and load address instructions are of the MEM type, and may access byte, half-word, word, double-word, triple-word, or quad-word data. Conditional and unconditional branches as well as the call and return instructions are of the CTRL type.

2.2. Register Architecture. The i960 architecture defines a register file consisting of 32 general-purpose registers that are divided into two sets: *global* registers and *local* registers. The local registers **r0** through **r15** represent the currently visible portion of a *local register cache*, where local registers from previous subroutine invocations are retained. Management of the local register cache is fully transparent to the user program, as the processor automatically flushes frames out to memory when the cache becomes full. The 16 global registers are not affected by procedure calls and returns, and are used for parameter passing and, within a procedure, as temporary value registers.

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