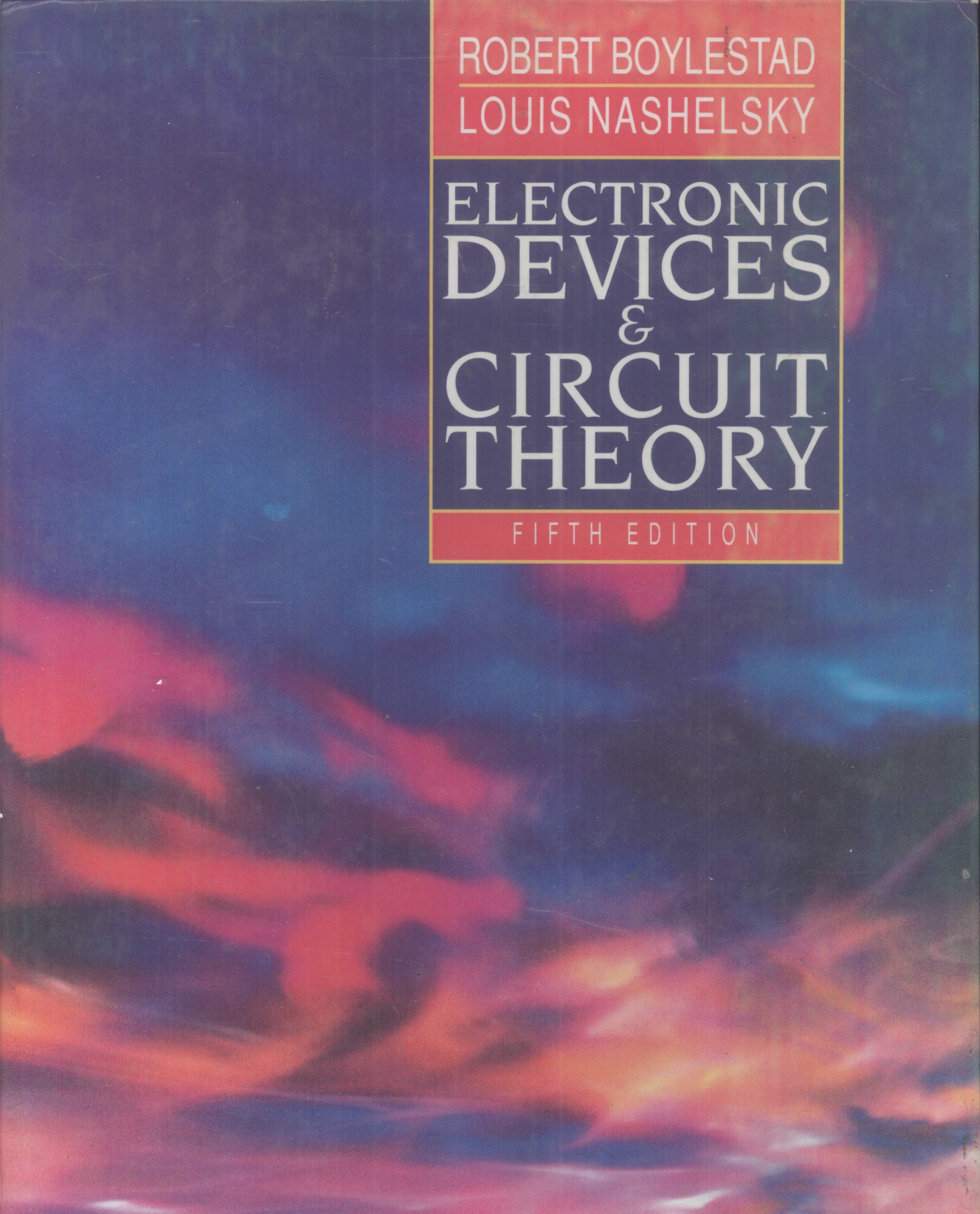
ROBERT BOYLESTAD
LOUIS NASHELSKY

ELECTRONIC DEVICES & CIRCUIT THEORY

FIFTH EDITION



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SIGNIFICANT EQUATIONS

1 Semiconductor Diodes $W = QV$, 1 eV $= 1.6 \times 10^{-19}$ J, $I_D = I_s(e^{kV_D/T_K} - 1)$, $R_{DC} = V_D/I_D$, $r_d = \Delta V_d/\Delta I_d = 26 \text{ mV}/I_D$, $r_{av} = \Delta V_d/\Delta I_d$, $P_D = V_D I_D$, $T_C = \Delta V_z/[V_z(T_1 - T_o)] \times 100\%$

2 Diode Applications $V_{BE} = V_D = 0.7$ V; half-wave: $V_{dc} = 0.318V_m$; full-wave: $V_{dc} = 0.636V_m$

3 Bipolar Junction Transistors $I_E = I_C + I_B$, $I_C = I_{C_{majority}} + I_{CO_{minority}}$, $I_C \simeq I_E$, $V_{BE} = 0.7$ V, $\alpha_{dc} = I_C/I_E$, $I_C = \alpha I_E + I_{CBO}$, $\alpha_{ac} = \Delta I_C/\Delta I_E$, $I_{CEO} = I_{CBO}/(1 - \alpha)$, $\beta_{dc} = I_C/I_B$, $\beta_{ac} = \Delta I_C/\Delta I_B$, $\alpha = \beta/(\beta + 1)$, $\beta = \alpha/(1 - \alpha)$, $I_C = \beta I_B$, $I_E = (\beta + 1)I_B$, $P_{C_{max}} = V_{CE}I_C$

4 DC Biasing: BJTs In general: $V_{BE} = 0.7$ V, $I_C \simeq I_E$, $I_C = \beta I_B$; fixed-bias: $I_B = (V_{CC} - V_{BE})/R_B$, $V_{CE} = V_{CC} - I_C R_C$, $I_{C_{sat}} = V_{CC}/R_C$; emitter-stabilized: $I_B = (V_{CC} - V_{BE})/(R_B + (\beta + 1)R_E)$, $R_i = (\beta + 1)R_E$, $V_{CE} = V_{CC} - I_C(R_C + R_E)$, $I_{C_{sat}} = V_{CC}/(R_C + R_E)$; voltage-divider: exact: $R_{Th} = R_1 \| R_2$, $E_{Th} = R_2 V_{CC}/(R_1 + R_2)$, $I_B = (E_{Th} - V_{BE})/(R_{Th} + (\beta + 1)R_E)$, $V_{CE} = V_{CC} - I_C(R_C + R_E)$, approximate: $V_B = R_2 V_{CC}/(R_1 + R_2)$, $\beta R_E \geq 10R_2$, $V_E = V_B - V_{BE}$, $I_C \simeq I_E = V_E/R_E$; voltage-feedback: $I_B = (V_{CC} - V_{BE})/[R_B + \beta(R_C + R_E)]$; common-base: $I_B = (V_{EE} - V_{BE})/R_E$; switching transistors: $t_{on} = t_r + t_d$, $t_{off} = t_s + t_f$; stability: $S(I_{CO}) = \Delta I_C/\Delta I_{CO}$; fixed-bias: $S(I_{CO}) = \beta + 1$; emitter-bias: $S(I_{CO}) = (\beta + 1)(1 + R_B/R_E)/(1 + \beta + R_B/R_E)$; voltage-divider: $S(I_{CO}) = (\beta + 1)(1 + R_{Th}/R_E)/(1 + \beta + R_{Th}/R_E)$; feedback-bias: $S(I_{CO}) = (\beta + 1)(1 + R_B/R_C)/(1 + \beta + R_B/R_C)$, $S(V_{BE}) = \Delta I_C/\Delta V_{BE}$; fixed-bias: $S(V_{BE}) = -\beta/R_B$; emitter-bias: $S(V_{BE}) = -\beta/[R_B + (\beta + 1)R_E]$; voltage-divider: $S(V_{BE}) = -\beta/[R_{Th} + (\beta + 1)R_E]$; feedback bias: $S(V_{BE}) = -\beta/(R_B + (\beta + 1)R_C)$, $S(\beta) = \Delta I_C/\Delta\beta$; fixed-bias: $S(\beta) = I_{C_1}/\beta_1$; emitter-bias: $S(\beta) = I_{C_1}(1 + R_B/R_E)/[\beta_1(1 + \beta_2 + R_B/R_E)]$; voltage-divider: $S(\beta) = I_{C_1}(1 + R_{Th}/R_E)/[\beta_1(1 + \beta_2 + R_{Th}/R_E)]$; feedback-bias: $S(\beta) = I_{C_1}(R_B + R_C)/[\beta_1(R_B + R_C(1 + \beta_2))]$, $\Delta I_C = S(I_{CO})\,\Delta I_{CO} + S(V_{BE})\,\Delta V_{BE} + S(\beta)\,\Delta\beta$

5 Field-Effect Transistors $I_G = 0$ A, $I_D = I_{DSS}(1 - V_{GS}/V_P)^2$, $I_D = I_S$, $V_{GS} = V_P(1 - \sqrt{I_D/I_{DSS}})$, $I_D = I_{DSS}/4$ (if $V_{GS} = V_P/2$), $I_D = I_{DSS}/2$ (if $V_{GS} \simeq 0.3V_p$), $P_D = V_{DS}I_D$, $I_D = k(V_{GS} - V_T)^2$

6 FET Biasing Fixed-bias: $V_{GS} = -V_{GG}$, $V_{DS} = V_{DD} - I_D R_D$; self-bias: $V_{GS} = -I_D R_S$, $V_{DS} = V_{DD} - I_D(R_S + R_D)$, $V_S = I_S R_S$; voltage-divider: $V_G = R_2 V_{DD}/(R_1 + R_2)$, $V_{GS} = V_G - I_D R_S$, $V_{DS} = V_{DD} - I_D(R_D + R_S)$; enhancement-type MOSFET: $I_D = k(V_{GS} - V_{GS(\text{Th})})^2$, $k = I_{D(\text{on})}/(V_{GS(\text{on})} - V_{GS(\text{Th})})^2$; feedback bias: $V_{DS} = V_{GS}$, $V_{GS} = V_{DD} - I_D R_D$; voltage-divider: $V_G = R_2 V_{DD}/(R_1 + R_2)$, $V_{GS} = V_G - I_D R_S$; universal curve: $m = |V_P|/I_{DSS} R_S$, $M = m \times V_G/|V_P|$, $V_G = R_2 V_{DD}/(R_1 + R_2)$

7 BJT Transistor Modeling $Z_i = V_i/I_i$, $I_i = (V_s - V_i)/R_{\text{sense}}$, $I_o = (V_s - V_o)/R_{\text{sense}}$, $Z_o = V_o/I_o$, $A_v = V_o/V_i$, $A_{v_s} = Z_i A_{v_{\text{NL}}}/(Z_i + R_s)$, $A_i = -A_v Z_i/R_L$, $r_e = 26\ \text{mV}/I_E$; common-base: $Z_i = r_e$, $Z_o \simeq \infty\ \Omega$, $A_v \simeq R_L/r_e$, $A_i \simeq -1$; common-emitter: $Z_i = \beta r_e$, $Z_o = r_o$, $A_v = -R_L/r_e$, $A_i \simeq \beta$, $h_{ie} = \beta r_e$, $h_{fe} = \beta_{ac}$, $h_{ib} = r_e$, $h_{fb} = -\alpha$.

8 BJT Small-Signal Analysis Common-emitter: $A_v = -R_C/r_e$, $Z_i = R_B \| \beta r_e$, $Z_o = R_C$, $A_i \simeq \beta$; voltage-divider: $R' = R_1 \| R_2$, $A_v = -R_C/r_e$, $Z_i = R' \| \beta r_e$, $Z_o = R_C$; emitter-bias: $Z_b = \beta(r_e + R_E) \simeq \beta R_E$, $A_v = -\beta R_C/Z_b = -R_C/(r_e + R_E) \simeq -R_C/R_E$; emitter-follower: $Z_b \simeq \beta(r_e + R_E)$, $A_v \simeq 1$, $Z_o \simeq r_e$; common-base: $A_v \simeq R_C/r_e$, $Z_i = R_E \| r_e$, $Z_o = R_C$; collector feedback: $A_v = -R_C/r_e$, $Z_i = \beta r_e \| R_F/|A_v|$, $Z_o \simeq R_C \| R_F$; collector dc feedback: $A_v = -(R_{F_2} \| R_C)/r_e$, $Z_i = R_{F_1} \| \beta r_e$, $Z_o = R_C \| R_{F_2}$; hybrid parameters: $A_i = h_f/(1 + h_o R_L)$, $A_v = -h_f R_L/[h_i + (h_i h_o - h_f h_r) R_L]$, $Z_i = h_i - h_f h_r R_L/(1 + h_o R_L)$, $Z_o = 1/[h_o - (h_f h_r/(h_i + R_s))]$

9 FET Small-Signal Analysis $g_m = g_{mo}(1 - V_{GS}/V_P)$, $g_{mo} = 2I_{DSS}/|V_P|$; basic configuration: $A_v = -g_m R_D$; unbypassed source resistance: $A_v = -g_m R_D/(1 + g_m R_S)$; source follower: $A_v = g_m R_S/(1 + g_m R_S)$; common gate: $A_v = g_m(R_D \| r_d)$

10 Systems Approach—Effect of R_s and R_L BJT: $A_v = R_L A_{v_{\text{NL}}}/(R_L + R_o)$, $A_i = -A_v Z_i/R_L$, $V_i = R_i V_s/(R_i + R_s)$; fixed-bias: $A_v = -(R_C \| R_L)/r_e$, $A_{v_s} = Z_i A_v/(Z_i + R_s)$, $Z_i = \beta r_e$, $Z_o = R_C$; voltage-divider: $A_v = -(R_C \| R_L)/r_e$, $A_{v_s} = Z_i A_v/(Z_i + R_s)$, $Z_i \simeq R_1 \| R_2 \| \beta r_e$, $Z_o = R_C$; emitter-bias: $A_v = -(R_C \| R_L)/R_E$, $A_{v_s} = Z_i A_v/(Z_i + R_s)$, $Z_i \simeq R_B \| \beta R_E$, $Z_o = R_C$; collector-feedback: $A_v = -(R_C \| R_L)/r_e$, $A_{v_s} = Z_i A_v/(Z_i + R_s)$, $Z_i = \beta r_e \| R_F/|A_v|$, $Z_o \simeq R_C \| R_F$; emitter-follower: $R'_E = R_E \| R_L$, $A_v = R'_E/(R'_E + r_e)$, $A_{v_s} = R'_E/(R'_E + R_s/\beta + r_e)$, $Z_i = R_B \| \beta(r_e + R'_E)$, $Z_o = R_E \| (R_s/\beta + r_e)$; common-base: $A_v \simeq (R_C \| R_L)/r_e$, $A_i \simeq -1$, $Z_i \simeq r_e$, $Z_o = R_C$; FET: bypassed R_S: $A_v = -g_m(R_D \| R_L)$, $Z_i = R_G$, $Z_o = R_D$; unbypassed R_S: $A_v = -g_m(R_D \| R_L)/(1 + g_m R_S)$, $Z_i = R_G$, $Z_o = R_D$; source-follower: $A_v = g_m(R_S \| R_L)/[1 + g_m(R_S \| R_L)]$, $Z_i = R_G$, $Z_o = R_S \| r_d \| 1/g_m$; common gate: $A_v = g_m(R_D \| R_L)$, $Z_i = R_S \| 1/g_m$, $Z_o = R_D$; cascaded: $A_{v_T} = A_{v_1} \cdot A_{v_2} \cdot A_{v_3} \cdots A_{v_n}$, $A_{i_T} = \pm A_{v_T} Z_{i_1}/R_L$

11 BJT and FET Frequency Response $\log_e c$ $\log_{10}a - \log_{10}b$, $\log_{10}1/b = -\log_{10}b$, $\log_{10}ab = \log_{10}a + \log_{10}b$, G_{dB} nW$|_{600\Omega}$, $G_{dB} = 20\log_{10} V_2/V_1$, $G_v = G_{v_1} + G_{v_2} + G_{v_3} + \cdots +$ equency (BJT): $f_{L_S} = 1/2\pi(R_s + R_i)C_S$, $f_{L_C} = 1/2\pi(R_o + R_L)C_C$, $f_{L_E} =$ $_s\|R_1\|R_2$, FET: $f_{L_G} = 1/2\pi(R_{sig} + R_i)C_G$, $f_{L_C} = 1/2\pi R_oC_C$, $f_{L_S} = 1/2$ ffect: $C_{M_i} = (1 -$ $A_v)C_f$, $C_{M_o} = (1 - 1/A_v)C_f$; high frequency (BJT): f_H $C_{W_i} + C_{be} + C_{M_i}$, $f_{H_o} = 1/2\pi R_{Th_2}C_o$, $R_{Th_2} = R_C\|R_L\|r_o$, $C_o = C_{W_o} + C_{ce}$ $3_{mid}f_\beta$; FET: $f_{H_i} = 1/$ $2\pi R_{Th_1}C_i$, $R_{Th_1} = R_{sig}\|R_G$, $C_i = C_{W_i} + C_{gs} + C_{M_i}$, f_{H_o} $_o + C_{ds} + C_{M_o}$; multi- stage: $f_1' = f_1/\sqrt{2^{1/n} - 1}$, $f_2' = (\sqrt{2^{1/n} - 1})f_2$; square $V')/V] \times 100\%$, $f_{L_o} = (P/\pi)f_s$, $P = (V - V')/V$

12 Compound Configurations Differential v common-mode voltage gain: $\beta R_C/[r_i + 2(\beta + 1)R_E]$

13 Discrete and IC Manufacturing Technique

14 Opamps CMRR $= A_d/A_c$; CMRR(log) $= 2C$ $'_1 = -R_f/R_1$; nonin- verting amplifier: $V_o/V_1 = 1 + R_f/R_1$; unity follower: $)V_1 + (R_f/R_2)V_2 +$ $(R_f/R_3)V_3]$; integrator: $v_o(t) = -(1/R_1C_1)\int v_1 dt$

15 Opamp Applications Constant-gain multip $/R_1$; voltage summing: $V_o = -[(R_f/R_1)V_1 + (R_f/R_2)V_2 + (R_f/R_3)V_3]$; high-pa ctive filter: $f_{oH} = 1/2\pi R_1C_1$

16 Power Amplifiers

Power in: $P_i = V_{CC}I_{CQ}$

power out: $P_o = V_{CE}I_C = I_C^2R_C = V_{CE}^2/R_C$ rms
$= V_{CE}I_C/2 = (I_C^2/2)R_C = V_{CE}^2/(2R_C)$ p
$= V_{CE}I_C/8 = (I_C^2/8)R_C = V_{CE}^2/(8R_C)$ p

efficiency: $\%\eta = (P_o/P_i) \times 100\%$

maximum efficiency: Class A, series-fed = 25%
Class A, transformer-coupled = 50%
Class B, push-pull = 78.5%
transformer relations: $V_2/V_1 = N_2/N_1 = I_1/I_2$, $R_2 = (N_2/N_1)^2 R_1$; power output: $P_o = [(V_{CE_{max}} - V_{CE_{min}})(I_{C_{max}} - I_{C_{min}})]/8$; class B power amplifier: $P_i = V_{CC}[(2/\pi)I_{peak}]$; $P_o = V_L^2(\text{peak})/(2R_L)$; % $\eta = (\pi/4)[V_L(\text{peak})/V_{CC}] \times 100\%$; $P_Q = P_{2Q}/2 = (P_i - P_o)/2$; maximum $P_o = V_{CC}^2/2R_L$; maximum $P_i = 2V_{CC}^2/\pi R_L$; maximum $P_{2_Q} = 2V_{CC}^2/\pi^2 R_L$; % total harmonic distortion (% THD) = $\sqrt{D_2^2 + D_3^2 + D_4^2 + \cdots} \times 100\%$; heat-sink: $T_J = P_D\theta_{JA} + T_A$, $\theta_{JA} = 40°\text{C/W}$ (free air); $P_D = (T_J - T_A)/(\Theta_{JC} + \Theta_{CS} + \Theta_{SA})$

17 Linear-Digital ICs Ladder network: $V_o = [(D_0 \times 2^0 + D_1 \times 2^1 + D_2 \times 2^2 + \cdots + D_n \times 2^n)/2^n]V_{ref}$; 555 oscillator: $f = 1.44(R_A + 2R_B)C$; 555 monostable: $T_{high} = 1.1R_AC$; VCO: $f_o = (2/R_1C_1)[(V^+ - V_C)/V^+]$; phase-locked loop (PLL): $f_o = 0.3/R_1C_1$, $f_L = \pm 8f_o/V$, $f_C = \pm(1/2\pi)\sqrt{2\pi f_L/(3.6 \times 10^3)C_2}$

18 Feedback Amplifiers and Oscillator Circuits $A_f = A/(1 + \beta A)$; series feedback; $Z_{if} = Z_i(1 + \beta A)$; shunt feedback: $Z_{if} = Z_i/(1 + \beta A)$; voltage feedback: $Z_{of} = Z_o/(1 + \beta A)$; current feedback: $Z_{of} = Z_o(1 + \beta A)$; gain stability: $dA_f/A_f = 1/(|1 + \beta A|)(dA/A)$; oscillator; $\beta A = 1$; phase shift: $f = 1/2\pi RC\sqrt{6}$, $\beta = 1/29$, $A > 29$; FET phase shift: $|A| = g_m R_L$, $R_L = R_D r_d/(R_D + r_d)$; transistor phase shift: $f = (1/2\pi RC)[1/\sqrt{6 + 4(R_C/R)}]$, $h_{fe} > 23 + 29(R_C/R) + 4(R/R_C)$; Wien bridge: $R_3/R_4 = R_1/R_2 + C_2/C_1$, $f_o = 1/2\pi\sqrt{R_1C_1R_2C_2}$; tuned: $f_o = 1/2\pi\sqrt{LC_{eq}}$, $C_{eq} = C_1C_2/(C_1 + C_2)$, Hartley: $L_{eq} = L_1 + L_2 + 2M$, $f_o = 1/2\pi\sqrt{L_{eq}C}$

19 Power Supplies (Voltage Regulators) Filters: $r = V_r(\text{rms})/V_{dc} \times 100\%$, V.R. = $(V_{NL} - V_{FL})/V_{FL} \times 100\%$, $V_{dc} = V_m - V_r(\text{p-p})/2$, $V_r(\text{rms}) = V_r(\text{p-p})/2\sqrt{3}$, $V_r(\text{rms}) \simeq (I_{dc}/4\sqrt{3})(V_{dc}/V_m)$; full-wave, light load $V_r(\text{rms}) = 2.4I_{dc}/C$, $V_{dc} = V_m - 4.17I_{dc}/C$, $r = (2.4I_{dc}/CV_{dc}) \times 100\% = 2.4/R_LC \times 100\%$, $I_{peak} = T/T_1 \times I_{dc}$; RC filter: $V'_{dc} = R_L V_{dc}/(R + R_L)$, $X_C = 2.653/C$ (half-wave), $X_C = 1.326/C$ (full-wave), $V'_r(\text{rms}) = (X_C/\sqrt{R^2 + X_C^2})$; regulators: $IR = (I_{NL} - I_{FL})/I_{FL} \times 100\%$, $V_L = V_z(1 + R_1/R_2)$, $V_o = V_{ref}(1 + R_2/R_1) + I_{adj}R_2$

20 Other Two-Terminal Devices Varactor diode: $C_T = C(0)/(1 + |V_r/V_T|)^n$, $T_{C_C} = (\Delta C/C_o(T_1 - T_0)) \times 100\%$; photodiode: $W = hf$, $\lambda = v/f$, 1 lm = 1.496×10^{-10} W

21 PNPN and Other Devices UJT: $R_{BB} = (R_{B_1} + R_{B_2})|_{I_E = 0}$, $V_{R_{B_1}} = \eta V_{BB}|_{I_E = 0}$, $\eta = R_{B_1}/(R_{B_1} + R_{B_2})|_{I_E = 0}$, $V_P = \eta V_{BB} + V_D$; phototransistor: $I_C \simeq h_{fe}I_\lambda$; PUT: $\eta = R_{B_1}/(R_{B_1} + R_{B_2})$, $V_P = \eta V_{BB} + V_D$

ELECTRONIC DEVICES AND CIRCUIT THEORY

Dedicated to:

ELSE MARIE, ERIC, ALISON, STACEY, and JOHANNA

and to

KATRIN, KIRA, LARREN, THOMAS, and JUSTIN

Preface

As we approached the 20th anniversary of the text it became increasingly clear that this 5th edition should represent a major revision of the work. The growing use of computer software, packaged IC units, and the expanded range of coverage necessary in the basic courses all were contributing factors in defining the content of this edition. Our continued teaching experience with the subject matter, feedback from numerous educators and reviewers and comments from students have helped define an improved pedagogy for the text. The general appearance of the text needed to be enhanced for improved readability—making the text material appear "friendlier" to the broad range of students. Accuracy is obviously very important, and considerable effort was directed toward careful reviewing of all examples, artwork, problems, and technical development of concepts. Inconsistencies in the artwork developed over past editions have been removed by a totally new rendering of all the artwork using computer generated figures. A broad range of ancillary material will accompany the text to support the educational process.

PEDAGOGY

Without question one of the most important improvements in this text is the manner in which the content lends itself to the typical course syllabus. Not only has the order of chapters and internal sections been changed but sections of a chapter that were primarily reading material has been moved to later chapters to insure a continuous, logical, sequential presentation of important concepts and methods of analysis. Our teaching experience with the new presentation has reinforced our belief that the material now has an improved pedagogy to support the instructor's lecture and help the student build the foundation necessary for his/her future studies. The number of examples has been substantially increased and isolated bold-faced ("bullet") statements have been introduced to identify important statements and conclusions. The format has been revamped to establish a friendlier appearance to the student and insure that the artwork is as close to the reference as possible. An additional color was employed in a manner that helps define important characteristics or isolate specific quantities in a network or on a characteristic. Icons have been developed for each chapter of the text to facilitate referencing a particular area of the text as quickly as possible. Problems have been developed for each section of the text that progress

from the simple to the more complex. In addition, an asterisk has been added to identify the more difficult exercises. The title of each section is also reproduced in the problem section to clearly identify the exercises of interest for a particular topic of study.

SYSTEMS APPROACH

On numerous visits to other schools, technical institutes and meetings of various societies it was noted that a more "systems approach" should be developed to support a student's need to become adept in the application of packaged systems. Chapters 8, 9, and 10 were specifically reorganized to develop the foundation of systems analysis to the degree possible at this introductory level. Although it may be easier to consider the effects of R_s and R_L with each configuration when first introduced, the effects of R_s and R_L also provide an opportunity to apply some of the fundamental concepts of system analysis. The later chapters on Op-amps and IC units will further develop the concepts introduced in these early chapters.

ACCURACY

There is no question that a primary goal of any publication is that it be as free of errors as possible. Certainly, the intent is not to challenge the instructor or student with planned inconsistencies. In fact, there is nothing more distressing to an author than to hear of errors in a text. To insure the highest level of accuracy for this edition there were three technical reviewers in addition to the efforts of both authors. In addition, solutions to many problems and examples were checked using the computer. We now feel certain that this text will enjoy the highest level of accuracy obtainable for a publication of this kind.

TRANSISTOR MODELLING

BJT transistor modelling is area that is approached in various ways. Some institutions employ the r_e model exclusively while others lean toward the hybrid approach or a combination of these two. This edition will emphasize the r_e model with sufficient coverage of the hybrid model to permit comparison between models and the application of both. An entire chapter (Chapter 7) has been devoted to the introduction of the models to insure a clear, correct understanding of each and the relationships that exist between the two.

PSpice AND BASIC

The last few years have seen a continuing growth of the computer content in introductory courses. Not only is the use of word-processing appearing in the first semester, but spreadsheets and the use of a software analysis package such as PSpice is also being introduced in numerous educational institutions.

PSpice was chosen as the package to appear throughout this text because recent surveys suggest that it is most frequently employed. Other possible packages include Micro-Cap III and Breadboard. The coverage of PSpice provides sufficient content to permit writing the input file for the majority of networks analyzed in this text. No prior knowledge of computer software packages is presumed.

There are a number of BASIC programs still included in the text to demonstrate the advantages of knowing a computer language and the additional benefits that arise from its use.

TROUBLESHOOTING

Troubleshooting is undoubtedly one of the most difficult to introduce, develop and demonstrate in a text mode. It is an art that can be introduced using a variety of techniques but experience and exposure are obviously the key elements in developing the necessary skills. The content is essentially a review of situations that frequently occur in the laboratory environment. Some general hints as to how to isolate a problem area are introduced along with a list of typical causes. This is not to suggest that the student will become proficient in the debugging of networks introduced in this text, but at the very least the reader will have some understanding of what is involved with the troubleshooting process.

NEW MATERIAL

Specific areas of the text have been expanded and new material has been introduced to satisfy the changing requirements of the basic electronics courses. The application of various devices has been increased in number with an increased emphasis on the frequency response. Op-amps are a particularly important component in today's market and have received the full treatment with two expanded chapters of coverage.

The chapter on instrumentation has reappeared in this edition in response to a survey of current users and the obvious need to provide some reading material for those students with limited laboratory experience. The user guides provided with laboratory equipment is seldom at the reading level of new electronics students.

ANCILLARIES

The range of ancillary material has grown considerably. In addition to a completely revised laboratory manual with an associated instructor's manual (with typical data) there is a disk with all the input files of the PSpice programs and more than 250 transparency masters. The Instructor's Solutions Manual for the text has been carefully prepared and reviewed to insure the highest level of accuracy. In fact, a majority of the solutions were tested using PSpice.

USE OF TEST

In general the text is broken down into two main components, the dc analysis and the ac or frequency response. For some schools the dc section is sufficient for a one semester sequence while for others the entire text may be covered in one semester by choosing specific topics. In any event the text is one that "builds" from the early chapters. Superfluous material is relegated to the later chapters to avoid excessive content on a particular subject early in the development stage. For each device the text has covered a majority of the important configurations and applications. By choosing specific examples and applications the content of a course can be reduced without losing the progressive building characteristics of the text. Then again, if an instructor feels a specific area particularly important the detail is provided for a more extensive review.

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