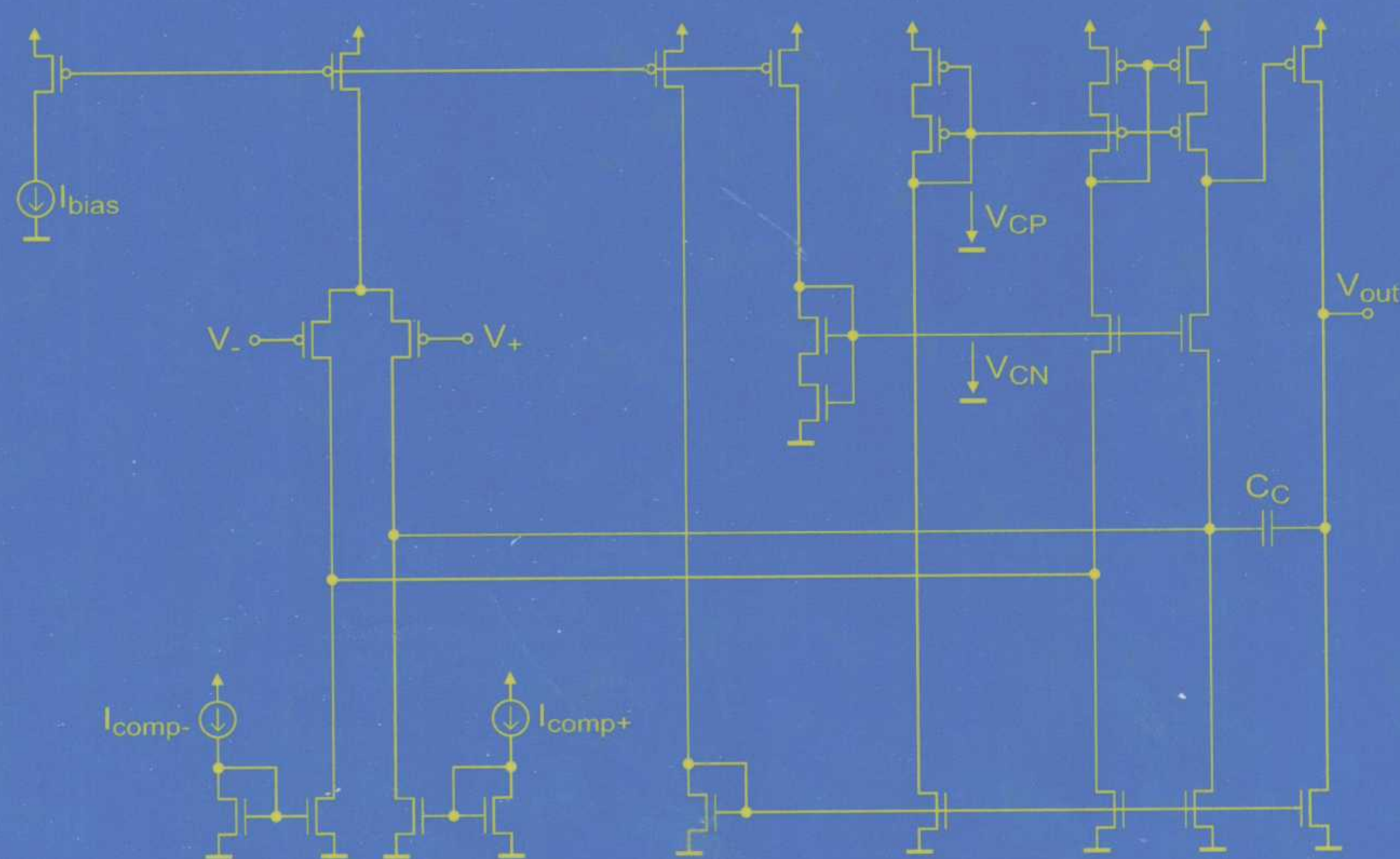


METHODOLOGY FOR THE DIGITAL CALIBRATION OF ANALOG CIRCUITS AND SYSTEMS

with Case Studies

Marc Pastre and Maher Kayal



Springer

METHODOLOGY FOR THE DIGITAL CALIBRATION OF ANALOG CIRCUITS AND SYSTEMS

with Case Studies

by

Marc Pastre

*Ecole Polytechnique Fédérale de Lausanne,
Switzerland*

and

Maher Kayal

*Ecole Polytechnique Fédérale de Lausanne,
Switzerland*



Springer

A C.I.P. Catalogue record for this book is available from the Library of Congress.

ISBN-10 1-4020-4252-3 (HB)
ISBN-13 978-1-4020-4252-2 (HB)
ISBN-10 1-4020-4253-1 (e-book)
ISBN-13 978-1-4020-4253-9 (e-book)

Published by Springer,
P.O. Box 17, 3300 AA Dordrecht, The Netherlands.

www.springeronline.com

Printed on acid-free paper

All Rights Reserved
© 2006 Springer

No part of this work may be reproduced, stored in a retrieval system, or transmitted in any form or by any means, electronic, mechanical, photocopying, microfilming, recording or otherwise, without written permission from the Publisher, with the exception of any material supplied specifically for the purpose of being entered and executed on a computer system, for exclusive use by the purchaser of the work.

Printed in the Netherlands.

Contents

List of Figures	xi
List of Tables	xvii
1. INTRODUCTION	1
1 Context	1
2 Objectives	2
3 Compensation methodology	2
4 Applications of the compensation methodology	2
5 Book organization	3
2. AUTOCALIBRATION AND COMPENSATION TECHNIQUES	5
1 Introduction	5
2 Matching	5
2.1 Matching rules	6
2.2 Matching parameters	6
3 Chopper stabilization	7
3.1 Principle	7
3.2 Analysis	8
3.3 Implementation	9
4 Autozero	11
4.1 Principle	11
4.2 Analysis	12
4.3 Noise	14
5 Correlated double sampling	18
6 Ping-pong	18
7 Other techniques	20

8	Classification	21
9	Conclusion	22
3.	DIGITAL COMPENSATION CIRCUITS AND SUB-BINARY DIGITAL-TO-ANALOG CONVERTERS	23
1	Introduction	23
2	Digital compensation	23
3	Successive approximations	24
3.1	Principle	25
3.2	Working condition	28
3.3	Reverse successive approximations algorithm	29
3.4	Complexity	31
4	Sub-binary radix DACs	31
4.1	Use of sub-binary DACs for successive approximations	31
4.2	Characteristics	32
4.3	Resolution	34
4.4	Tolerance to radix variations	34
5	Component arrays	35
5.1	Sizing	36
6	Current sources	38
6.1	Current-mirror DAC	39
7	R/2R ladders	40
8	Linear current division using MOS transistors	41
8.1	Principle	41
8.2	Second-order effects	45
8.3	Parallel configuration	45
8.4	Series configuration	46
9	M/2M ladders	48
9.1	Principle	48
9.2	Complementary ladder	49
9.3	Second-order effects	50
9.4	Trimming	51
10	R/xR ladders	51
10.1	Principle	51
10.2	Working condition	53
10.3	Terminator calculation	54
10.4	Terminator implementation	55
10.5	Ladder sizing	57
10.6	Terminator sizing	58

10.7	Radix	60
11	$M/2^+M$ ladders	62
11.1	$M/3M$ ladders	62
11.2	$M/2.5M$ ladders	64
11.3	Ladder selection and other $M/2^+M$ ladders	65
11.4	Current collector design	67
11.5	Complementary ladders	72
11.6	Layout	72
11.7	Measurements	73
12	Comparison	77
13	Linear DACs based on $M/2^+M$ converters	78
13.1	Principle	78
13.2	Calibration algorithm	81
13.3	Radix conversion algorithm	84
13.4	Digital circuit implementation	85
13.5	Analog circuit implementation	87
13.6	Compensation of temperature variations	90
13.7	Comparison with other self-calibrated converters	90
14	Conclusion	91
4.	METHODOLOGY FOR CURRENT-MODE DIGITAL COMPENSATION OF ANALOG CIRCUITS	93
1	Introduction	93
2	Two-stage Miller operational amplifier	93
3	Compensation current technique	96
3.1	Detection configuration	97
3.2	Detection node	100
3.3	Compensation node	105
3.4	DAC resolution	113
3.5	Low-pass decision filtering	114
3.6	Continuous-time compensation	115
3.7	Up/down DAC	117
4	Simulation with digital compensation circuits	124
4.1	Principle	125
4.2	Automatic compensation component	126
4.3	Compensation component during adjustment	128
4.4	Compensation component during compensation	130
4.5	Multiple digital compensation	133
4.6	Example of implementation for PSpice	134

4.7	Offset compensation of the Miller amplifier	136
5	Application to SOI 1T DRAM calibration	138
5.1	1-transistor SOI memory cell	139
5.2	Memory cell imperfections	140
5.3	Sensing scheme	141
5.4	Calibration principle	144
5.5	Calibration algorithm	146
5.6	Measurements	147
6	Conclusion	148
5.	HALL MICROSYSTEM WITH CONTINUOUS DIGITAL GAIN CALIBRATION	151
1	Introduction	151
2	Integrated Hall sensors	151
2.1	Hall effect	152
2.2	Hall sensors	153
2.3	Hall sensor models	155
3	Spinning current technique	157
4	Sensitivity calibration of Hall sensors	160
4.1	Sensitivity drift of Hall sensors	161
4.2	Integrated reference coils	162
4.3	Sensitivity calibration	163
4.4	State of the art	166
5	Hall sensor microsystems	171
5.1	Analog front-ends for current measurement	171
6	Continuous digital gain calibration technique	173
6.1	Principle	173
6.2	Combined modulation scheme	175
6.3	Demodulation schemes	176
6.4	Gain compensation	179
6.5	Offset compensation	183
6.6	Noise filtering	184
6.7	Delta-sigma analog-to-digital converter	189
6.8	Rejection of signal interferences	193
7	Conclusion	197
6.	IMPLEMENTATION OF THE HALL MICROSYSTEM WITH CONTINUOUS CALIBRATION	199
1	Introduction	199

2	Hall sensor array	199
3	Preamplifier	201
3.1	Programmable gain range preamplifier	201
3.2	DDA	202
3.3	Operational amplifier	207
4	Demodulators	208
4.1	Switched-capacitor integrators	209
4.2	External signal demodulator	213
4.3	Reference demodulator	216
4.4	Offset demodulator	220
5	Delta-sigma modulator	221
6	System improvements	224
6.1	Compensation of the reference demodulator offset	224
6.2	Coil-sensor capacitive coupling	225
6.3	External interferences	226
6.4	Alternate modulation/demodulation schemes	227
7	System integration	230
7.1	Configuration and measurement possibilities	230
7.2	Integrated circuit	231
7.3	Measurement results	233
8	Conclusion	240
7.	CONCLUSION	241
1	Highlights	241
2	Main contributions	242
3	Perspectives	242
	References	245
	Index	255

List of Figures

Figure 1.	Functional chopper amplifier	7
Figure 2.	Temporal analysis of a chopper amplifier	8
Figure 3.	Frequency analysis of a chopper amplifier	8
Figure 4.	Fully differential chopper amplifier	9
Figure 5.	Implementation of a modulator/demodulator using cross-coupled switches	10
Figure 6.	CMOS transmission gate	10
Figure 7.	Demodulator for single output chopper amplifier	11
Figure 8.	Autozero amplifier principle	12
Figure 9.	Analogically compensated autozero amplifier	13
Figure 10.	Digitally compensated autozero amplifier	13
Figure 11.	Autozero baseband and foldover noise transfer functions	15
Figure 12.	Resulting noise with autozero and small amplifier bandwidth	16
Figure 13.	Resulting noise with autozero and large amplifier bandwidth	17
Figure 14.	Effect of the $1/f$ corner frequency on the resulting noise	18
Figure 15.	Ping-pong amplifier system	19
Figure 16.	Operational amplifier swapping	20
Figure 17.	Digital compensation of the offset of an operational amplifier	24
Figure 18.	Ideal 4-bits DAC input/output characteristics	25
Figure 19.	Equivalent offset	26

Figure 20.	Successive approximations algorithm	26
Figure 21.	Successive approximations algorithm timing	27
Figure 22.	Reverse successive approximations algorithm	30
Figure 23.	Reverse successive approximations algorithm timing	30
Figure 24.	Input/output characteristics of a radix 1.75 DAC	32
Figure 25.	Input/output characteristics of a radix 1.5 DAC	33
Figure 26.	Parallel capacitor array	36
Figure 27.	Series resistor array	36
Figure 28.	Sub-binary DAC based on current-mirrors	39
Figure 29.	Current-mode R/2R ladder	40
Figure 30.	Normalized drain current of the MOS transistor	43
Figure 31.	Current division circuit	43
Figure 32.	Current division without input current	44
Figure 33.	Current division with input	44
Figure 34.	Equivalent transistor of two transistors in parallel	46
Figure 35.	Equivalent transistor of two transistors in series	47
Figure 36.	M/2M ladder	48
Figure 37.	PMOS M/2M ladder	49
Figure 38.	Inverse M/2M ladder	50
Figure 39.	R/xR ladder	51
Figure 40.	Modified R/xR ladder	53
Figure 41.	2R terminator in a R/3R ladder	56
Figure 42.	Maximum allowable mismatch in function of xT	59
Figure 43.	Best-achievable radix with a sub-binary converter	61
Figure 44.	M/3M ladder	62
Figure 45.	M/2.5M ladder	64
Figure 46.	M/2 ⁺ M ladder selection	66
Figure 47.	Current mirror as M/3M current collector	68
Figure 48.	Voltage/current characteristics of a diode-connected transistor	69
Figure 49.	Successive approximations with current mirrors as collectors	71
Figure 50.	Layout overview of one stage of a M/2.5M converter	72
Figure 51.	M/2 ⁺ M test-chip micrograph	73

Figure 52.	Standard deviation of the current division in $M/2.5M$ ladders	75
Figure 53.	Standard deviation of ρ in each stage of the $M/2.5M_4$ ladder	76
Figure 54.	Standard deviation of ρ in each stage of the $M/3M_1$ ladder	77
Figure 55.	Input/output characteristics before calibration	79
Figure 56.	Input/output characteristics after calibration	80
Figure 57.	DAC system architecture	81
Figure 58.	DAC calibration principle	82
Figure 59.	DAC calibration algorithm	83
Figure 60.	DAC radix conversion algorithm	85
Figure 61.	Digital circuit implementation	86
Figure 62.	Transresistance current collector	87
Figure 63.	Regulated cascode current collector	88
Figure 64.	Single-input current comparator	89
Figure 65.	DAC micrograph	90
Figure 66.	Two-stage Miller operational amplifier	94
Figure 67.	Small-signal model of the two-stage amplifier	95
Figure 68.	Offset detection in the closed-loop configuration	98
Figure 69.	Offset detection in the open-loop configuration	100
Figure 70.	Offset measurement in the closed-loop configuration	101
Figure 71.	Offset measurement in the open-loop configuration	102
Figure 72.	Implementation of a comparator with a digital buffer	104
Figure 73.	Input/output characteristics of the CMOS inverter	104
Figure 74.	Compensation by current injection	105
Figure 75.	Offset correction by additional differential pair	107
Figure 76.	Offset correction by degenerated current mirror	107
Figure 77.	Offset correction by unilateral current injection	108
Figure 78.	Offset correction by improved unilateral current injection	110
Figure 79.	Offset correction by bilateral current injection	111
Figure 80.	Analog averaging of the offset measurement	114
Figure 81.	Digital averaging of the offset measurement	115
Figure 82.	Imperfection tracking with successive approximations	116
Figure 83.	Imperfection tracking with up/down	117

Figure 84.	Up/down current mirror principle	118
Figure 85.	Smooth transition during up/down step	119
Figure 86.	Up/down current mirror schematic	122
Figure 87.	Up/down current mirror micrograph	124
Figure 88.	2-pass simulation algorithm	125
Figure 89.	Single-ended compensation component in the schematic editor	126
Figure 90.	Differential compensation component in the schematic editor	127
Figure 91.	Single-ended compensation component netlist for the first pass	128
Figure 92.	Model of the analog feedback loop of the first pass	128
Figure 93.	Differential compensation component netlist for the first pass	130
Figure 94.	Single-ended compensation component netlist for the second pass	131
Figure 95.	Final value range of the successive approximations algorithm	132
Figure 96.	Differential compensation component netlist for the second pass	133
Figure 97.	Modified 2-pass simulation algorithm	134
Figure 98.	PSpice diode model	135
Figure 99.	Programmable current source	136
Figure 100.	Untrimmed offset of a typical Miller amplifier	137
Figure 101.	Miller amplifier offset with single-ended 8-bits trimming	138
Figure 102.	SOI 1T DRAM cell	139
Figure 103.	Read current dispersion of the 1T DRAM cell	140
Figure 104.	Retention characteristics of the 1T DRAM cell	141
Figure 105.	Reference current window as a function of time	141
Figure 106.	Sense amplifier for SOI 1T DRAM	142
Figure 107.	Sense amplifier model	143
Figure 108.	Automatic reference adjustment algorithm	145
Figure 109.	Optimized automatic reference adjustment algorithm	147
Figure 110.	Write/read cycles on 3 adjacent memory cells	148
Figure 111.	Hall effect	152

Figure 112.	Cross-like Hall sensor and symbol	153
Figure 113.	Cross-like Hall sensor implementation in P-substrate CMOS	154
Figure 114.	Purely resistive Hall sensor model	155
Figure 115.	Modelling of the offset of the Hall sensor	156
Figure 116.	Modelling of the offset and Hall effect	156
Figure 117.	Spinning current technique	157
Figure 118.	Sensor and preamplifier	158
Figure 119.	Typical thermal drift of the current-related sensitivity	161
Figure 120.	Integrated calibration coil	162
Figure 121.	Sensitivity calibration principle	164
Figure 122.	Influence of the calibration period on the variation of B_{ext}	166
Figure 123.	Calibration by dual signal \pm reference measurement paths	167
Figure 124.	Calibration by separate signal and reference measurement paths	169
Figure 125.	Calibration by frequency separation	170
Figure 126.	System architecture	174
Figure 127.	Gain adjustment feedback loop	180
Figure 128.	Gain adjustment feedback loop with ADC and digital comparison	181
Figure 129.	Compensation current injection	182
Figure 130.	Offset correction feedback loop	183
Figure 131.	Spectral representation of the modulated reference signal	185
Figure 132.	Band-limitation of the noise to increase the SNR	186
Figure 133.	Low-pass filtering after demodulation to increase the SNR	187
Figure 134.	Demodulator and delta-sigma filter transfer functions	188
Figure 135.	Delta-sigma used as an analog-to-digital integrator	189
Figure 136.	Typical signals in the delta-sigma modulator	190
Figure 137.	Low-pass filter function of the delta-sigma ADC	193
Figure 138.	High-pass parasitic transfer function of the reference demodulator	195
Figure 139.	Parasitic transfer function before and after filtering	196

Figure 140.	Hall sensor and reference coil array	200
Figure 141.	Preamplifier block diagram	201
Figure 142.	Sensor array and first stage of the preamplifier	202
Figure 143.	Model of the DDA with 5 differential inputs	203
Figure 144.	Schematic of the DDA	205
Figure 145.	Schematic of the operational amplifier	207
Figure 146.	Switched-capacitor integrator	209
Figure 147.	Addition principle	210
Figure 148.	Subtraction principle	211
Figure 149.	Switch timing for an addition	212
Figure 150.	Switch timing for a subtraction	212
Figure 151.	External signal demodulator switch timing	214
Figure 152.	Demodulator phase shift	215
Figure 153.	Reference demodulator	217
Figure 154.	Reference signal demodulator switch timing	218
Figure 155.	Offset signal demodulator switch timing	221
Figure 156.	Delta-sigma modulator	222
Figure 157.	Delta-sigma switch timing	223
Figure 158.	Offset compensation in the gain adjustment feedback loop	224
Figure 159.	Model of the coil-sensor capacitive coupling	225
Figure 160.	Micrograph of the current measurement microsystem	232
Figure 161.	Preamplifier and demodulator output for $B_{\text{ext}} = 0$	235
Figure 162.	Preamplifier and demodulator output for negative B_{ext}	236
Figure 163.	Preamplifier and demodulator output for positive B_{ext}	237
Figure 164.	Nonlinearity measurement	238
Figure 165.	Offset drift measurement	239
Figure 166.	Sensitivity drift measurement	239

List of Tables

Table 1.	Characteristics of the compensation techniques	21
Table 2.	Successive approximations algorithm timing	28
Table 3.	Reverse successive approximations algorithm timing	31
Table 4.	Bit current values in the sub-binary DAC	39
Table 5.	Characteristics of the M/3M ladder	63
Table 6.	Characteristics of the M/2.5M ladder	65
Table 7.	2^+ resistor implementation	67
Table 8.	M/2 ⁺ M test-chip ladder characteristics	74
Table 9.	M/2 ⁺ M current division measurement	74
Table 10.	Calibration table for the example of figure 55	84
Table 11.	Characteristics of the two-stage Miller operational amplifier	96
Table 12.	Closed-loop and open-loop offset measurement	103
Table 13.	Compensation currents for worst-case and Monte Carlo	131
Table 14.	Typical specifications of a current measurement microsystem	172
Table 15.	Combined modulation scheme	176
Table 16.	Demodulation schemes	177
Table 17.	External signal, reference signal and noise levels	184
Table 18.	Sensor and coil characteristics	201
Table 19.	Characteristics of the DDA	206
Table 20.	Characteristics of the operational amplifier	208
Table 21.	External signal demodulation intermediate results	216
Table 22.	Reverse modulation scheme	228

Table 23.	Reverse demodulation schemes	228
Table 24.	Multiplexed modulation scheme	229
Table 25.	Multiplexed demodulation scheme	230
Table 26.	Capacitor values in the reference demodulator	231
Table 27.	Pin functions	233
Table 28.	Demodulator output for $B_{\text{ext}} = 0$	235
Table 29.	Demodulator output for negative B_{ext}	236
Table 30.	Demodulator output for positive B_{ext}	237
Table 31.	Microsystem characteristics	240

Chapter 1

Introduction

1 CONTEXT

Ever since the invention of the transistor in the late 50's, its fabrication technology has been evolving, allowing the device integration in a continuously shrinking area. High-performance integrated analog systems have always been difficult to design. Sometimes, calibration is used to gather the extra performance that the analog devices cannot provide intrinsically. But the evolution of the manufacturing technology renders even basic analog systems difficult to design today. With the size reduction, the intrinsic precision of the components degrades. In parallel, the supply voltage decreases, limiting the topologies which can be used. Many modern technologies are specifically suited for pure digital circuits, and some analog devices, like capacitors, are not available. In these conditions, analog design is a challenge even for experienced designers.

To relieve the extreme design constraints in analog circuits, digital calibration becomes a must. It allows a low-precision component to be used in high-performance systems. If the calibration is repeated, it can even cancel the effect of temperature drift and ageing.

The digital calibration is compatible with the evolution of fabrication technologies, which ever more facilitates the integration of digital solutions at the cost of a dramatic reduction of analog performances. Thanks to the reduction of the size of digital devices, even complex digital calibration solutions can be integrated and become a viable alternative to intrinsically precise analog designs.

Digital calibration allows to realize high-performance analog systems with modern technologies. This enables pure analog designs to be implemented even in fully digital processes. In existing mixed-signal designs, the full system realization also becomes possible with technologies providing higher integration density. Finally, because circuit performances rely on digital calibration, retargeting is simplified. The digital blocks can be synthesized automatically, whereas only a limited design effort is invested in the analog circuit.