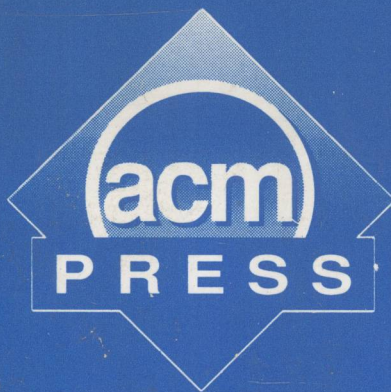




SPAA '92

**4th Annual ACM Symposium
on Parallel Algorithms
and Architectures**

**June 29 – July 1, 1992
San Diego, California**

**Sponsored by
ACM SIGACT
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Foreword

The papers in this volume were presented at the 4th Annual ACM Symposium on Parallel Algorithms and Architectures, held on June 29 - July 1, 1992 at San Diego California. The symposium was sponsored by the Special Interest Group on Automata and Computability Theory (SIGACT) and the Special Interest Group on Computer Architecture (SIGARCH) of the ACM, in cooperation with European Association for Theoretical Computer Science (EATCS).

The 45 papers were chosen by the program committee from the 120 extended abstracts submitted. The Committee's decisions were based on the perceived originality, quality, and appropriateness to the theme of the Symposium. The submissions were not refereed; it is expected that the authors will publish polished and complete versions in scientific journals.

The Program Committee would like to express its thanks to all who submitted papers for consideration.

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SPAA'92: 4th Annual ACM Symposium on Parallel Algorithms and Architectures

Following two pages were omitted from the SPAA'92 proceedings, 4th Annual ACM Symposium on Parallel Algorithms and Architectures. The figures are referred to in the article SPAA'92, " pages 316 - 322, by Jeffrey M. Arnold, Duncan A. Buell, and Elaine G. Davis, of Supercomputing Research Center in Bowie, Maryland.

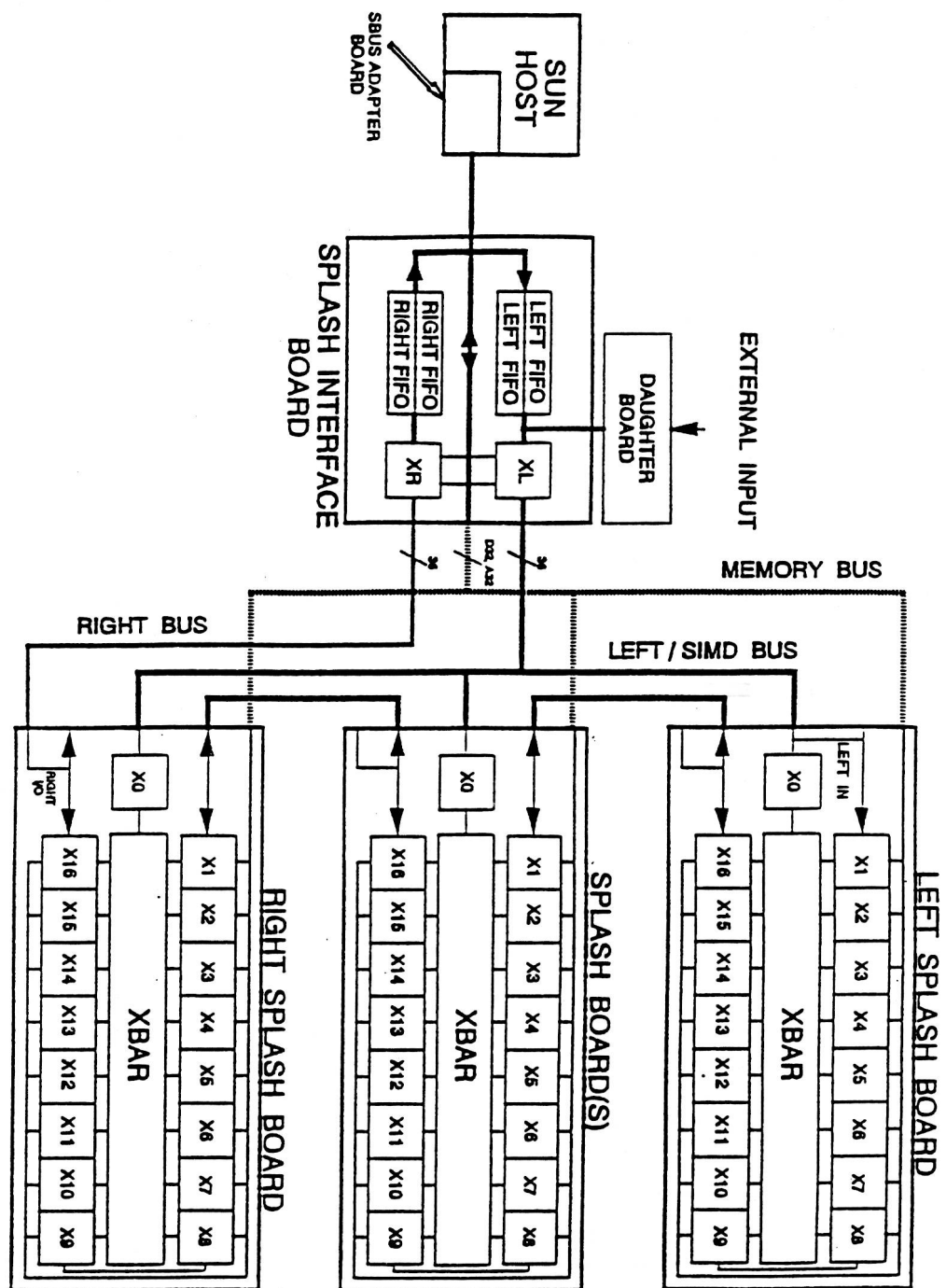


Figure 1. The SBus Adapter Board

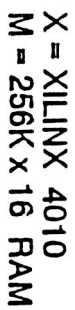


Figure 2: The SPLASH II Board

Keynote Speech

Charles L. Seitz

Caltech

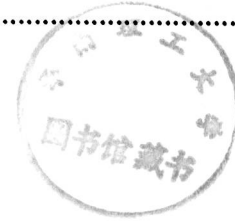
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Keynote Speech

Charles L. Seitz

Caltech

“The Caltech Mosaic C: an Experimental, Fine-Grain Multicomputer”

SESSION 1: Routing

Adaptive Deadlock- and Livelock-Free Routing With All Minimal Paths in Torus Networks

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Abstract

This paper consists of two parts. In the first part, a new algorithm for deadlock- and livelock-free routing for the n -dimensional torus network is presented. This algorithm, called **-Channels*, is *fully-adaptive minimal*, i.e. all paths with a minimal number of hops from source to destination are available for routing. **-Channels* works for messages of unknown size, thus yielding new routing techniques for both packet-switched and *worm-hole* models. **-Channels* differs radically from the packet-switched fully-adaptive minimal methods presented in SPAA '91 by Pifarré, Gravano, Felperin, and Sanz [PGFS91]. In particular, the packet-based techniques in [PGFS91] do not work for worm-hole routing as deadlock situations can be constructed.

**-Channels* requires only five virtual channels per bidirectional link of the n -dimensional torus. In fact, only three virtual channels are necessary for the links in one of the dimensions, thus yielding a total of $10(n - 1) + 6$ buffers per node.

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This bound gives the smallest number of channels known in the literature for fully-adaptive minimal *worm-hole* routing. Previous algorithms for fully-adaptive worm-hole routing in n -dimensional tori require more than $O(2^{n-1})$ virtual channels per bidirectional link (see [LH91]). In addition, these results also yield the smallest number of buffers known in the literature for packet-switched fully-adaptive minimal routing.

In the second part of this paper, a comparison of four worm-hole techniques in the 2-dimensional torus is shown in terms of activity in the routing nodes and experimental performance evaluation. Simulation results on the performance of the four worm-hole algorithms are shown for dynamic injection models. Meaningful comparisons required the equalization of the number of virtual channels for all of the techniques, and this is accomplished by resorting to the concept of lane-channels introduced in [Dal90]. The performance of these schemes is measured for different traffic models: random and bit-reversal. Two worm lengths are tried.

1 Introduction.

Message routing in large interconnection networks has attracted a great deal of interest in recent years. Different underlying machine models and hardware architectures have been used and proposed [DS87], [RBJ88, Ran85], [Upf89, LM89], [Val88], [KS90], [NS87], [Hil85], [CEDK91], [BCC⁺88], [LLK⁺91].

A desirable feature of routing algorithms is adaptivity, i.e., the ability of messages to use alternative paths toward their destinations according to traffic congestion in the nodes of the network. The amount of hardware resources grow with the degree of adaptivity desired, and resources may become critical if deadlock and live-