**TECHNICAL DIGEST** 

# **WIEEE**

international

# ELECTRON DEVICES

meeting

2004

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TECHNICAL DIGEST

# international

# ELECTRON DEVICES

meeting

2004





# 2004 International Electron Devices Meeting TECHNICAL DIGEST

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#### WELCOME FROM THE GENERAL CHAIR

On behalf of the IEDM Committee, I would like to welcome you to the 2004 IEEE International Electron Devices Meeting. This marks our 50<sup>th</sup> annual conference for IEDM, and in recognition of this exciting occasion, special reception and historical poster session will be held on Monday evening. In addition, all of the conference attendees will receive a DVD containing the technical digest contents from the past 50 years. This impressive collection of material illustrates well the pivotal role IEDM has played as the leading forum for the presentation of research and development in the area of electron devices and their applications over the past half century.

The tradition is continuing this year, with a strong collection of invited and contributed papers from over 20 different countries, both from academia and industry. Over 640 abstracts were submitted in total this year, of which the committee accepted 230 for presentation at the conference. Short summaries of each abstract are included on the IEDM home page, and we encourage everyone to visit the site at:

http://www.ieee.org/conference/iedm

In addition to the regular paper sessions, the conference will again feature several special sessions:

On Sunday, two short courses are scheduled titled "45nm CMOS Technology" and "Devices for Next-Generation Digital Consumer Circuits and Systems". They are designed for broad appeal to IEDM participants, with material suitable for both newcomers as well as experts in the field. These courses have been organized by internationally known researchers and will be presented by people active in the respective topics.

The plenary session on Monday will feature a presentation looking back at the conference over the past few decades, "IEDM – a View as a Participant and a Customer," and two presentations looking forward to new challenges for the industry, "Future Semiconductor Manufacturing – Challenges and Opportunities" and "Emerging Technologies on Silicon," with speakers from North America, Asia and Europe.

The IEDM Tuesday Luncheon speaker this year will be Dr. Richard E. Smalley, Rice University professor and Nobel laureate. He will be speaking on "Our Energy Challenge", discussing the formidable task of supplying sufficient, sustainable, clean power to all of the world's people in the 21<sup>st</sup> century.

This year's Emerging Technologies session is titled "Nano-computing Devices." The six invited talks, delivered by experts in their respective fields, will cover a broad range of alternative technologies, ranging from molecules to spin devices to nano-mechanical structures, with a focus on understanding their potential for future logic and computation systems.

On Tuesday night, two timely and provocative panel discussions are planned: "What will end CMOS scaling – Money or Physics?" and, appropriately linked to extend the Emerging Technologies session discussions, "Nanoelectronics – Now or Never?"

On behalf of the IEEE Electron Devices Society, which sponsors the IEDM, Jon Candelaria, Technical Program Chair and Kaizad Mistry, Technical Program Vice-chair, I wish to express my sincere appreciation to the members of the IEDM committee for the outstanding job they have done in planning and organizing the 2004 conference. Likewise, the authors are to be commended for their efforts in preparing and presenting the high-quality papers that form the foundation of the IEDM.

It is with great pleasure that I extend a warm welcome to everyone attending the 2004 IEEE International Electron Devices Meeting, and helping to celebrate our 50<sup>th</sup> year.

Jeffrey Welser General Chair



Jeff Welser General Chair



Jon Candelaria Technical Program Chair



Kaizad Mistry Technical Program Vice-Chair

### The Beginnings of the IEDM

The following are the recollections of R.L. Pritchard, who was actively involved with the very first meetings of what would become the International Electron Devices Meeting:

The driving force for the creation of the Technical Meeting on Electron Devices, as it was then known, was the extremely rapid growth of the solid-state-device field, following the invention of the transistor in 1948. Shortly thereafter, a small device research conference was formed, sponsored by the Institute of Radio Engineers (IRE), one of the predecessors of the IEEE. This conference, which was by-invitation-only, permitted advantageous information interchange among the device-research workers in the field. However, as some of the device research graduated into the device-development arena, there was a need to be able to talk about results to a broader, but still specialized, audience.

Discussions about this need for a new meeting began in the early nineteen fifties with the officers of the IRE Professional Group on Electron Devices (PGED), with support from those with microwave-tube interests, and the concept of a general technical meeting of the IRE PGED emerged. The meeting was planned for two days, in Washington, DC, opening with a general session comprising invited papers, followed by a day and a half of three simultaneous sessions for contributed papers, respectively, on solid-state devices, microwave devices, and electron tubes in general. No exhibits or tutorial sessions were planned, and there were limited social activities; there was only a cocktail party followed by an informal dinner on the first evening. However, a luncheon with an invited speaker was planned for the first day.

The resources for making this meeting a reality came primarily from USA-based industry –e.g., the major manufacturers of electron tubes at that time – and from USA government agencies – which had a strong interest in the emerging solid-state device field as well as that of microwave tubes. (One of the reasons for holding the meeting in Washington, DC was the pool of volunteers available there.) No professional meeting organizers were employed; it was an all volunteer effort.

The first such meeting was held on 24-25 October 1955 (Thursday and Friday) and was very successful, with approximately 700 attendees, and a technical program with approximately 60 papers. Paper selection was done by a Technical Program Committee, with three subcommittees, one for each of the topics of the simultaneous sessions. For each of the nine sessions there was a Session Chair and a Session Organizer. Authors of the papers, for the most part, were from the same sources as cited above for the resources behind the meeting, although there were a few papers from academia.

After the success of the first EDM, it was clear that a need had been established for an annual meeting. Although international participation was welcomed, the first EDM Meetings were primarily USA oriented. Subsequently, the scope of the meetings became more global, and the name was changed to the International Electron Devices Meeting (IEDM).

R. L. Pritchard

Member, Technical Program Committee, First Meeting Chair, Technical Program Committee, Second Meeting

#### AWARD PRESENTATIONS

#### **PLENARY SESSION**

#### Monday, December 13

2003 Roger A. Haken Best Student Paper Award: Yuan Xie, University of Michigan

For the paper entitled: "Novel UHF Micromechanical Extensional Wine-Glass Mode Ring Resonators"

Paul Rappaport Award: Ken Uchida, Junji Koga, Ryuji Ohba and Akira Toriumi, Toshiba Corporation
For the paper entitled: "Programmable Single-Electron Transistor Logic for Future Low-Power Intelligent LSI: Proposal and Room-Temperature Operation"

**EDS George E. Smith Award:** Tomohisa Mizuno, Naoharu Sugiyama, Tsutomu Tezuka and Shinichi Takagi For the paper entitled: "(110) Strained-SOI n-MOSFETs with Higher Electron Mobility"

EDS Chapter of the Year Award: REL/CMPT/ED Singapore Chapter

"To an EDS chapter based on the quantity and quality of the activities and programs implemented by the chapter."

EDS Distinguished Service Award: Louis C. Parrillo, Parrillo Consulting, LLC

"To recognize and honor outstanding service to the Electron Devices Society."

EDS Graduate Student Fellowship Award: HongYu Yu, National University of Singapore and David John, University of British Columbia and Martin von Haartman, KTH, Royal Institute of Technology and David DiSanto, Simon Fraser University

"To promote, recognize, and support graduate level study and research within the Electron Devices Society's field of interest."

J.J. Ebers Award: Jerry Fossum, University of Florida

"For outstanding contributions to the advancement of SOI CMOS devices and circuits through modeling"

#### IEDM Luncheon

#### Tuesday, December 14

2004 IEEE Cledo Brunetti Award: Stephen Y. Chou, Princeton University

"For the invention and development of tools for nanoscale patterning, especially nanoimprint lithography and for the scaling of devices into new physical regimes"

2004 IEEE Andrew S. Grove Award: Krishna C. Saraswat, Stanford University

"For seminal contributions to silicon process technology"

2004 IEEE Daniel E. Noble Award: Larry J. Hornbeck, Texas Instruments

"For his pioneering work and sustained development of the Digital Micromirror Device, used in projection displays"

#### **LUNCHEON PRESENTATION**

Luncheon Presentation: "Our Energy Challenge", Professor Richard Smalley, Rice University

#### **CONFERENCE HIGHLIGHTS**

<u>Date</u>	<u>Time</u>	Room	Event
12/12	9:00 a.m 5:30 p.m.	Continental Ballrooms	Short Courses
12/13	9:00 a.m. – 12:00 p.m.	Continental Ballrooms	Plenary Session
12/13	6:30 p.m. – 9:00 p.m.	Grand Ballroom B	Reception
12/14	12:20 p.m. – 2:00 p.m.	Grand Ballroom B	Luncheon
12/14	8:00 p.m. – 10:00 p.m.	Continental Ballrooms	Panel Sessions

#### **IEDM EXECUTIVE COMMITTEE**

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H.-S. Philip Wong 50th Anniversary Stanford University Stanford, CA

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Melissa Widerkehr Widerkehr and Associates Gaithersburg, MD



Seated from left to right: Clark Nguyen, Emerging Technologies Chair; Melissa Widerkehr, Conference Manager; Kaizad Mistry, Technical Program Vice-Chair; Jeff Welser, General Chair; Jon Candelaria, Technical Program Chair; Veena Misra, Publications Chair; H.S. Philip Wong, 50<sup>th</sup> Anniversary Chair

First row standing from left to right: Coming Chen, Asian Arrangements Chair; Meikei leong, CMOS Devices Subcommittee Chair; Andrea Lacaita, European Arrangements Chair; Thomas Bonifield, Publicity Vice-Chair; Gaudenzio Meneghesso, Quantum Electronics and Compound Semiconductors Chair; Kazunari Ishimaru, Asian Arrangements Chair; Sandip Tiwari, Solid State Devices Chair; Phyllis Mahoney, Conference Manager

Second row standing from left to right: Thomas Skotnicki, European Arrangements Chair; Shou Gwo Woo, Detectors, Sensors and MEMS Subcommittee Chair; Paolo Pavan, CMOS and Interconnect Reliability Subcommittee Chair; Witek Maszara, Integrated Circuits and Manufacturing Subcommittee Chair; Ralf Brederlow; Short Course Vice-Chair; Cliff King, Publicity Chair; Mark Foisy, Modeling and Simulation Subcommittee Chair; Chris Auth, Process Technology Subcommittee Chair (Missing: Vivek Subramanian, Short Course Chair)

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Charles Dachs

Philips Research Leuven

Leuven. Belaium

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- 1.2 Future Semiconductor Manufacturing -Challenges 11 and Opportunities, Hiroshi Iwai, Tokyo Institute of Technology, Yokohama, Japan
- **1.3 Emerging Technologies on Silicon**, Michel **17** Brillouet, CEA/LETI, Grenoble, France

# SESSION 2: Displays, Sensors and MEMS – MEMS Technologies and Applications

Monday, December 13, 1:30 p.m. Continental Ballroom 1-3

Co-Chairs: Darrin Young, Case Western Reserve

University

Jo DeBoeck, IMEC

1:30 p.m. Introduction

1:35 p.m.

2.1 High-Speed MEMS-based Gas Chromatography, M. Agah, G. R. Lambertus, R. D. Sacks, and K. D. Wise, University of Michigan, Ann Arbor, MI

2:00 p.m.

2.2 A Reliable and Compact Polymer-Based Package for Capacitive RF-MEMS Switches, Y. Oya\*, A. Okubora\*, M. Van Spengen, P. Soussan, S. Stoukatch, X. Rottenberg, P. Ratchev, H. Tilmans, W. DeRoedt, E. Beyne, P. De Moor, I. De Wolf, and K. Baert, IMEC, Heverlee, Belgium and \*Sony Corp., Kanagawa, Japan

2:25 p.m.

2.3 A Fully Integrated CMOS and High Voltage Compatible RF MEMS Technology, L. Guan, J. K.O. Sin, H. Liu\*, and Z. Xiong, Hong Kong University of Science and Technology, Clear Water Bay, Hong Kong and \*Cornell University, Ithaca, NY

2.50 p.m.

2.4 Post-Fabrication Laser Trimming of Micromechanical Filters, M. A. Abdelmoneum, M.M. Demirci, S-S Li, C.T.-C. Nguyen, University of Michigan, Ann Arbor, MI

3:15 p.m.

2.5 A Trench-Sidewall Single-wafer-MEMS Technology and its Typical Application in High-Performance Accelerometers, X. Li, B. Cheng, Y. Wang, L. Gu, J. Dong, H. Yang, Z. Song, Chinese Academy of Sciences, Shanghai, China

3:40 p.m.

2.6 An Electrothermally-Actuated, Dual-Mode Micromirror for Large Bi-Directional Scanning, A. Jain, S. Todd, H. Xie, University of Florida, Gainesville, FL

4:05 p.m.

2.7 Novel Ferroelectrics-Based Micro-Acoustic Devices and Their Ultrasonic Applications, Y-P Zhu, T-L Ren, Y. Yang, X.-M. Wu, N.-X. Zhang, L-T Liu, Z.-M. Tan, H.-N. Wang, J. Cai, S.-D. Wang, Z-J Li, Tsınghua Univ., Beijing, Chına

## SESSION 3: Integrated Circuits and Manufacturing – DRAM

Monday, December 13, 1:30 p.m. Continental Ballroom 4

Co-Chairs: Luan Tran, Micron Technology

Harald Seidl, Infineon

1:30 p.m. Introduction

1:35 p.m.

3.1 Highly Scalable Sub-50nm Vertical Double Gate
Trench DRAM Cell, T. Schloesser, D. Manger, R. Weis, S.
Slesazeck, F. Lau, S. Tegen, M. Sesterhenn, K.
Muemmler, J. Nuetzel, D. Temmler, B. Kowalski, U.
Scheler, M. Stavrev, D. Koehler, Infineon Technologies,
Dresden, Germany

2.00 p.m.

3.2 Enhanced Data Retention of Damascene-finFET DRAM with Local Channel Implantation and <100> Fin Surface Orientation Engineering, C. Lee, J-M Yoon, C-H Lee, J.C. Park, T.Y. Kim, H.S. Kang, S.K. Sung, E.S. Cho, H.J. Cho, Y.J. Ahn, D. Park and K. Kim, B.-I. Ryu, Samsung Electronics, Kyoungi-Do, Korea

2:25 p.m.

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3.3 Lattice Strain Design in W/WN/Poly-Si Gate DRAM 65 for Improving Data Retention Time, K. Okonogi, K. Ohyu, A. Toda\* and H. Kobayashi, Elpida Memory, Inc and \*NEC Corporation, Kanagawa, Japan

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2:50 p.m.

3.4 Mechanically Enhanced Storage Node for Virtually Unlimited Height (MESH) Capacitor Aiming at Sub 70nm DRAMs, D.H. Kim, J.Y. Kim, M. Huh, Y.S. Hwang, J.M. Park, D.H. Han, D.I. Kim, M.H. Cho, B.H. Lee, H.K. Hwang, J.W. Song, N.J. Kang, G.W. Ha, S.S. Song, M.S. Shim, S.E. Kim, J.M. Kwon, B.J. Park, H.J. Oh, H.J. Kim, D.S. Woo, M.Y. Jeong, Y.I. Kim, Y.S. Lee, H.J. Kim, J.C. Shin, J.W. Seo, S.S. Jeong, K.H. Yoon, T.H. Ahn, J.B. Lee, Y.W. Hyung, S.J. Park, H.S.Kim, W.T. Choi, G.Y. Jin, Y.G. Park, K. Kim, Samsung Electronics, Kyoungi-do, Korea

3:15 p.m.

3.5 A Highly Manufacturable Deep Trench Based DRAM Cell Layout with a Planar Array Device in a 70nm Technology, J. Amon, A. Kieslich, L. Heineck, T. Schuster J. Faul, J. Luetzen, C. Fan, C.-C. Huang, B. Fischer\*, G. Enders\*, S.Kudelka, U. Schroeder, K.-H. Kuesters, G. Lange\*, J. Alsmeier\*, Infineon Technologies AG, Dresden, Germany and \*Munich, Germany

# SESSION 4: Process Technology – Fully-Silicided (FUSI) Gates

Monday, December 13, 1:30 p.m. Continental Ballroom 5

Co-Chairs: Jakub Kedzierski, IBM TJ Watson

Gyoyoung Jin, Samsung Electronics

1:30 p.m Introduction

1:35 p.m.

4.1 Advanced Gate Stacks with Fully Silicided (FUSI) Gates and High-k Dielectrics: Enhanced Performance at Reduced Gate Leakage, E.P. Gusev, C. Cabral, Jr., B.P. Linder, Y.H. Kim, K. Maitra, E. Cartier, H. Nayfeh\*, R. Amos\*, G. Biery, N. Bojarczuk, A. Callegari, R. Carruthers, S.A. Cohen, M. Copel, M.M. Frank, S. Fang\*, S. Guha, M. Gribelyuk, P. Jamison, R. Jammy, M. Ieong, J. Kedzierski, P. Kozlowski, V. Ku\*, D. Lacey, D. LaTulipe, V. Narayanan, H. Ng\*, P. Nguyen\*, J. Newbury, V. Paruchuri, R. Rengarajan\*, G. Shahidi, A. Steegen\*, M. Steen, S. Zafar and Y. Zhang, IBM SRDC, Yorktown Heights, NY and \* IBM Microelectronic Division, Hopewell Junction, NY

2:00 p.m.

4.2 Partial Silicides Technology for Tunable Work Function Electrodes on High-k Gate Dielectrics-Fermi Level Pinning Controlled PtSi<sub>x</sub> for HFO<sub>x</sub> (N) pMOSFET, T. Nabatame, M. Kadoshima, K. Iwamoto, N. Mise, S. Migita\*, M. Ohno, H. Ota\*, N. Yasuda, A. Ogawa, K. Tominaga, H. Satake and A. Toriumi\*, ASET, Tsukuba, Japan and \*AIST, Tsukuba, Japan

2:25 p.m.

4.3 Work Function Tuning Through Dopant Scanning and Related Effects Ni Fully Silicided Gate for Sub-45nm Nodes CMOS, D Aimé, B. Froment, F. Cacho, V Carron\*, S. Descombes, Y. Morand, N. Emonet, F. Wacquant, T. Farjot\*, S. Jullian\*\*, C. Laviron\*, M. Juhel, R. Pantel, R. Molins#, D. Delille, A. Halimaoui, D. Bensahel, A. Souifi^, STMicroelectronics, Crolles, France and \*CEA-LETI, \*\*Philips Semiconductor, Crolles France and #Centre des Materiaux Pierre-Marie Fourt, Evry, France and ^LPM-CNRS, Villeurbanne, France

2:50 p.m.

4.4 Dual Workfunction Ni-Silicide/HfSiON Gate Stacks by Phase-Controlled Full-Silicidation (PC-FUSI) Technique for 45nm-node LSTP and LOP Devices, K. Takahashi, K. Manabe, T. Ikarashi, N. Ikarashi, T. Hase, T. Yoshihara, H. Watanabe, T. Tatsumi, and Y. Mochizuki, NEC Corporation, Kanagawa, Japan

3:15 n m

4.5 Proposal of New HfSiON CMOS Fabrication Process (HAMDAMA) for Low Standby Power Device, T. Aoyama, T. Maeda, K. Torii, K. Yamashita, Y. Kobayashi, S. Kamiyama, T. Miura, H. Kitajima and T. Arikado, Selete, Tsukuba, Japan

3:40 p.m.

4.6 Diffusion-less Junctions and Super Halo Profiles for PMOS Transistors Formed by SPER and FUSI Gate in 45 nm Physical Gate Length Devices, S. Severi, K. G. Anil, J. B. Pawlak\*, R. Duffy\*, K. Henson, R. Lındsay\*\*, A. Lauwers, A. Veloso, J.-F. de Marneffe, J. Ramos, B. Sijmus, K. Devriendt, R.A. Camillo-Castillo^, P. Eyben, W. Vandervost, M. Jurczak, S. Biesemans and K. De Meyer, IMEC, Leuven, Belgium, \*Philips Research Leuven, Heverlee, Belgium and \*\*Infineon, Munich, Germany and \*University of Florida, Gainesville, FL

# SESSION 5: CMOS and Interconnect Reliability – NBTI Effect in Conventional and High-k Dielectrics

Monday, December 13, 1:30 p.m. Continental Balfroom 6

Co-Chairs: Muhammad Ashraful Alam, Purdue

University

Samuel Pan, TSMC

1:30 p.m. Introduction

1:35 p m.

5.1 Mechanism of Negative Bias Temperature Instability in CMOS Devices: Degradation, Recovery and Impact of Nitrogen (Invited), S. Mahapatra, M.A. Alam\*, P. Bharath Kumar, T. R. Dalei and D. Saha, Indian Institute of Technology, Bombay, India, and \*Purdue University. West Lafavette. IN

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125

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2:00 p m.

5.2 'On-the-fly" Characterization of NBTI in Ultra-Thin Gate-Oxide PMOSFETs, M. Denais , A. Bravaix\*\*, V. Huard\*, C. Parthasarathy, G. Ribes, F. Perrier\*, Y. Rey-Tauriac and N. Revil, STMicroelectronics, Crolles, France, \*Philips Semiconductors, Crolles, France, \*\*UMR CNRS, Toulon, France

2:25 p.m.

5.3 A Geometrical Unification of the Theories of MBTI and HCI Time-Exponents and Its Implications for Ultra-Scaled Planar and Surround Gate MOSFETs, H. Kufluoglu, M. Alam, Purdue University, West Lafayette, IN

2:50 p.m

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5.4 Influence of Nitrogen in Ultra-thin SiON on Negative Bias Temperature Instability under AC Stress, Y. Mitani, Toshiba Corporation, Yokohama, Japan

3:15 p m.

5.5 Negative Bias Temperature Instabilities in 121 HfSiON/TaN-Based pMOSFETs, M. Houssa, M. Aoulaiche, S Van Elshocht, S. De Gendt, G. Groeseneken, and M. Heyns, IMEC, Leuven, Belgium

3:40 p.m

5.6 HCl and BTI Characteristics of ALD HfSiO(N) Gate Dielectrics as the Compositions and the Post Treatment Conditions, J.P. Kim, Y.-S. Kim, H.J. Lim, J.H. Lee, S. J. Doh, H.-S. Jung, S.-K. Han, M.-J Kim, J.-H. Lee, N.-I. Lee, H.-K. Kang, K.-P. Suh, and Y.-S. Chung\*, Samsung Electronics Co., Kyoungi-Do, Korea and \*Samsung Advanced Institute of Technology

4:05 p.m.

5.7 Physical Model of BTI, TDDB and SILC in HfO<sub>2</sub>-Based High-k Gate Dielectrics, K. Torii, K. Shiraishi\*, S. Miyazaki\*\*, K. Yamabe\*, M. Boero\*, T. Chikyow\*\*\*, K. Yamada\*\*\*, H. Kitajima, and T. Arikado, Selete, Ibaraki, Japan, \*University of Tsukuba, Ibaraki, Japan, \*\*Hiroshima University, Hiroshima, Japan, \*\*\*National Institute for Materials Science, Tsukuba, Japan

# SESSION 6: Modeling and Simulation – Transport in Nanoscale Silicon-Based FETs – I

Monday, December 13, 1:30 p.m. Continental Ballroom 7-9

Co-Chairs: Mark Stettler, Intel

Enrico Sangiorgi, University of Bologna

1:30 p.m. Introduction

1:35 p.m

6.1 Simulation Study of Ge n-channel 7.5 nm DGFETs of Arbitrary Crystallographic Alignment, S. E. Laux, IBM T.J. Watson Research Center, Yorktown Heights, NY

2:00 p.m.

6.2 Bandstructure Effects in Ballistic Nanoscale
MOSFETs, A. Rahman, G. Klimeck, T. Boykin\* and M.
Lundstrom, Purdue University, West Lafayette, IN and
\*University of Alabama, Huntsville, AL

2:25 p.m.

**6.3** Relevance of Remote Scattering in Gate to Channel Mobility of Thin-Oxide CMOS Devices, P.M. Solomon and M. Yang, IBM T.J. Watson Research Center, Yorktown Heights, NY

2:50 p.m.

**6.4 Quantum Mechanical Calculation of Hole Mobility** in Silicon Inversion Layers Under Arbitrary Stress, E. Wang\*, P. Matagne, L. Shifren, B. Obradovic, R. Kotlyar, S. Cea, J. He, Z. Ma, R. Nagisetty, S. Tyagi, M. Stettler and M.D.Giles, Intel Corporation, Hillsboro, OR and \*Santa Clara, CA

3:15 p.m.

**6.5 Impact of Surface Roughness on Silicon and Germanium Ultra-Thin-Body MOSFETs,** T. Low, M.F. Li, W.J. Fan\*, S.T. Ng\*, Y.-C. Yeo, C. Zhu, A. Chin\*\*\*, L. Chan\*\* and D.L. Kwong\*\*\*, National University of Singapore, Singapore, \*Nanyang Technological University, Singapore, \*\*Chartered Semiconductor Manufacturing, Singapore, \*\*\*University of Texas, Austin, TX

#### SESSION 7: CMOS Devices - Strained Silicon I

Monday, December 13, 1:30 p.m. Imperial Baliroom A

Co-Chairs: Kelin Kuhn, Intel

Manoj Mehrotra, Texas Instruments

1.30 p.m. Introduction

1:35 p.m.

7.1 Selectively Formed High Mobility Strained Ge PMOSFETs for High Performance CMOS, H. Shang, J. Chu, S. Bedell, E. P. Gusev, P. Jamison\*, Y. Zhang, J. Ott, M. Copel, D. Sadana, K. Guarini and M. leong, IBM SRDC, Yorktown Heights, NY and \*Hopewell Junction, NY

2:00 p.m.

**7.2 Low Power Device Technology with SiGe Channel, HfSiON, and Poly-Si Gate,** H.C.-H. Wang, S.-J. Chen, M.-F. Wang, P.-Y. Tsai, C.-W. Tsai, T.-W. Wang, S.M. Ting, T.-H. Hou, P.-S. Lim, H.-J. Lin, Y. Jin, H.-J. Tao, S.-C. Chen, C.H. Diaz, M.-S. Liang, and C. Hu, TSMC, Taiwan, ROC

2:25 p.m.

7.3 Performance Comparison and Channel Length Scaling of Strained Si FETs on SiGe-on-Insulator (SGOI), J. Cai, K. Rim, A. Bryant, K. Jenkins, C. Ouyang, D. Singh, Z. Ren\*, K. Lee, H. Yin\*, J. Hergenrother, T. Kanarsky\*, A. Kumar, X. Wang\*, S. Bedell, A. Reznicek, H. Hovel, D. Sadana, D. Uriarte\*, R. Mitchell\*, J. Ott, D. Mocuta\*, P. O'Neil\*, A. Mocuta\*, E. Leobandung\*, R. Miller, W. Haensch and M. leong\*, IBM SRDC, Yorktown Heights, NY, \*IBM Microelectronics Division, Hopewell Junction, NY

2:50 p.m.

7.4 Impact of Parasitic Resistance and Silicon Layer Thickness Scaling for Strained-Silicon MOSFETs on Relaxed Si<sub>1-x</sub>Ge<sub>x</sub> Virtual Substrate, H. Kawasaki, K. Ohuchi, A. Oishi, O. Fujii, H. Tsujii, T. Ishida, K. Kasaı, Y. Okayama, K. Kojima, K. Adachi, N. Aoki, T. Kanemura, D. Hagishıma\*, M. Fujiwara, S. Inaba, K. Ishimaru, N. Nagashima\*\* and H. Ishiuchi, Toshiba Corporation Semiconductor Company, Kanagawa, Japan, \*Toshiba Corporation, Yokohama, Japan, \*\*Sony Corporation, Japan

3.15 p.m.

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7.5 High Electron and Hole Mobility Enhancements in Thin-Body Strained Si/Strained SiGe/Strained Si Heterostructures on Insulator, I. Åberg, C. Ní Chléirigh, O. Olubuyide, X. Duan and J. Hoyt, MIT, Cambridge, MA

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3:40 p.m

7.6 Performance Enhancement of Partially- and Fully-Depleted Strained-SOI MOSFETs and Characterization of Strained-Si Device Parameters, T. Numata, T. Irisawa, T. Tezuka, J. Koga, N. Hirashita, K. Usuda, E. Toyoda\*, Y. Miyamura\*\*, A. Tanabe, N. Sugiyama, and S. Takagi\*\*\*, MIRAI-ASET, Kanagawa, Japan, \*Toshiba Ceramics, \*\*Komatsu Electronic Metals, \*\*\*MIRAI-AIST, Japan

4.05 p.m.

7.7 3D GOI CMOSFETs with Novel IrO<sub>2</sub>(Hf) Dual Gates and High-k Dielectric on 1P6M-0.18µm-CMOS, D. S. Yu, A. Chin\*, C. C. Laio, C.F. Lee, C.F. Cheng, W. J. Chen\*\*, C. Zhu\*, M.-F. Li\*, W.J. Yoo\*, S.P. McAlister^, and D. L. Kwong\*\*\*, National Chiao Tung University, Hsinchu, Taiwan, ROC, \*National University of Singapore, Singapore, \*\*National Pingtung University of Science and Techology, Pingtung, Taiwan and ^National Research Council of Canada, Ottawa, Canada and\*\*\*The University of Texas, Austin, TX

# SESSION 8: Solid State Devices – Room Temperature Single Electronics and Tunneling Devices

Monday, December 13, 1:30 p.m. Imperial Ballroom B

Co-Chairs: Zoran Krivokapic, AMD

Adrian Ionescu, EPFL

1.30 p.m Introduction

1:35 p.m.

8.1 Room-Temperature Demonstration of Integrated Silicon Single-Electron Transistor Circuits for Current Switching and Analog Pattern Matching, M. Saitoh, H. Harata, and T. Hiramoto, University of Tokyo, Tokyo, Japan

2:00 p.m.

8.2 Transistor in a Test Tube - Harnessing Molecular Biology to the Self-Assembly of Molecular Scale Electronics (Invited), U. Sivan, K. Keren, E. Braun, R. Berman and E. Buchstab, Technion-Israel Institute of Technology, Haifa, Israel

2:25 p.m.

8.3 The Tunneling Field Effect Transistor (TFET) as an Add-on for Ultra-Low-Voltage Analog and Digital Processes, Th. Nirschl, P.-F. Wang, C. Weber\*, J. Sedlmeir\*, R. Heinrich\*, R. Kakoschke\*, K. Schrufer\*, J. Holz\*, C. Pacha\*, T. Schulz\*, M. Ostermayr\*, A. Olbrich\*, G. Georgakos\*, E. Ruderer\*, W. Hansch, D. Schmitt-Landsiedel, Technical University, Munich, Germany and \*Infineon Technologies, Munich, Germany

2:50 p.m

8.4 Room-Temperature Single-Electron Transfer and Detection with Silicon Nanodevices, K. Nishiguchi, A. Fujiwara, Y. Ono, H. Inokawa, and Y. Takahashi, NTT Corporation, Kanagawa, Japan

3:15 p.m.

8.5 80nm Self-Aligned Complementary I-MOS Using Double Sidewall Spacer and Elevated Drain Structure and Its Applicability to Amplifiers with High Linearity, W.Y. Choi, J.Y. Song, B.Y. Choi, J.D. Lee, Y.J. Park, and B.-G. Park, Seoul National University, Seoul, Korea