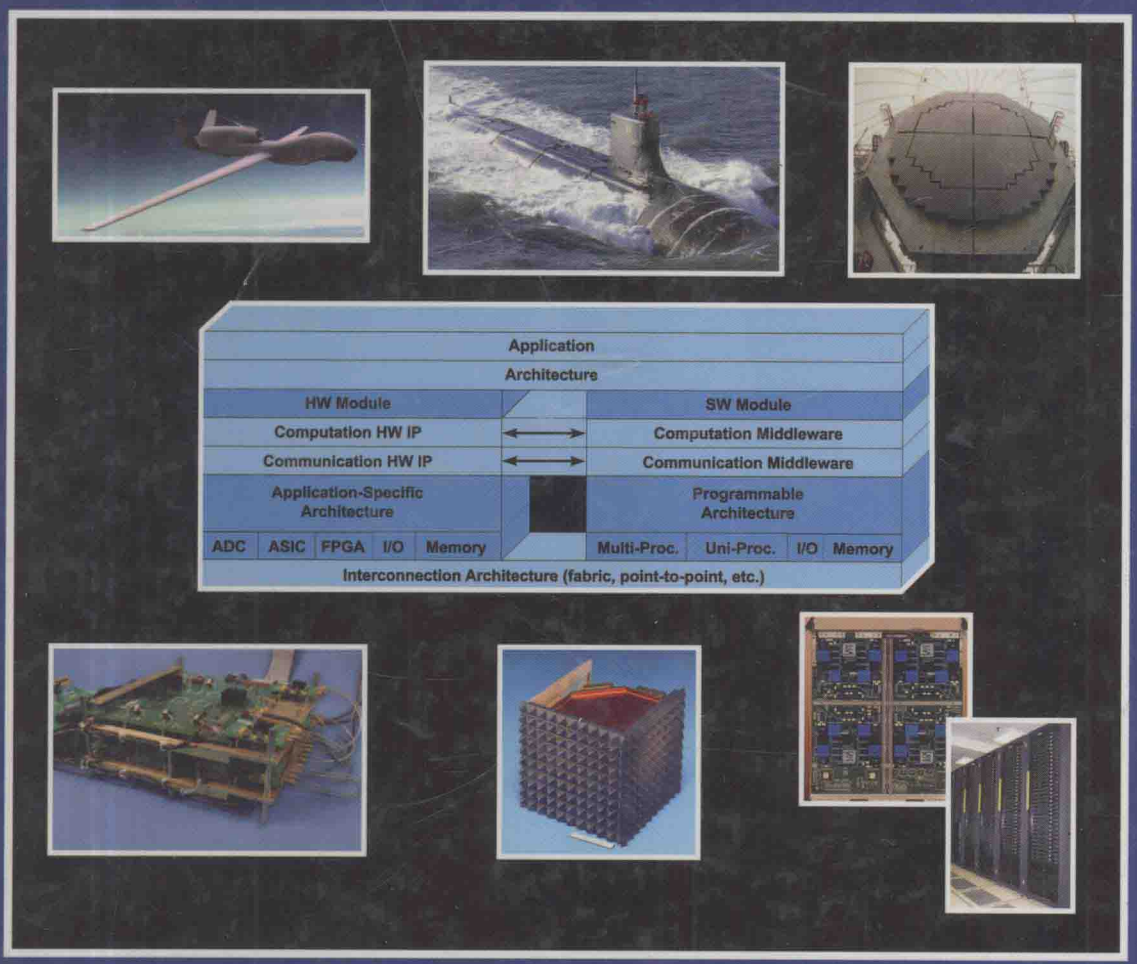
High Performance Embedded Computing Handbook

A Systems Perspective



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Dedication

This handbook is dedicated to MIT Lincoln Laboratory for providing the opportunities to work on exciting and challenging hardware and software projects leading to the demonstration of high performance embedded computing systems.

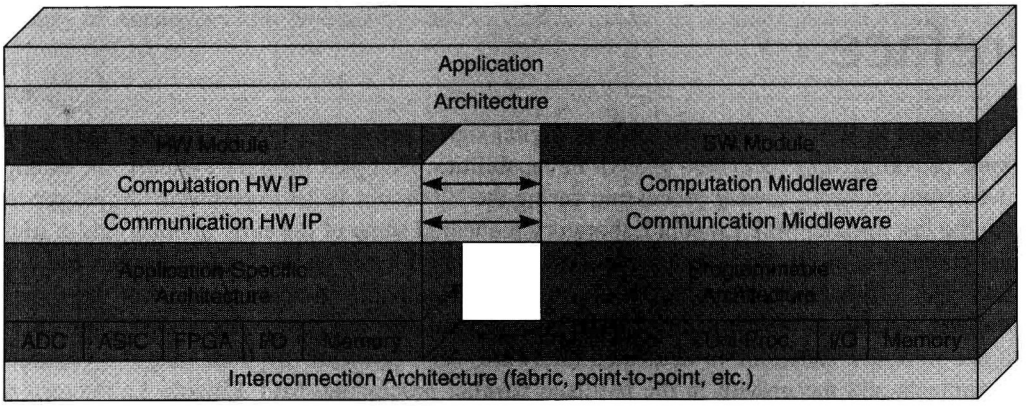
Preface

Over the past several decades, advances in digital signal processing have permeated many applications, providing unprecedented growth in capabilities. Complex military systems, for example, evolved from primarily analog processing during the 1960s and 1970s to primarily digital processing in the last decade. MIT Lincoln Laboratory pioneered some of the early applications of digital signal processing by developing dedicated processing performed in hardware to implement application-specific functions. Through the advent of programmable computing, many of these digital processing algorithms were implemented in more general-purpose computing while still preserving compute-intensive functions in dedicated hardware. As a result of the wide range of computing environments and the growth in the requisite parallel processing, MIT Lincoln Laboratory recognized the need to assemble the embedded community in a yearly national event. In 2006, this event, the High Performance Embedded Computing (HPEC) Workshop, marked its tenth anniversary of providing a forum for current advances in HPEC. This handbook, an outgrowth of the many advances made in the last decade, also, in several instances, builds on knowledge originally discussed and presented by the handbook authors at HPEC Workshops. The editors and contributing authors believe it is important to bring together in the form of a handbook the lessons learned from a decade of advances in high performance embedded computing.

This HPEC handbook is best suited to systems engineers and computational scientists working in the embedded computing field. The emphasis is on a systems perspective, but complemented with specific implementations starting with analog-to-digital converters, continuing with front-end signal processing addressing compute-intensive operations, and progressing through back-end processing requiring intensive parallel and programmable processing. Hardware and software engineers will also benefit from this handbook since the chapters present their subject areas by starting with fundamental principles and exemplifying those via actual developed systems. The editors together with the contributing authors bring a wealth of practical experience acquired through working in this field for a span of several decades. Therefore, the approach taken in each of the chapters is to cover the respective system components found in today's HPEC systems by addressing design trade-offs, implementation options, and techniques of the trade and then solidifying the concepts through specific HPEC system examples. This approach provides a more valuable learning tool since the reader will learn about the different subject areas by way of factual implementation cases developed in the course of the editors' and contributing authors' work in this exciting field.

Since a complex HPEC system consists of many subsystems and components, this handbook covers every segment based on a canonical framework. The canonical framework is shown in the following figure. This framework is used across the handbook as a road map to help the reader navigate logically through the handbook.

The introductory chapters present examples of complex HPEC systems representative of actual prototype developments. The reader will get an appreciation of the key subsystems and components by first covering these chapters. The handbook then addresses each of the system components shown in the aforementioned figure. After the introductory chapters, the handbook covers computational characteristics of high performance embedded algorithms and applications to help the reader understand the key challenges and recommended approaches. The handbook then proceeds with a thorough description of analog-to-digital converters typically found in today's HPEC systems. The discussion continues into front-end implementation approaches followed by back-end parallel processing techniques. Since the front-end processing is typically very compute-intensive, this part of the system is best suited for VLSI hardware and/or field programmable gate arrays. Therefore, these subject areas are addressed in great detail.



Canonical framework illustrating key subsystems and components of a high performance embedded computing (HPEC) system.

The handbook continues with several chapters discussing candidate back-end implementation techniques. The back-end of an HPEC system is often implemented using a parallel set of high performing programmable chips. Thus, parallel processing technologies are discussed in significant depth. Computing devices, interconnection fabrics, software architectures and metrics, plus middleware and portable software, are covered at a level that practicing engineers and HPEC computational practitioners can learn and adapt to suit their own implementation requirements. More and more of the systems implemented today require an open system architecture, which depends on adopted standards targeted at parallel processing. These standards are also covered in significant detail, illustrating the benefits of this open architecture trend.

The handbook concludes with several chapters presenting application examples ranging from electro-optics, sonar surveillance, communications systems, to advanced radar systems. This last section of the handbook also addresses future trends in high performance embedded computing and presents advances in microprocessor architectures since these processors are at the heart of any future HPEC system.

The HPEC handbook, by leveraging the contributors' many years of experience in embedded computing, provides readers with the requisite background to effectively work in this field. It may also serve as a reference for an advanced undergraduate course or a specialized graduate course in high performance embedded computing.

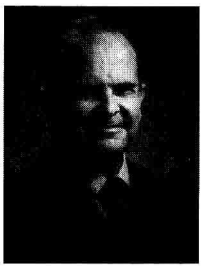
David R. Martinez
Robert A. Bond
M. Michael Vai

Acknowledgments

This handbook is the product of many hours of dedicated efforts by the editors, authors, and production personnel. It has been a very rewarding experience. This book would not have been possible without the technical contributions from all the authors. Being leading experts in the field of high performance embedded computing, they bring a wealth of experience not found in any other book dedicated to this subject area.

We would also like to thank the editors' employer, MIT Lincoln Laboratory; many of the subjects and fundamental principles discussed in the handbook stemmed from research and development projects performed at the Laboratory in the past several years. The Lincoln Laboratory management wholeheartedly supported the production of this handbook from its start. We are especially grateful for the valuable support we received during the preparation of the manuscript. In particular, we would like to thank Mr. David Granchelli and Ms. Dorothy Ryan. Dorothy Ryan patiently edited every single chapter of this book. David Granchelli coordinated the assembling of the book. Also, many thanks are due to the graphics artists—Mr. Chet Beals, Mr. Henry Palumbo, Mr. Art Saarinen, and Mr. Newton Taylor. The graphics work flow was supervised by Mr. John Austin. Many of the chapters were proofread by Mrs. Barbra Gottschalk. Finally, we would like to thank the publisher, Taylor & Francis/CRC Press, for working with us in completing this handbook. The MIT Lincoln Laboratory Communications Office, editorial personnel, graphics artists, and the publisher are the people who transformed a folder of manuscript files into a complete book.

About the Editors

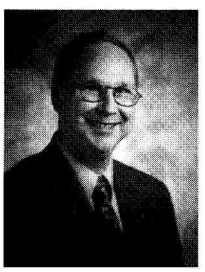


Mr. David R. Martinez is Head of the Intelligence, Surveillance, and Reconnaissance (ISR) Systems and Technology Division at MIT Lincoln Laboratory. He oversees more than 300 people and has direct line management responsibility for the division's programs in the development of advanced techniques and prototypes for surface surveillance, laser systems, active and passive adaptive array processing, integrated sensing and decision support, undersea warfare, and embedded hardware and software computing.

Mr. Martinez joined MIT Lincoln Laboratory in 1988 and was responsible for the development of a large prototype space-time adaptive signal processor. Prior to joining the Laboratory, he was Principal Research Engineer at ARCO Oil and Gas Company, responsible for a multidisciplinary company project to demonstrate the viability of real-time adaptive signal processing techniques. He received the ARCO special achievement award for the planning and execution of the 1986 Cuyama Project, which provided a superior and cost-effective approach to three-dimensional seismic surveys. He holds three U.S. patents.

Mr. Martinez is the founder, and served from 1997 to 1999 as chairman, of a national workshop on high performance embedded computing. He has also served as keynote speaker at multiple national-level workshops and symposia including the Tenth Annual High Performance Embedded Computing Workshop, the Real-Time Systems Symposium, and the Second International Workshop on Compiler and Architecture Support for Embedded Systems. He was appointed to the Army Science Board from 1999 to 2004. From 1994 to 1998, he was Associate Editor of the *IEEE Signal Processing* magazine. He was elected an IEEE Fellow in 2003, and in 2007 he served on the Defense Science Board ISR Task Force.

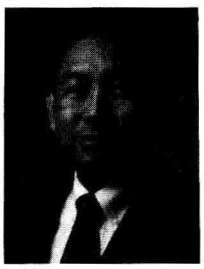
Mr. Martinez earned a bachelor's degree from New Mexico State University in 1976, an M.S. degree from the Massachusetts Institute of Technology (MIT), and an E.E. degree jointly from MIT and the Woods Hole Oceanographic Institution in 1979. He completed an M.B.A. at the Southern Methodist University in 1986. He has attended the Program for Senior Executives in National and International Security at the John F. Kennedy School of Government, Harvard University.



Mr. Robert A. Bond is Leader of the Embedded Digital Systems Group at MIT Lincoln Laboratory. In his career, he has focused on the research and development of high performance embedded processors, advanced signal processing technology, and embedded middleware architectures. Prior to coming to the Laboratory, Mr. Bond worked at CAE Ltd. on radar, navigation, and Kalman filter applications for flight simulators, and then at Sperry, where he developed simulation systems for a Naval command and control application.

Mr. Bond joined MIT Lincoln Laboratory in 1987. In his first assignment, he was responsible for the development of the Mountaintop RSTER radar software architecture and was coordinator for the radar system integration. In the early 1990s, he was involved in seminal studies to evaluate the use of massively parallel processors (MPP) for real-time signal and image processing. Later, he managed the development of a 200 billion operations-per-second airborne processor, consisting of a 1000-processor MPP for performing radar space-time adaptive processing and a custom processor for performing high-throughput radar signal processing. In 2001, he led a team in the development of the Parallel Vector Library, a novel middleware technology for the portable and scalable development of high performance parallel signal processors.

In 2003, Mr. Bond was one of two researchers to receive the Lincoln Laboratory Technical Excellence Award for his "technical vision and leadership in the application of high-performance embedded processing architectures to real-time digital signal processing systems." He earned a B.S. degree (honors) in physics from Queen's University, Ontario, Canada, in 1978.



Dr. M. Michael Vai is Assistant Leader of the Embedded Digital Systems Group at MIT Lincoln Laboratory. He has been involved in the area of high performance embedded computing for over 20 years. He has worked and published extensively in very-large-scale integration (VLSI), application-specific integrated circuits (ASICs), field programmable gate arrays (FPGAs), design methodology, and embedded digital systems. He has published more than 60 technical papers and a textbook (*VLSI Design*, CRC Press, 2001). His current research interests include advanced signal processing algorithms and architectures, rapid prototyping methodologies, and anti-tampering techniques.

Until July 1999, Dr. Vai was on the faculty of the Electrical and Computer Engineering Department, Northeastern University, Boston, Massachusetts. At Northeastern University, he developed and taught the VLSI Design and VLSI Architecture courses. He also established and supervised a VLSI CAD laboratory. In May 1999, the Electrical and Computer Engineering students presented him with the Outstanding Professor Award. During his tenure at Northeastern University, he performed research programs funded by the National Science Foundation (NSF), Defense Advanced Research Projects Agency (DARPA), and industry.

After joining MIT Lincoln Laboratory in 1999, Dr. Vai led the development of several notable real-time signal processing systems incorporating high-density VLSI chips and FPGAs. He coordinated and taught a VLSI Design course at Lincoln Laboratory in 2002, and in April 2003, he delivered a lecture entitled "ASIC and FPGA DSP Implementations" in the IEEE lecture series, "Current Topics in Digital Signal Processing." Dr. Vai earned a B.S. degree from National Taiwan University, Taipei, Taiwan, in 1979, and M.S. and Ph.D. degrees from Michigan State University, East Lansing, Michigan, in 1985 and 1987, respectively, all in electrical engineering. He is a senior member of IEEE.

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