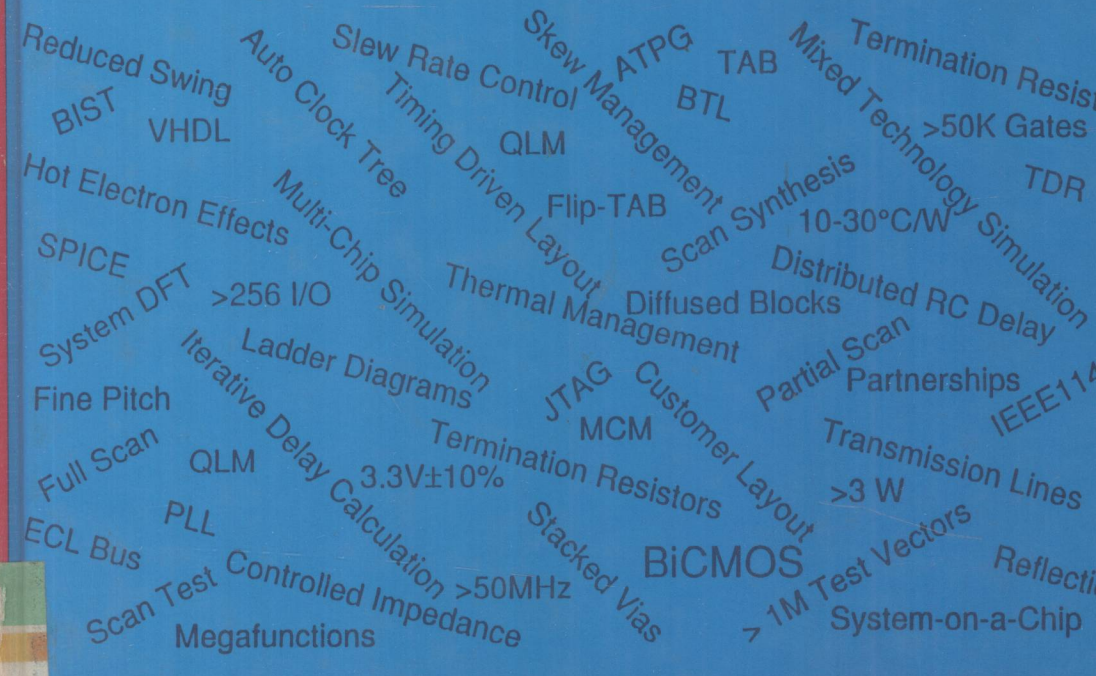
Designing with High Performance ASICs

Joseph Di Giacomo



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Joseph Di Giacomo
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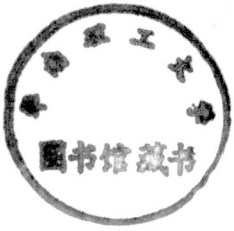

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Preface

ASIC (application-specific integrated circuit) technology has emerged as a technique and a philosophy by which companies can customize products in both a cost- and time-effective manner. Computer-aided design and computer-aided manufacturing tools have made ASIC a reality.

In the past, IC circuits were designed and developed by integrated-circuit specialists. Significant design skills were required to undertake and complete a design. With the advent of computer-aided-design (CAD) tools and user-friendly interfaces, many more people are now involved in design.

However, there's a need to tutor "design" people in the basic concepts, principles, and methods of high-performance ASIC design. Somehow in perfecting a design system in which the computer checks and verifies an ASIC design and does all the thinking and work, a significant gap now exists in understanding the basic principles of high-performance ASIC design. In most cases, when a design does not work the vendor is blamed. The inexperience of the designer is rarely questioned.

The purpose of this book is to present the fundamental principles of high-performance ASIC design in a clear manner and related to specific examples. This book saves designers time and work, reduces the overall cost of a design, and stimulates the creative aspect of the design.

Many design illustrations contained in this text use specific numbers from real products. Although illustrations use specific numbers, they are meant to illustrate fundamental procedures and concepts. The calculations do not necessarily reflect current technologies nor are they appropriate for

all products. Not all vendors supply the same type of data or allow designers the same level of control over their designs.

I would like to express my grateful appreciation to Dick Grossman and John Carey of Motorola for making this project a reality; to Tim Boland, Bill Blood, Jerry Prioste, Dave Pivin, Ruth Waterman Massey, Clarence Nakata, and Philip Rudnick of Motorola, whose material was used to generate the book; and to all those who reviewed the book and to all who helped in the preparation of the manuscript.

Joseph Di Giacomo

Symbols

Ci (DD.32, p. 97). The capacitance associated with the input of an internal logic macro.

Cin (DD.31, p. 97). The input capacitance associated with the input of an input buffer.

Cout (DD.33, p. 97). The capacitance associated with the output of an output buffer.

fmax. The maximum rate at which clock pulses meeting the clock requirements may be applied to a sequential circuit.

Idd (CMD-1, p. 97). The quiescent positive supply current that flows into the Vdd pins of a cell when none of the internal nodes is being switched.

Iin. The input leakage current. This is the maximum input leakage current flowing into and out of a buffer under the specified conditions.

Ioh. The minimum current of the output buffers. This is the guaranteed minimum current flowing from an output buffer at the specified voltage level for the indicated buffer type and the indicated conditions.

Iol. The maximum current of the output buffers. This is the guaranteed maximum current flowing into an output buffer at the specified voltage level for the indicated buffer type and the indicated conditions.

Iqz. The output leakage current. This is the maximum output leakage current of an output buffer in the high-impedance state under the specified conditions.

Iss (CMD-2, p. 97). The quiescent negative supply current that flows out of the Vss pins when no internal pins are switching.

Tf. The signal fall time for a high-to-low logic transition.

Th. The minimum time during which the data to be recognized must remain constant after the specified edge of the control signal (clock) to ensure proper data recognition.

Tphl. The high-to-low propagation delay.

Tplh. The low-to-high propagation delay.

Tr. The signal rise time for a low-to-high logic transition.

Trec. The amount of time between the disabling edge of the asynchronous signal (set, reset, load) and the enabling edge of a synchronous signal (clock).

Tsu. The minimum time during which data to be recognized must remain constant prior to the specified edge of the control signal to ensure proper data recognition.

Twh. The time between the 50% point of the rising edge and the 50% point of the falling edge of a pulse.

Twl. The time between the 50% point of the falling edge and the 50% point of the rising edge of a pulse.

Variables, logic (DD.26, p. 96). Logic macro specific variables:
K1: loading constant, rising
K2: loading constant, falling
IPC: input capacitance for a given input pin
K3: output edge rate, rising slope
K4: output edge rate, falling slope
K7: input edge-rate sensitivity, rising for $<$ 5ns.
K8: input edge-rate sensitivity, falling for $>$ 5ns.
K9: input edge-rate sensitivity, rising for $>$ 5ns.
K10: input edge-rate sensitivity, falling for $<$ 5ns.

Vdd (DD.20, p. 96). The positive power supply voltage.

Vih (DD.22, p. 96). The minimum voltage that represents a logic High at an input.

Vil (DD.23, p. 96). The maximum voltage that represents a logic Low at an input.

Voh (DD.24, p. 96). The minimum voltage at an output terminal for the specified output current.

Vol (DD.25, p. 96). The maximum voltage at an output terminal for the specified output current.

Vss (DD.21, p. 96). The negative power supply voltage (ground).

Contents

1

Introduction

1.1 PURPOSE OF THE BOOK

The purpose of this book is to present the fundamental principles of high-performance ASIC design, in a clear manner and related to specific examples. This book saves designers time and work, reduces the overall cost of a design, and stimulates the creative aspect of the design.

The specific intention of the material is

- to provide rules for measuring ASIC performance
- to show specific examples of ASIC designs
- to focus on basic principles and techniques
- to follow a step-by-step procedure to accomplish a successful design

1.2 EXPECTED LEARNING OUTCOME

The material of this book is meant for ASIC designers, senior engineering students, and graduate students. There is an obvious outcome of exposing readers to this material, testing them in this material, and bringing them to a new level of knowledge.

I would like to bring the readers of this book to a syntopical level of understanding. That is, upon completing the studying of this material, readers should accomplish the following:

- state their ASIC problems in a succinct manner
- understand ASIC technical terms, language, and procedures associated with the material
- ask intelligent questions about ASIC high performance and ask those questions in the right order
- understand the pros and cons of an ASIC discussion
- analyze a technical discussion on ASIC parameters and be objective in reaching a solution to the problem
- do high-performance ASIC design

1.3 ASIC DESIGN ENVIRONMENT AND ISSUES

1.3.1 ASIC Design Today

ASIC design today is depicted by a plethora of buzz words and characteristics, as shown in Figure 1.1. Terms such as skew, back annotation, turnkey, scan, and EDIF can be readily learned and understood. As ASIC pushes into the high-performance/submicron world, additional terms (Figure 1.2) such as ladder diagrams, RC delay, timing driven layout, and skew management must also be understood and mastered. This book uses an expanded index and glossary to help designers locate specific design terms and topics. It is a working reference to the design process.

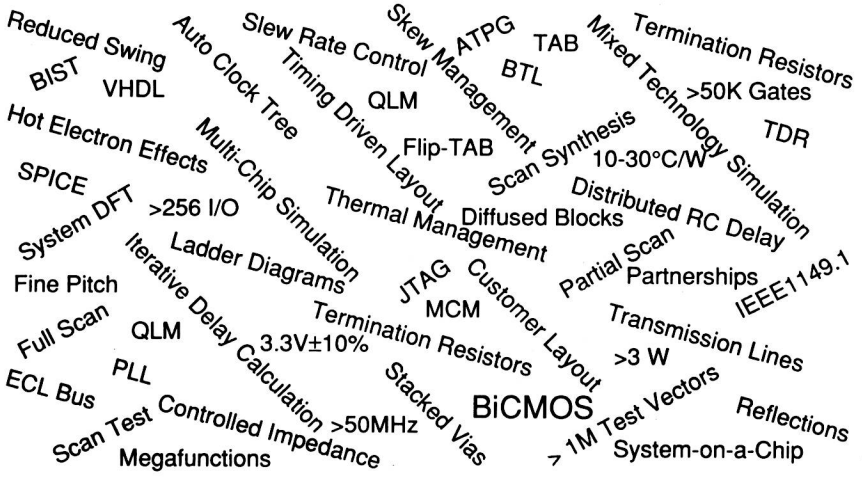

Figure 1.1 ASIC design today is depicted by these buzz words and characteristics.

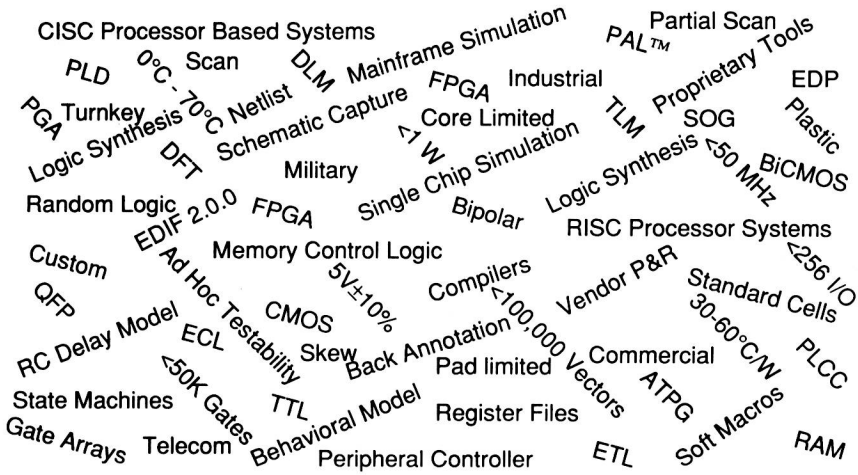

Figure 1.2 The submicron world is all of the previous and these, too.

1.3.2 ASIC New Capabilities and Benefits

With the advent of high-performance/submicron technology, new capabilities and benefits are possible in circuit design. For example:

- higher-speed circuits are achievable by the use of 0.8-micron CMOS/BiMOS technology
- higher levels of integration and complexity are possible with up to 300K gates available
- architectural changes, coupling memory to on-chip CPU elements, are possible using imbedded memory elements of 256K bits
- wider data/clock busses and the integration of multiple large chips are possible with the advent of 500 leaded packages
- power dissipation is reduced and off-chip electrical performance improved by the use of lower power supply voltages, such as 3.3 volts
- smaller chip sizes and shorter interconnect lengths are possible by using up to four layers of metal for interconnect and power distribution
- interconnects are shortened by using multichip modules
- efficient test techniques evolve, resulting in reduced costs for chip testing and system testing

1.3.3 ASIC New Challenges

ASIC designers are faced with new challenges, such as

- handling clock frequencies greater than 50 MHz
- operating in an RF signal environment involving controlled impedance lines, shorter interconnect paths, and reduced logic level swings
- developing economical tests for 256 inputs and outputs
- handling power dissipations approaching 5 watts
- incorporating design-for-test techniques into the architecture
- improving simulation accuracy and managing skew problems

1.3.4 ASIC Design Methodology Evolution

As system clock frequencies increase, the intrinsic macro delay, as a percentage, decreases and the metal delay increases. See Figure 1.3. To account for this, changes in the design methodology occur. For example:

- layout moves toward being timing-driven as well as density/complexity-driven
- more time is spent integrating than designing
- more time is spent debugging than integrating
- physical design moves closer to the designer
- the need for a quick interactive cycle is required to tune designs or fix design errors
- multiple chip simulation and multiple technology simulations are required

1.3.5 ASIC Designer Needs

As ASIC capabilities are extended, the ASIC designer needs

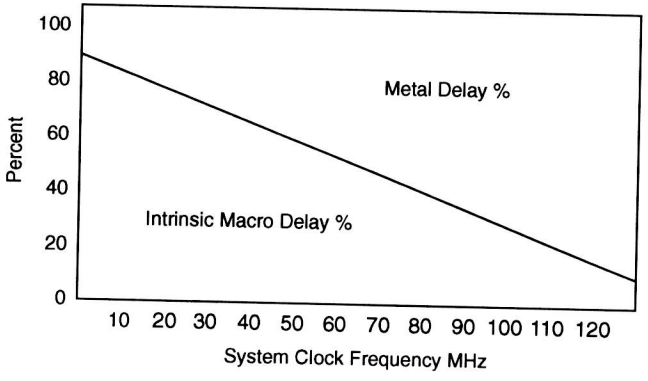

Figure 1.3 Delay vs. clock frequency.

- design tools to handle 2X to 5X the complexity of today's tools
- complete accuracy of the design process and methodology
- rapid cycle times for all project phases
- ability to reuse and upgrade designs
- more abstract front-end input
- flexibility of choice of ASIC technologies
- complete ASIC design data management

1.3.6 ASIC Vendor Requirements

In this new environment, ASIC vendors must be capable of providing

- a stable manufacturing environment
- customer support that is tightly coupled
- a clean set of tools and platform support that are not just ASIC vendor point solutions
- early access to the latest technology for silicon, packaging, and assembly
- a total solution to the customer's system requirements

More specifically, vendors need to create architectural and technology mappings in a structured environment. See Figure 1.4. For example, to

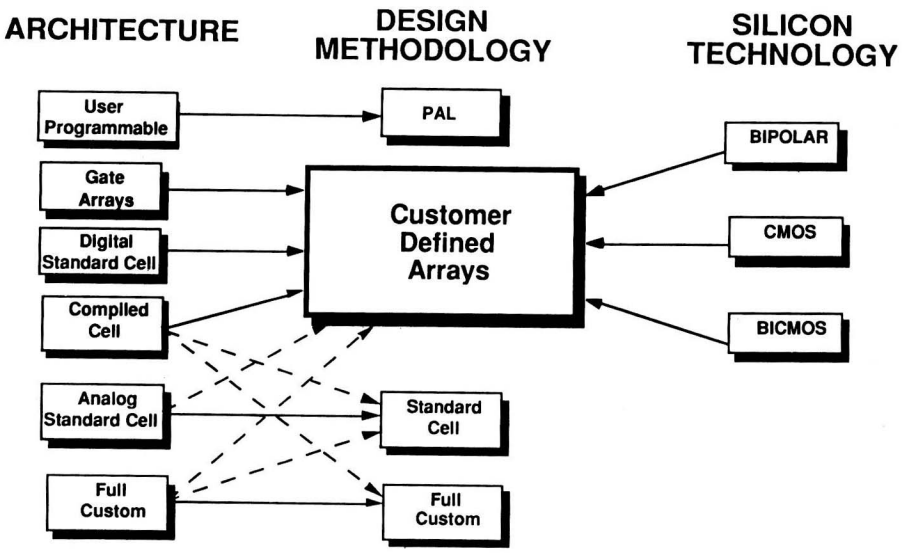

Figure 1.4 Customer-defined arrays.

satisfy a customer's needs, ASIC design methodology must be capable of handling programmable arrays, gate arrays, digital and analog standard cells, compiled cells, and full custom structures and then implementing them with CMOS, BiCMOS, or bipolar technology. In this way, sophisticated customers can create application-specific-based arrays that are optimized for performance and density.

1.3.7 ASIC Test Vector Development

As the complexity of integrated circuits increases, the problem of testing becomes increasingly difficult. If circuits are to be testable, test requirements must influence the design procedure. Testability should be added to the traditional aspects of design: performance, functionality, speed, power consumption, and reliability.

To emphasize the testing issue, this book starts out discussing design for testability (DFT). Design for testability is a design methodology that considers test requirements throughout the design cycle and incorporates features that permit thorough testing with minimum effort and maximum fault detection. Test vector development involves developing a designer's vectors that satisfy operational goals and also developing production test vectors that exercise the logic elements of the design without consideration for the circuit's use.

1.3.8 ASIC Technologies

There are two basic ASIC technologies discussed: ASIC CMOS arrays and ASIC ECL arrays. The CMOS arrays are high-density arrays built on a 1.0-micron drawn gate length (0.75 micron effective), triple-layer CMOS process. Designers can achieve over 75,000 usable gates on a channeless architecture having minimum chip dimensions and resulting in subnanosecond loaded gate performance. CMOS arrays are available in gate increments from 3000 to 105,000 gates. With a utilization factor of 75%, the arrays provide usable count gates of from 2000 to 75,000 gates. Triple-layer metal is used for metal routing and for power distribution. The typical gate delay is 250 picoseconds for a two-input NAND oxide isolated primary cell. The low power gate consumption is 6 microwatts/gate/MHz. The arrays have 5-V CMOS and TTL-compatible I/O options. I/O cells can be paralleled on chip for 48-mA drive capability.

The ECL arrays are high-density arrays built on a 1.0-micron process with four layers of metal. Gate utilizations of more than 80% are achievable. The periphery of the array is surrounded by 400 I/O cells that are either 10K or 100K compatible. There are 400 signal pads and 136 power pads surrounding the logic core. Each macrocell contains a combination of 25 resistor and NPN elements. The ECL circuit structures are implemented

with three-level series gating to improve the logic efficiency over to level series gate macrocells. To minimize signal deterioration when crossing the large chip, active driver circuits are implemented that boost speed by a factor of 5 for heavily loaded outputs. Gates in the array core feature typical unloaded propagation delays of 100 to 240 picoseconds depending on the power level chosen, 2 to 0.5 milliwatts/gate. Typical loaded delays (fanout = 3, 100 mils of interconnect) would range from 300 to 500 picoseconds for the power levels chosen. The base array includes 14,784 macrocells set up in an $X-Y$ matrix of 88 rows and 168 columns. Slave bias drivers are regularly spaced in the columns to minimize loading of the bias signal.

1.3.9 ASIC Packaging

A variety of packages are available for the ASIC arrays. They are plastic leaded chip carrier (PLCC), plastic quad flat packs (QFP), pin grid array (PGA), leaded chip carrier (LCC), ceramic quad flat pack (CQFP), and the tape automated bond process.

1.4 ORGANIZATION OF THE BOOK

This book has been planned with several needs in mind. First, this book does not need to be read from start to finish to make sense or be useful. Through an expanded index, a detailed glossary, a list of design principles, and tutorial material, designers can use the book as a working reference to the design process. The expanded index helps designers locate specific design topics; the detailed glossary helps designers to quickly understand the terminology used; the list of principles ensures easy access to the design modifications that need to be made; and the tutorial material provides additional design support information.

Second, the design principles and the tutorial material have been separated. This provides the designer a checklist of design principles for immediate use without having to sift through a lot of text material.

Third, this book can be used in a standard lecture course at the undergraduate and graduate levels. The focus of the text material and exercises is to improve the creative skills, problem-solving skills, and communication skills of the students.

Each chapter follows a similar format. First, the definitions are listed, because there is a language associated with the understanding of the material. The definitions are also listed in the glossary. Second, each chapter lists a set of design principles that make the ASIC design a reality the first time around. Each design principle is clearly stated, followed by an explanation and an appropriate example. Many figures are used in the examples. These figures should be extensively studied because it is not possible in a

book of this scope to explain every circuit in the same detail as an application note.

Chapter 2 is an introductory chapter that explains ASIC designs, ASIC flow diagrams, design cycles, and factory flows.

Chapter 3 is dedicated to ASIC testing. The object of ASIC design is to produce designs that meet specification and can also be tested using reasonable resources of equipment, time, and money.

Chapter 4 focuses on ASIC logic design. It is important to develop the right logic design technique. ASIC design libraries are more complex and ASIC speeds have increased significantly. With complex designs, it is important to eliminate all race conditions.

Chapter 5 discusses ASIC timing and delay principles. Today, the calculation of propagation delays and timing limits are performed by sophisticated computer programs. However, it is important for the ASIC designer to understand the methods and processes associated with these calculations in order to evaluate the results and make decisions about the resulting performance.

Chapter 6 covers ASIC clock distribution. The basis of ASIC synchronous design is the clock signal. The major problems in synchronous systems are to minimize race conditions and clocking skews.

Chapter 7 presents ASIC CMOS design principles. ASIC high-density CMOS arrays are usually presented as a family of arrays that offer a designer a wide selection of available gates. In order to use those arrays properly, certain design principles must be followed.

Chapter 8 is dedicated to ASIC ECL design. ECL arrays are very high-performance arrays. Degradation of performance due to capacitance, loading, and transmission line effects must be minimized. In order to use ECL arrays, certain design principles must be followed.

Chapter 9 focuses on ASIC packaging principles. ASIC arrays need a packaging environment that is fast and reliable. A proper package provides physical support for the array, provides signal and ground leads, removes the heat, and protects the array from the environment.

Chapter 10 discusses special topics related to ASIC design. The special topics are structured design review, CMOS Latchup, and handling ASIC array devices.

The appendixes contain a glossary, a list of design principles, a list of symbols, and several tutorial sections.

An extensive index, listing many design terms, is used so that this ASIC book can be used as a reference as well as a design textbook.

Finally, it should be noted that this book is meant to assist an ASIC user to achieve silicon on the first pass through a vendor's CAD system. This book does not deal with the vendor design of ASIC cells and macros. The designer (user) must remain in control of the design and make sure that a complete understanding of the design principles needed to achieve a correct design are understood.