HIGH-SPEED ANALOG-TO-DIGITAL CONVERSION

By MICHAEL J. DEMLER

High-Speed Analog-to-Digital Conversion

Michael J. Demler

Academic Press, Inc.
Harcourt Brace Jovanovich, Publishers
San Diego New York Boston London Sydney Tokyo Toronto

This book is printed on acid-free paper. ♾

Academic Press, Inc.
San Diego, California 92101

United Kingdom Edition published by
Academic Press Limited
24–28 Oval Road, London NW1 7DX

Library of Congress Cataloging-in-Publication Data

Demler, Michael J.
High-speed analog-to-digital conversion / Michael J. Demler.
p. cm.
Includes bibliographical references and index.
ISBN 0-12-209048-9
1. Analog-to-digital converters. I. Title.
TK78887.6.D46 1991
621.381'5322--dc20 90-49744
CIP

PRINTED IN THE UNITED STATES OF AMERICA
91 92 93 94 9 8 7 6 5 4 3 2 1

High-Speed Analog-to-Digital Conversion

////////////

This book is dedicated in loving memory of
my son Michael and to Mom, Dad, and Rosie
for all the years of support and encouragement.

Preface

This book focuses on techniques for the high-speed conversion of analog signals into digital code. Devices and circuits that perform this task of data conversion are generally referred to as A/Ds (analog-to-digital converters), while the complementary function of digital-to-analog conversion is performed by D/As. The primary goal of this book is to provide a reference for practicing engineers who are working with data converters and to assist them in the selection and application of high-speed A/Ds. The subject matter grew out of the author's own experience in the design of high-speed A/D integrated circuits and his extensive contact with the actual users of these devices.

Paralleling the more widely heralded advances in purely digital devices such as microprocessors and memory chips, A/Ds have quietly followed a similar evolution. From the early circuit boards assembled with discrete components, today's integrated circuit technology enables the fabrication of complete single-chip data acquisition systems containing tens of thousands of transistors and precision networks of resistors and capacitors. The complementary development of digital signal processor (DSP) technology has increased the use of A/Ds as the interface for the

acquisition and measurement of the many signals that exist in the real world as spectrums of analog waveforms.

The state of the art in A/Ds includes many different types of devices, but they can generally be grouped into three categories based on their architecture and performance: *high-resolution; high-speed,* or *flash;* and *subranging,* or *two-pass.*

High-resolution A/Ds are generally built using serial architectures that most often determine one bit at a time in a sequence of measurements. Examples of such devices include monolithic 16-bit devices and up to 22-bit hybrid components.

High-speed, or flash, A/D integrated circuits employ parallel techniques from which all the bits are determined simultaneously in a single measurement. Devices are now available that provide 8 bits of resolution at sampling rates as high as 500 megasamples per second and 10 bits of resolution at rates greater than 50 megasamples per second.

Subranging, or two-pass, A/Ds combine both serial and parallel techniques in order to extend high-speed performance to higher resolution than could be obtained with an entirely parallel approach. Examples of this architecture exist in hybrid devices providing up to 12 bits of resolution at 10 megasamples per second.

Although the label "high-speed" could be applied to an A/D in any of these categories as an indication of relative performance, it is not the intention of this book to engage in such competitive comparisons. The core of this book is based on the author's belief that the real breakthroughs in A/D speed are largely due to the rapid advances that have been made in flash converter technology. Unlike all other types of data converters, flash A/Ds are only practical in monolithic integrated circuit form. For designers of high-speed A/D systems, this book will provide vital information on the details of the parallel architectures that form flash A/Ds and also describe the subranging configurations that rely on flash A/Ds.

Although the main objective of this book is to aid in the application of A/D components and architectures where the highest possible conversion speed is required, design engineers need more than a circuit "cookbook" to build high-speed data conver-

ter systems. It is important to understand the internal structure of these devices because fundamental differences in technology and design eventually determine the proper choice for each application. Coverage of some of the details of the IC design and fundamental circuit theory is included in order to point out the salient features of the various types of A/Ds that are available. References are provided for those interested in exploring the fine points in more detail.

This book makes selection and application of A/Ds easier by breaking through the barriers created by specmanship and by conveying a clearer understanding of manufacturers' data sheets and the devices they represent. Every specification is intended to model the error sources that exist in real A/Ds. Rather than simply providing a list of definitions for the various parameters that are used, the mathematical derivation of these models is supplied. Without resorting to advanced mathematics purely to expound on theory, these derivations are intended to illustrate the underlying concepts in a manner that any engineer can follow. This background information is vital in order for designers to form direct comparisons where no single standard exists among the various manufacturers.

Chapter 1 sets a foundation for understanding A/Ds by reviewing the architectures that are most frequently utilized in the different categories of performance. This survey will assist the reader in identifying the type of A/Ds to consider for various applications.

Chapter 2 focuses on high-speed A/Ds by exploring the details of the functional blocks that make up flash A/Ds. The flash, or fully parallel, architecture provides the fastest possible technique for A/D conversion. Differences between the CMOS and bipolar implementations of flash A/Ds are emphasized.

Chapter 3 explains the purpose and importance of the various high-speed A/D specifications. A technical definition and derivation of each parameter will help the reader develop a clearer understanding of manufacturers' data sheets.

Chapter 4 describes the support circuits that are required to fully exploit the performance of flash A/Ds. Selection criteria are provided for ancillary ICs such as op-amps, buffers, and voltage

references. Tips are given for improving the performance of flash A/Ds through proper application of peripheral components.

Chapter 5 gives some examples of application circuits that utilize flash A/Ds and contains ideas on exploiting the flexibility of these devices as building blocks. Subranging techniques that extend high-speed conversion to higher resolution are also introduced.

Chapter 6 describes the testing methods that can be used to evaluate high-speed A/D performance. Techniques for engineering characterization as well as manufacturing test are discussed.

The bibliography provides an extensive list of references from the author's files that will allow the reader to explore some of the A/D conversion topics in more detail. This material from many different sources has contributed greatly to the author's expertise and includes the key contributions that have been made to the state of the art in A/D conversion.

Michael J. Demler

Contents

1 A/D Converter Architectures

There is no universal A/D that is best suited to all situations, but there should be an optimum approach to address the needs of each application. Misapplication of an A/D can occur when the objectives of the user of a certain device are inconsistent with those of its designer. To alleviate such problems, this chapter will provide an overview of the most popular architectures that are utilized to implement A/D converters. In block diagram format, functional descriptions will explain the key features of each type of A/D. By understanding the fundamental differences in the A/D types and the various advantages and disadvantages of each approach, the selection process can be refined to consider only those A/Ds that are likely to provide a good fit for the intended application.

Type I: Serial A/Ds

The common feature of all serial A/Ds is that they embody an algorithm which attempts to iteratively minimize the difference between the input signal and an analog approximation that is created proportional to some accurate reference source. In each comparison, or conversion cycle, at most 1 bit is determined and accumulated to form the final N-bit result. Said another way, the

signal passes at least N times through a set of the A/D's basic functional blocks in all serial converters. This does not necessarily imply that serial approaches cannot be used to provide high speed, however, as will be seen from the descriptions that follow. The serial-type A/Ds include the widest variety of performance of any architecture, since this category encompasses the slowest types and those with the lowest power as well as the highest resolution of any A/D architecture.

Ramp or Integrating A/Ds

The basic architecture of an integrating A/D is shown in Fig. 1-1. This example represents the dual-slope technique, which is predominantly used in low-speed applications such as panel meters and digital volt meters. In such cases the high accuracy that can be achieved with this approach is of primary importance.

For the dual-slope A/D, quantization of the input signal proceeds in three phases. In the first phase a feedback loop is closed around the analog signal path while the input is set to zero. This cycle performs an autozero function, since any residual

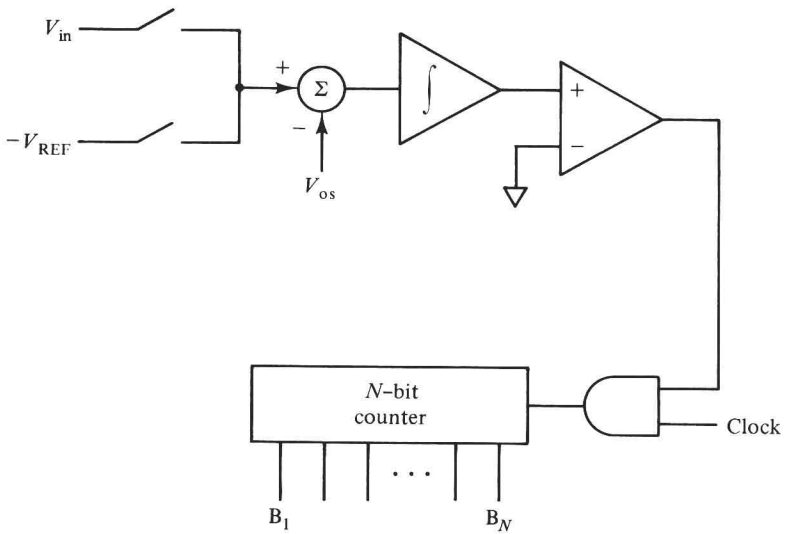

Figure 1-1 Architecture of dual-slope A/D converter.

errors in the signal path, such as offset in the integrator, are stored on a summing junction where they can be subtracted from the input.

In the second phase of conversion the analog signal is switched to the input of an integrator while the counter, which is cleared in the autozero phase, is allowed to count up to full scale. When the counter overflows, the integration of the input signal is stopped. Since a fixed number of clock cycles is always used (2^N for the N-bit counter), the charge accumulated on the integrating capacitor will be directly proportional to the amplitude of the input signal.

In the final phase of conversion an accurate reference voltage of opposite polarity to the analog signal is applied to the input of the integrator. The integration of this DC reference voltage will cause the integrator output to decrease linearly, as in the ramp shown in Fig. 1-2. During this interval the counter is again allowed to run up from zero. When the comparator input reaches the autozeroed level, where the conversion began, its output switches off the clock to the counter and terminates the conversion.

To illustrate how the quantized value of the input signal is obtained, the following equations describe the state of the integrator at the end of the conversion.

$$\int_0^{2^N \cdot T_{CLK}} v_{in}\, dt - \int_0^{T_c} V_{REF}\, dt = 0$$

$$\int_0^{2^N \cdot T_{CLK}} v_{in}\, dt = V_{REF} \cdot T_c$$

$$= V_{REF} \cdot \text{COUNT} \cdot T_{CLK}$$

For a DC input:

$$\frac{v_{in}}{V_{REF}} = \frac{\text{COUNT}}{2^N}$$

The high degree of accuracy in the quantization process results because, at least in this ideal case, the digital output is directly proportional to the integrated input signal. The final state of the

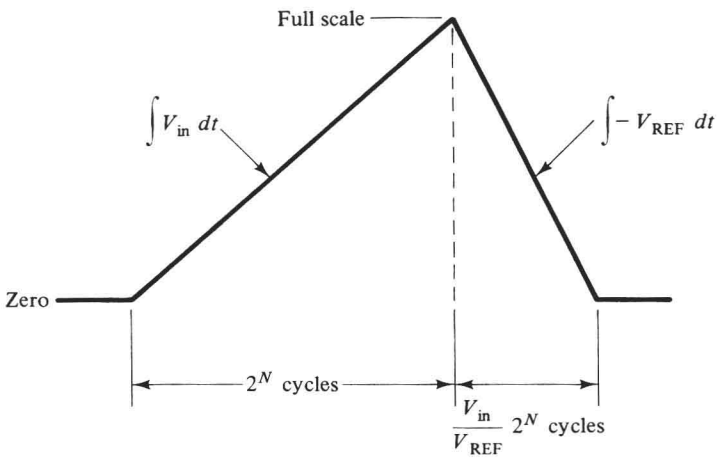

Figure 1-2 Dual-ramp conversion cycle.

counter depends only on the reference voltage and the degree to which the interval between clock pulses is constant. Very high stability reference circuits can be chosen, and it can also be assumed that clock instabilities will be insignificant over the duration of the conversion process. Accuracy of other components is not critical, since the reference and the input are both applied to the same signal path and autozeroing can be employed.

Limitations in the speed of this architecture are obviously associated with the number of bits in the counter. To digitize a full-scale signal (neglecting autozeroing time), 2^{N+1} clock cycles are necessary. The number of clock cycles doubles with each additional bit of resolution. One step that can be taken to speed up the process is to use a triple-ramp approach. In this technique two different rates of reference integration are employed. One counter can be used at higher speed for the coarse conversion to determine the MSBs, crossing over to a slower speed counter for the fine resolution required in the LSBs.

Delta-Sigma A/Ds

The delta-sigma (or sigma-delta) A/D is increasing in popularity for audio-band signal processing and low-frequency measurement applications. This is due to its ability to be easily integrated

on a chip that is predominantly made up of complex digital circuitry, without requiring more expensive precision analog components. There can also be speed advantages compared to other integrating architectures. A typical implementation is shown in Fig. 1-3.

Delta-sigma A/Ds are based on the translation of high-speed, low-resolution samples of a band-limited input signal into a higher resolution, lower speed digital output. Because of the high-speed sampling operation relative to the limited input frequency, this type of A/D is usually referred to as an "oversampling" architecture. It is often implemented in a CMOS (complementary metal oxide semiconductor) process which allows the signal processing blocks to be constructed using switched-capacitor sampled-data techniques. The input samples are summed in an integrator that feeds its output to a comparator, which can be considered a 1-bit A/D. The comparator makes decisions at the high-speed clock rate as to whether the integrator output is positive or negative. These decisions are then fed serially to a digital filter and also used to control a 1-bit D/A in the feedback loop, which outputs either +REF or −REF.

At first glance the delta-sigma A/D appears very similar to the previous integrating A/D. However, by applying feedback from

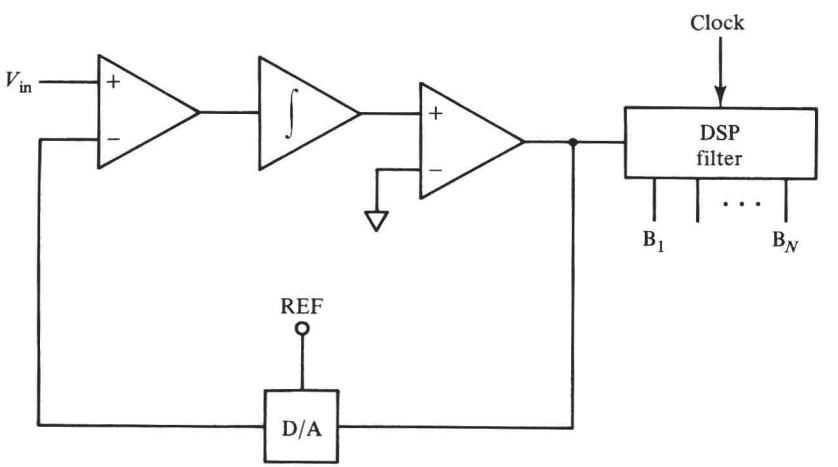

Figure 1-3 Architecture of a delta-sigma A/D.