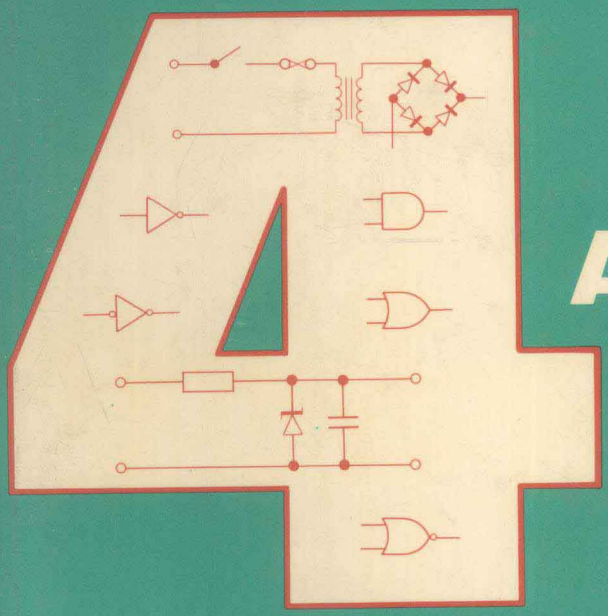
STUDY NOTES FOR TECHNICIANS

MICROPROCESSOR BASED SYSTEMS LEVELS 4 AND 5



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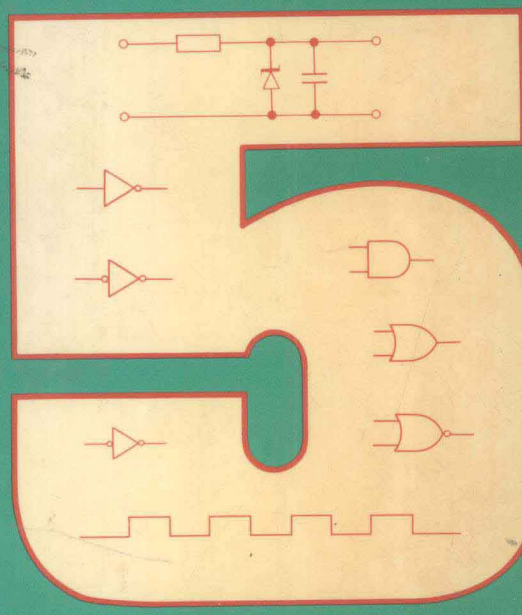

R.C.Holland

Study Notes for Technicians

Microprocessor Based Systems Levels 4 and 5

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McGRAW-HILL BOOK COMPANY (UK) LIMITED

London · New York · St Louis · San Francisco · Auckland · Bogotá
Guatemala · Hamburg · Johannesburg · Lisbon · Madrid · Mexico
Montreal · New Delhi · Panama · Paris · San Juan · São Paulo
Singapore · Sydney · Tokyo · Toronto

Published by
McGRAW-HILL Book Company (UK) Limited
MAIDENHEAD • BERKSHIRE • ENGLAND

British Library Cataloguing in Publication Data

Holland, R. C.
Study notes for technicians.
Microprocessor based systems levels 4 and 5
1. Electronic engineering
I Title
621.3 TK145

ISBN 0-07-084693-6

Library of Congress Cataloging in Publication Data

Holland, R. C.
Study notes for technicians.

(McGraw-Hill study notes for technicians series)
1. Microprocessors. 2. Microprocessors -Programming.
3. Microcomputers. I. Title. II. Series.
TK895.M5H65 1984 001.64'2 83-22174
ISBN 0-07-084693-6 (pbk.)

1234PB 843

Typeset by RDL Artset Ltd, Sutton, Surrey

Printed and bound in Great Britain by
Page Bros (Norwich) Ltd.

Preface

This book covers the syllabus of the TEC (Technician Education Council) units titled Microprocessor Based Systems 4 and 5. The book is the third in a series which is designed to support the levels 1 to 5 microelectronic and microprocessor systems units. However the work is intended to appeal also to a readership outside this TEC grouping and, if read in conjunction with the previous two books in the series, it should enable the reader to develop a detailed understanding of the subject of microelectronics and microcomputers. If it is read in isolation, then the reader should possess some previous knowledge of the subject.

The format used in the text is that applied generally in the McGraw-Hill Study Note series, viz. to introduce each topic with a description of principle, followed by a series of worked examples and a selection of exercises for the student to complete. Answers are given at the end of the book. The author's choice of examples and exercises is based upon extensive practical teaching of these microelectronic subjects.

Most circuit and programming examples use the Intel 8085 and the Zilog Z80 microprocessors. It is felt that an important element of simplicity would have been lost if the text had attempted to cover a wider range of microprocessors. Practical programming work on a microprocessor development system will augment the text and should give the reader a comprehensive understanding of the subject.

The author wishes to thank his family and colleagues for their support during the preparation of this book.

Other books in this series cover Microelectronic Systems levels 1 and 2 (the first book) and level 3 (the second book).

Contents

1 Microprocessor Systems

1.1 Microprocessors

Most microcomputer engineers and programmers have their favourite microprocessors. However, it is possible to make almost any microprocessor do any job, and so the choice of microprocessor for any particular application is normally determined by consideration of which device is available and is familiar to the user.

Sixteen-bit processors offer many advantages over 8-bit devices. However, the 8-bit processor or CPU (central processor unit) still dominates microcomputer applications. So much auxiliary circuitry and support software have been developed for the 8-bit devices that their bigger brothers have not yet upstaged them.

A comparison of microprocessors would be based upon the following typical benchmarks:

(a) Word length (8- or 16-bit normally)
(b) Facilities which are available within the instruction set (e.g., addressing modes, arithmetic functions)
(c) Speed of operation of a typical instruction
(d) Addressing range (i.e., number of memory locations that can be accessed)
(e) Input/output facilities (i.e., instructions for input and output of data, plus range of support chips for connection to external devices)

These features would have the implications shown in Fig. 1.1 in the standard three-block diagram of a microcomputer.

Subsidiary characteristics of microprocessors which are worthy of consideration are:

(a) Compatibility with other microprocessors, e.g., machine code programs for the Intel 8080 will also run on the Intel 8085 and the Zilog Z80
(b) Number of registers (the more the better)

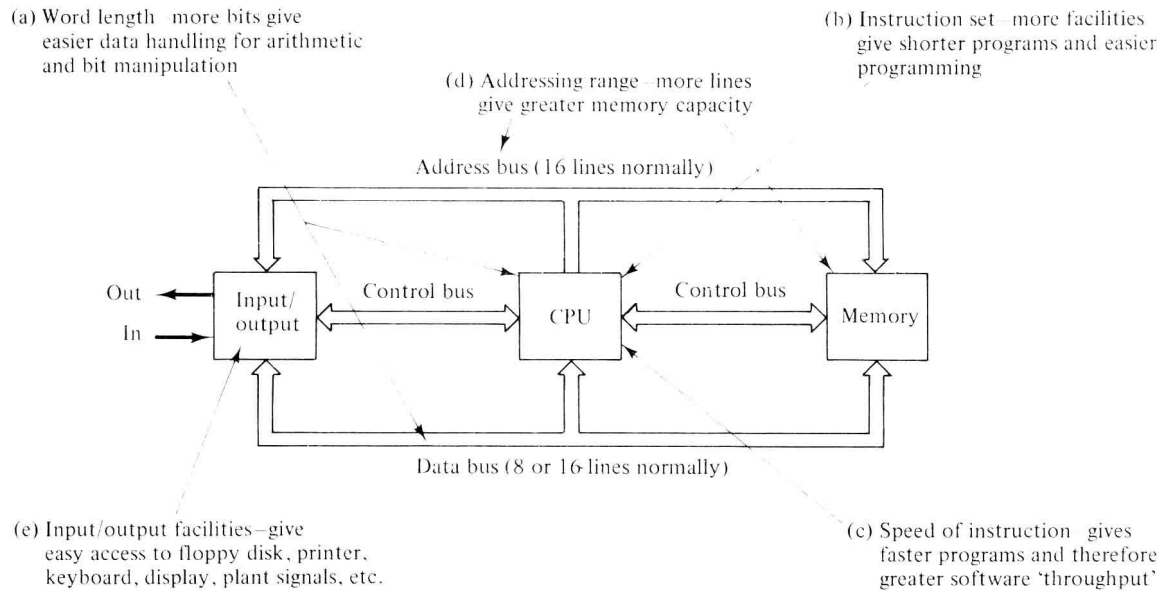


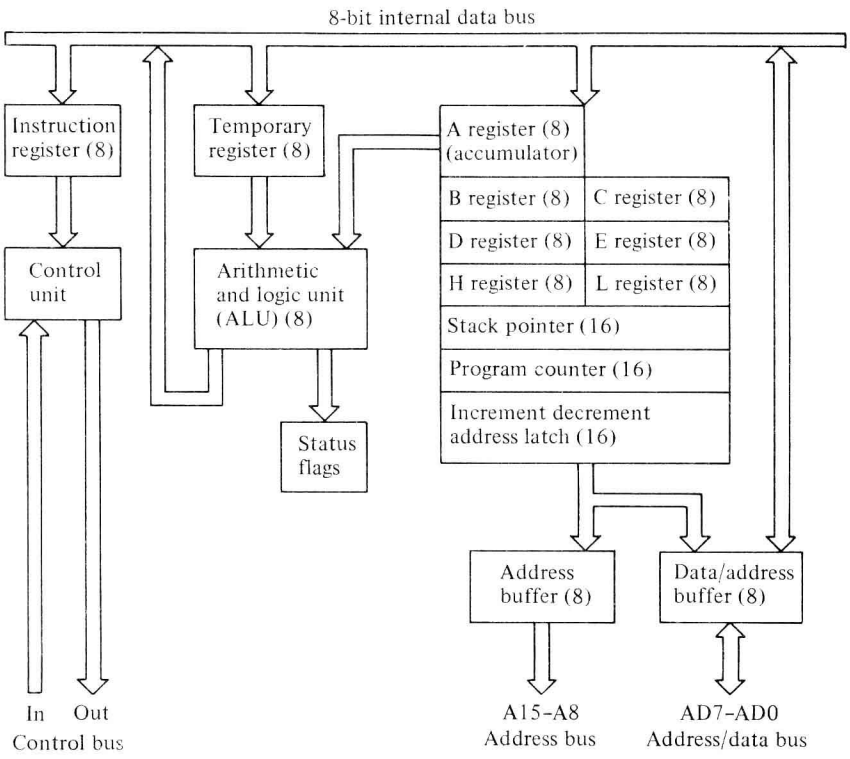
Figure 1.1 Influence of microprocessor features on microcomputer operation

(c) Number of interrupts
(d) Special interrupt facilities, e.g., the use of a new set of registers within an interrupt routine

Examples

1. Compare the main features of the Intel 8085 and the Zilog Z80 8-bit microprocessors.

Answer: Consider the following simplified drawing of the Intel 8085 CPU:

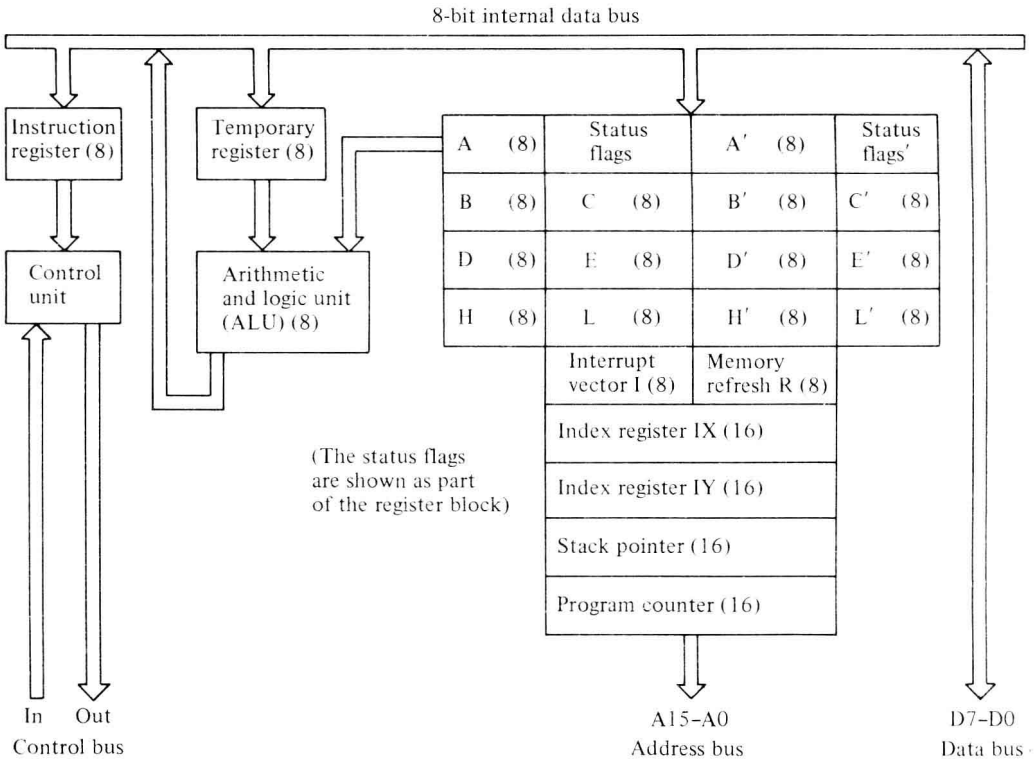


The Intel 8085 CPU

Notice the following features:

(a) The usual modules of ALU, control unit, instruction register, program counter, and stack pointer are present.
(b) There are seven work registers – A(accumulator), B, C, D, E, H, and L. They are all 8-bit registers, but the latter six can be used in pairs to provide 16-bit working for a small number of instructions.
(c) The address bus and data bus are multiplexed, i.e., the data bus and the least significant half of the address bus share the same pins. Thus demultiplexing must be provided external to the CPU.

Now consider the following simplified drawing of the Zilog Z80 CPU:



The Zilog Z80 CPU

The Z80 is an extension of the Intel 8080 and 8085 CPUs, i.e., it possesses all of the essential features of the other devices, plus the following:

(a) A duplicate set of work registers A to L is available. This is a benefit in an interrupt routine, which can switch to the second set of registers instead of saving all register contents on the stack.

(b) Two index registers give the facility of indexed addressing, i.e., an indexed instruction specifies an 8-bit displacement from a base address in IX or IY. This feature eases data table accessing.

(c) The interrupt vector I holds the top 8 bits of an indirect address; the interrupting device supplies the bottom 8 bits. Thus interrupt vectors (start

addresses of interrupt routines) can be specified by external logic. The Intel 8085 has a similar facility.

(d) The memory refresh register R is automatically incremented after each instruction 'fetch' operation. Thus dynamic RAM can be refreshed automatically.

(e) Additional instructions are available, e.g., a single block move instruction transfers a data block from any memory area to any other (or input/output port), a block compare (scan a block for a defined value) is available, individual register bits can be tested and altered, etc.

A comparison of the 8085 and Z80 CPUs is made in the following table:

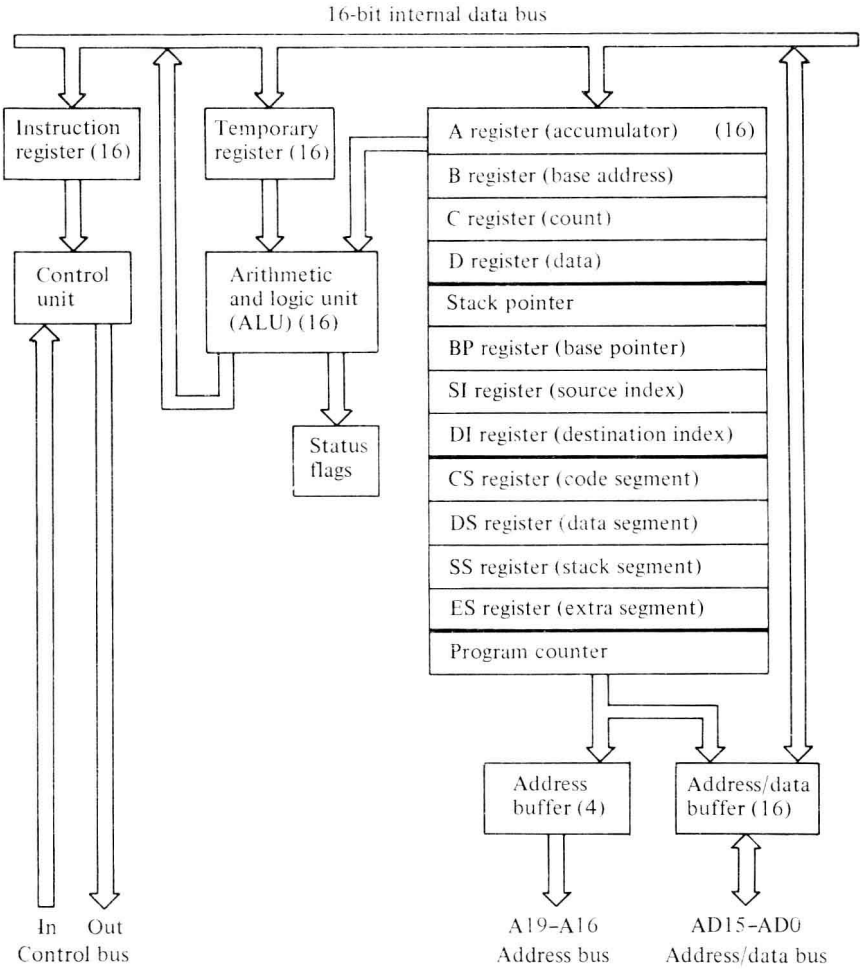
Feature	8085	Z80
(a) Word length (bits)	8	8
(b) Instructions (number)	113	158 (including extra addressing modes)
(c) Speed of instruction–add from memory (clock cycles)	7 = 3.5 μs for 2 MHz clock	7 = 3.5 μs for 2 MHz clock
(d) Addressing range	64K	64K
(e) Input/output	IN, OUT + single bit input/output	IN, OUT + extra addressing modes

This table shows a large number of common features. However, the Z80 does possess additional instructions, addressing modes, and other characteristics which may be attractive to the user. One anachronistic disadvantage of the Z80 may be considered to be the large and complicated array of instructions which are available. A newcomer to microcomputer programming is often somewhat bewildered by the complexity of this instruction set.

2. Compare the main features of the Intel 8086 and the Texas Instruments 9980A 16-bit microprocessors.

Answer: Sixteen-bit microprocessors offer significant advantages over 8-bit devices. In particular, arithmetic operations can be far more precise, e.g., numbers from −32 000 to +32 000 can be represented with 16 bits, while only 256 numbers can be represented in 8-bit microprocessors. Sixteen-bit devices also offer multiply and divide instructions. Additional addressing modes and more registers are available to make the programmer's job much easier.

Consider the following simplified drawing of the Intel 8086 CPU:

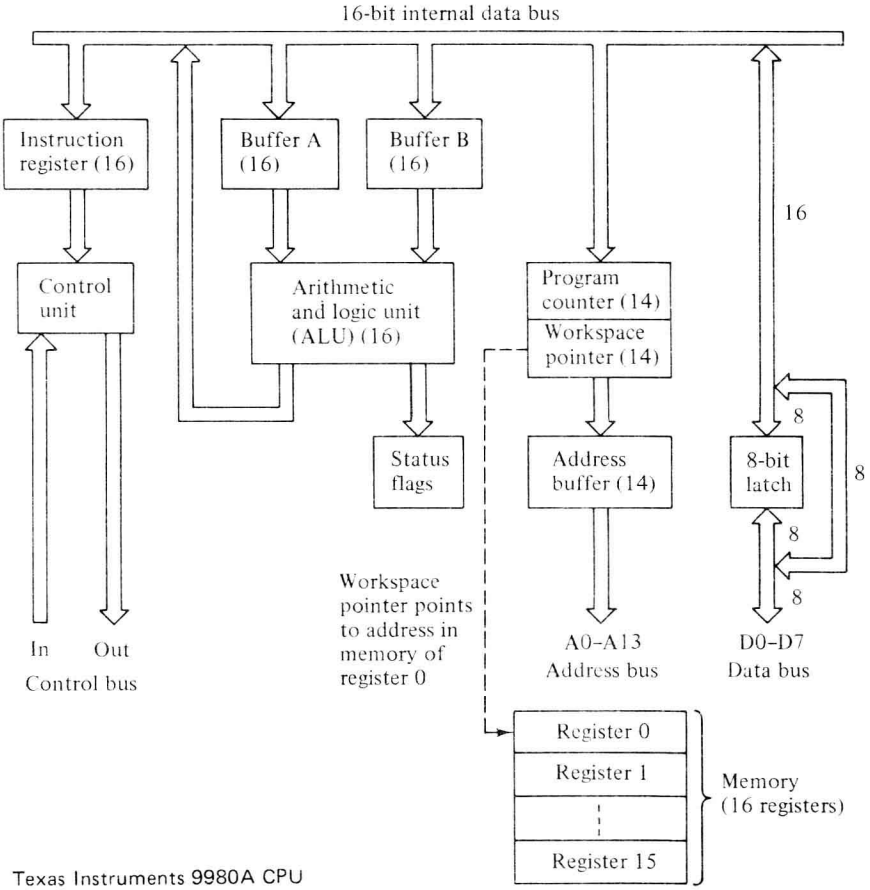


The Intel 8086 CPU

The register set is similar to the 8-bit 8085, except of course that all registers are 16 bits in length. The 8086 possesses three blocks of four registers. The first eight are all in effect accumulators, i.e., they can be used in most arithmetic and logic instructions. The last three of these eight are associated with base and indexed addressing, which are additional addressing modes to the 8085. The third group of four registers is associated with segment addressing, which is a variation of indexed addressing.

Notice that the data bus and 16 bits of the address bus connections are multiplexed, i.e., they share the same pins on the device. Thus external circuitry is required to separate them. The extra four address lines extend the address bus to a total of 20 address lines, which provide 1M byte addressing capacity.

Now consider the following simplified drawing of the Texas Instruments 9980A CPU:



Texas Instruments 9980A CPU

The Texas Instruments 9980A possesses *no* work registers in the CPU. They are held in the RAM part of memory and the CPU's workspace pointer holds the start address of the register block. While this does mean that instructions which use registers, i.e., the majority of instructions, possess relatively slow execution times, it does yield one big advantage. An interrupt routine, or even a subroutine, can use a new set of 16 registers, and this feature avoids the necessity to store away the contents of registers within the routine.

One limitation of this device is that only 14 address lines are used, i.e., the CPU can address only 16K locations. However, Texas Instruments offer another similar device in this range of microprocessors, the 64-pin 9900, which possesses a wider addressing range.

Sixteen-bit microprocessor designers were faced with a problem of deciding how to store 16-bit instructions and data items in memory, which is always 8 bits wide. The answer is clearly to store one word in two memory locations. The diagram of the 9980A shows how it handles data transfers in and out of the CPU by time-sharing 2 bytes using the 8-bit latch.

A comparison of the 8086 and 9980A CPUs is made in the following table:

Feature	8086	9980A
(a) Word length (bits)	16	16
(b) Instructions (number)	> 100	69
(c) Speed of instructions– fastest instruction (μs)	0.25 (8 MHz clock)	2.6 (8 MHz clock)
(d) Addressing range	1M byte	16K byte
(e) Input/output	Normal input and output	Similar, but with variable number of bits

This table shows that the 8086 offers several advantages over the 9980A (or the 9900), e.g., wider addressing range and faster speed. However, the Texas Instruments device possesses the novel feature of holding its work registers in RAM. This is beneficial when interrupt routines are used because these routines can simply switch to a new set of registers elsewhere in memory.

It must be stressed that there is often no best choice of microprocessor. Almost any CPU can be made to perform almost any function, although inefficiently. The main criterion which is considered when a choice of device is to be made is which device is available and is familiar to the user.

Exercises

1. What does the 'word length' of a microprocessor imply?

2. Why have 8-bit microprocessors not been replaced by 16-bit devices?

3. What is the word length of a microprocessor which possesses a 16-bit program counter, an 8-bit instruction register, and a 6-bit status register?

4. What is the memory addressing range of a microprocessor which possesses 18 address lines?

5. Name two microprocessors which share a degree of machine code compatibility.

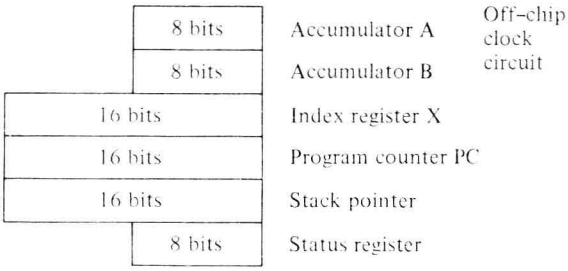
6. What advantage does a large number of addressing modes give?

7. State an advantage and a disadvantage of the use of a large instruction set.

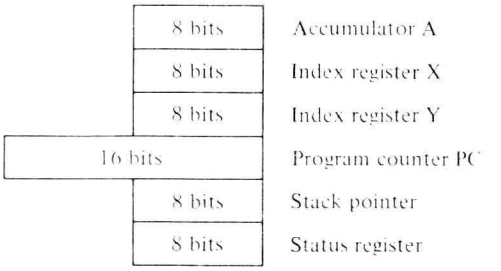
8. State five advantages of the Z80 microprocessor over the 8085.

9. The following diagrams indicate the registers which are available with two common 8-bit microprocessors:

(a) Motorola MC6800



(b) MOS Technology 6502



On-chip clock circuit
(needs only external crystal or RC circuit)

(Note: This latter device is used extensively in home computers, e.g., the BBC, Apple, and Commodore PET microcomputers.)

Both devices are 40-pin, possess 16 address lines, a similar number of instructions, and only 1 external interrupt line (apart from RESET and a non-maskable interrupt, which means that polling is necessary if several interrupts are handled by the external interrupt line). Both devices use memory-mapped input/output (i.e., memory read and write instructions are used for input/output transfers) and the 6502 alone possesses indirect addressing.

State two advantages which each device offers over the other. Would you express a clear preference for either device?

10. What is 'indexed' addressing?

11. What is the normal number range of a 16-bit microprocessor?

12. What is unusual about the 16-bit Texas Instruments 9980A microprocessor's registers, and what advantage does this offer?

13. Locate the manufacturer's data sheets for any microprocessor which is not discussed in this section; a magazine article is an alternative source of such information. Compare its operation and facilities with the devices which you have encountered in this text.

1.2 Complete microcomputer systems hardware

Complete microcomputer circuits are not difficult to design. Memory and input/output chips are connected in a straightforward way to the address and data busses to provide the required configuration.

Figure 1.2 shows a generalized schematic of a microcomputer which comprises a microprocessor, ROM, RAM, and input/output chips.

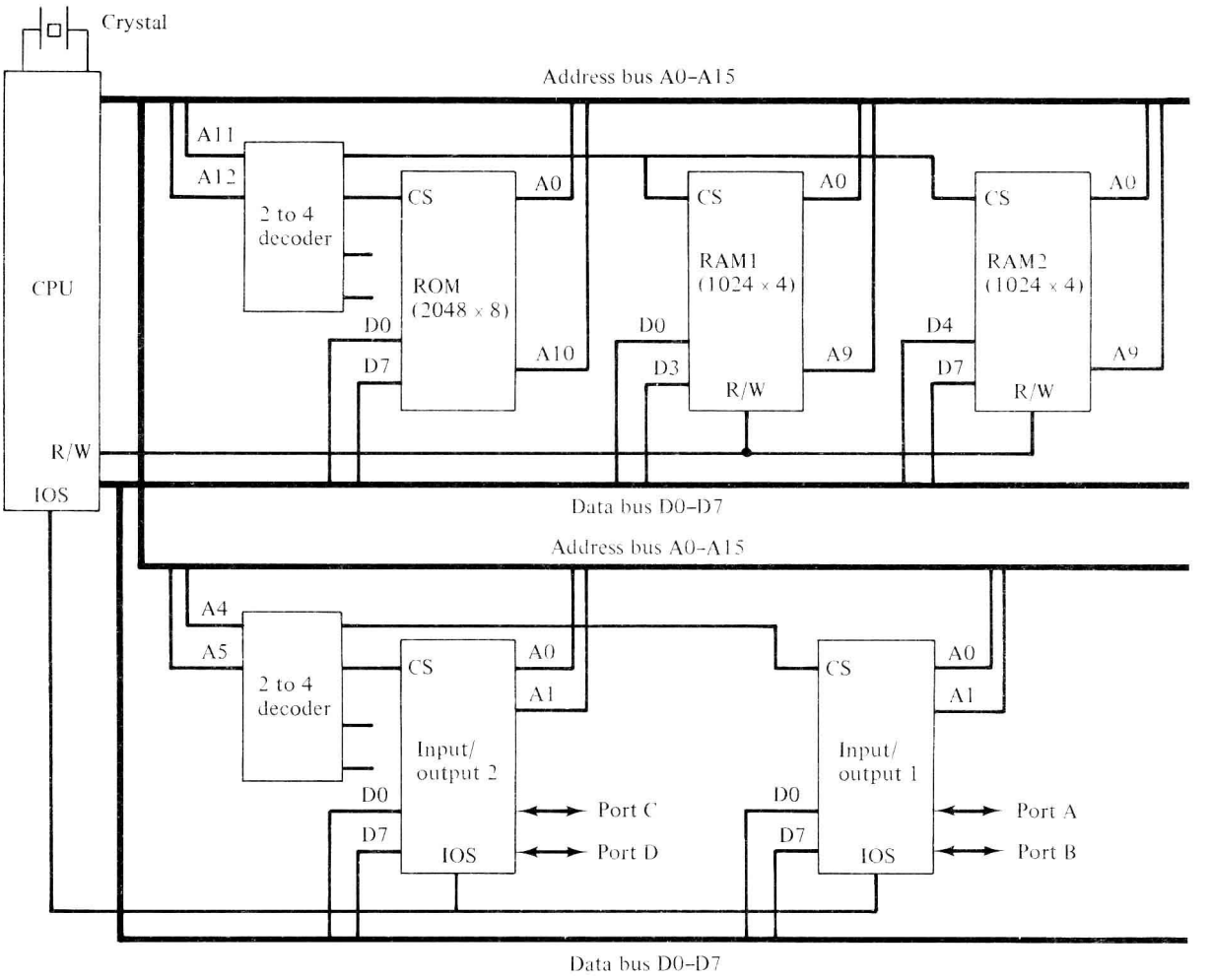


Figure 1.2 Generalized microcomputer schematic

Observe the following points:

(a) *CPU.* Only 2 of the 8 to 12 (typically) control bus lines, viz. R/W (read/write) and IOS (input/output selected) are shown. It is assumed that the missing signals which handle interrupts, DMA (direct memory access), clock outputs, etc., are not required in this configuration. The CPU is assumed to possess an on-chip clock circuit, i.e., connection to an external crystal only is required. The address and data busses are distributed throughout the additional circuitry in the normal manner.

(b) *Memory.* A single 2K ROM (2048 x 8 – 11 address lines give 2048 addresses) chip is used. Two 1024 x 4 static RAM chips combine to give 1K of RAM. Notice that the data bus is split between them so that each chip stores one half of each storage byte and that they share the same chip select and read/write signals.

(c) *Input/output.* Two identical two-port (i.e., 16 input/output signals) input/output chips are connected. Ports A, B, C, and D may be connected to remote devices such as a numerical segment display, manual keyboard, printer, VDU, etc. Notice that two address lines are connected to

each device to give a total of four address combinations in each case. These four addresses in the case of input/output chip 1 may be for:

(1) Port A
(2) Port B
(3) Timer circuit
(4) Control register to select ports A and B as input *or* output ports, i.e., the chip is 'programmable'

If only two addresses existed on the chip, e.g., if options (3) and (4) are not available, then only one address line is connected.

(d) *Address decoder.* Two decoder chips are required to generate the chip select signals for each memory and input/output device. Only one device can be selected at any time, of course.

Recall the truth table for a 2 to 4 decoder (Table 1.1). The top decoder generates chip select signals for memory as follows:

(1) RAM—when A12 and A11 are set to 00
i.e., address range of

```
A12 A11                A0
 0   0   XXX  XXXX XXXX
```

or base address of hex 0000 (all X's = 0)
end address of hex 07FF (all X's = 1)

(2) ROM—when A12 and A11 are set to 01
i.e., address range of

```
A12 A11                A0
 0   1   XXX  XXXX XXXX
```

or base address of hex 0800 (all X's = 0)
end address of hex 0FFF (all X's = 1)

Similarly, the bottom decoder generates chip selects for the input/output chips as follows:

(1) Input/output 1—when A5 and A4 are set to 00
i.e., address range of

```
A5A4  A1A0
 0 0  YYXX  (YY are irrelevant,
             say 00)
```

or Port A = hex 00 (XX = 00)
Port B = hex 01 (XX = 01)

(2) Input/output 2—when A5 and A4 are set to 01
i.e., address range of

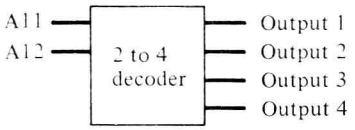
```
A5A4  A1A0
 0 1  YYXX  (YY are irrelevant,
             say 00)
```

or Port C = hex 10 (XX = 00)
Port D = hex 11 (XX = 01)

A circuit which is only slightly more complicated than this configuration is often all that is necessary for a straightforward application like a washing machine controller or a PLC (programmable logic controller—industrial sequence controller).

If large memory arrays or considerable input/output circuitry is required it is often necessary to mount the complete circuit on several PCBs (printed circuit boards). In this case bus drivers are commonly applied to enable the CPU bus signals sufficient electrical drive capability to feed along a backboard into large IC (integrated circuit) configurations. Drivers help to avoid timing problems which may occur due to pulse degradation when CPU signals are transmitted along extended paths to adjacent circuits or boards.

Table 1.1 Truth table for a 2 to 4 decoder



A12	A11	Output 4	Output 3	Output 2	Output 1
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

Examples

3. An Intel 8085 microprocessor multiplexes the data bus and one half of the address bus, i.e., these signals share the same CPU pins and must be split into separate signals for interconnection to memory and input/output chips. Show how specially designed memory and input/output support chips avoid the use of a de-multiplexing chip.

Answer: See Fig. 1.3. Notice the following features:

(a) AD0 to AD7 carries the multiplexed data bus and one half of the address bus. The signal ALE (address latch enable) is used by the CPU to signify

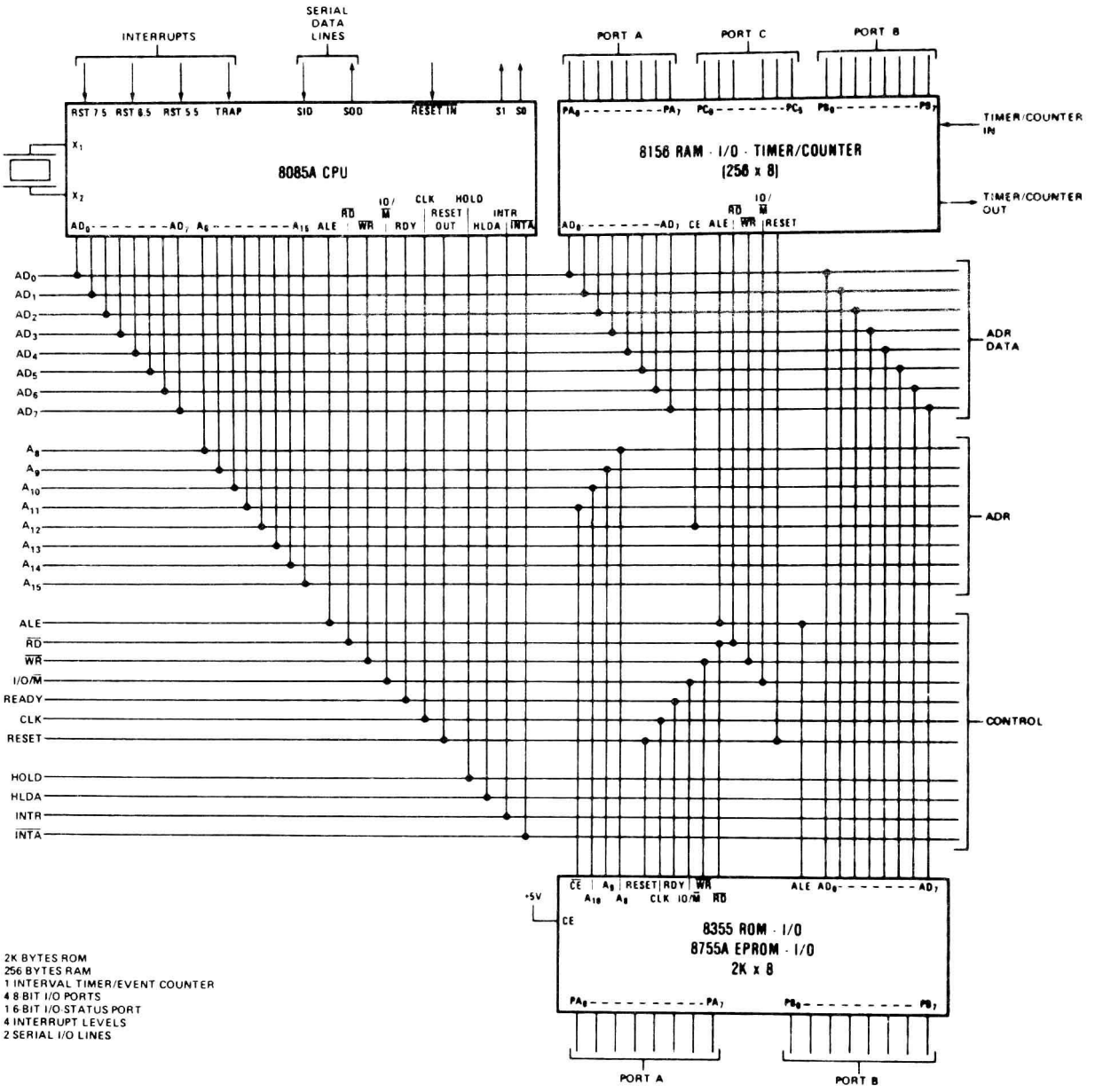


Figure 1.3 Simple Intel 8085 microcomputer configuration (*Courtesy of Intel Corporation*)