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Foreword

On behalf of the Executive and Technical Program Committees, welcome to the Eighth IEEE International Conference on Computer-Aided Design!

This year, the Digest of Technical Papers contains 124 papers from more than 20 countries. Four hundred and forty-two papers were submitted to the conference, which is a 5% increase over last year. To ensure the highest quality in the accepted papers, the program committee reviewed complete papers rather than abstracts and it also used a blind review process, in which the names and affiliations of the authors were removed from the papers prior to review.

The Technical Program Committee consists of 64 leading experts in the field of CAD divided into nine areas of interest: High-Level Simulation, Simulation, High-Level Synthesis, Logic Synthesis, Layout Verification and Analog Synthesis, Placement, Routing, Testing, and CAD Frameworks. The Committee has a strong international representation (at least one European and one Asian representative were present in each subcommittee).

In addition to the technical sessions, one panel and eight half-day-long tutorials have been included in the technical program of ICCAD-90. The half-day tutorials offer more flexibility to the CAD professionals interested in learning more about some of the hottest topics in CAD. We hope that many of you will take the opportunity of participating in one or more tutorials on Thursday.

This year we are experimenting with one-day registration to encourage a larger participation of CAD professionals. Daily breakfasts and lunches are provided to all conference attendees to encourage and promote professional interaction in a less formal setting. A cocktail party and a banquet are also provided in the conference registration fee. As last year, the banquet will feature a chamber music group and will have no invited speaker.

We are looking forward to another successful conference. Thank you for participating in another exciting ICCAD!

Alberto Sangiovanni-Vincentelli
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Technical Program Chair

Conference Committee

Conference Chair
Alberto Sangiovanni-Vincentelli
University of California
Department of EECS
515 Cory Hall
Berkeley, CA 94720
(415)642-4882

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C&C Research Laboratories
1-1 Miyazaki 4-Chome
Miyamae-ku, Kawasaki, 213
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Cupertino, CA
95014-2599
(408)285-5771

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ASIC Design Engineering Center
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Hyogo-Pref., 664 Japan
+81-727-84-7470

European Representative
Jochen Jess
Eindhoven University of
Technology
Den Dolech 2, Postbus 513
5600 MB Eindhoven
The Netherlands
+31-40-743353

Local Arrangements Chair
Min-Yu Hsueh
Cadence Design Systems, Inc.
555 River Oaks Parkway
San Jose, CA 95134
(408)944-7571

Conference Managers
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Marie R. Pistilli
MP Associates, Inc.
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Boulder, CO 80301
(303)530-4562

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Tutorial: Formal Verification of Hardware Designs

David Dill, Stanford University
P.A. Subrahmanyam, AT&T Bell Laboratories

Background: *Participants will get the most out of this tutorial if they are familiar with basic digital design and computer architecture, automata theory, and know a little bit of formal logic.*

Description: Hardware designs are becoming more and more difficult to debug using traditional methods: thinking hard, simulating, and constructing prototypes. This has become a major bottleneck in the process of getting a new product to market, so there is increasing interest in the alternative of formal verification of designs, where automatic or manual methods are used to prove that the design meets some specification. The state of the art is advancing rapidly in both theory and practice; it is on the verge of having a major impact on CAD for digital design.

Formal verification consists of many different subproblems that call for different solutions. We will examine systems from different viewpoints and levels of abstraction. In each case, we will emphasize questions such as: When is formal verification helpful? What methods are practical, or potentially practical? What problems remain to be solved? Specific methods that will be discussed are: theorem-proving, application of binary decision diagrams, and methods for verifying state-machine behavior. We will also discuss the interaction between formal verification and other aspects of CAD, such as synthesis and testability.

This course is directed at CAD developers who want to initiate or augment their own program in synthesis and verification, to CAD managers wishing to get a summary of the state of the art (including potential benefits), and to researchers in CAD wanting to probe the frontiers of the field.

Tutorial: Multi-Level Logic Synthesis

Robert K. Brayton, University of California, Berkeley

Background: *In this tutorial, we will survey the combinational logic synthesis techniques that have been established as having practical significance as well as some theoretical developments which we judge promising for the future. We will begin by exploring the role that multi-level logic synthesis plays in the transformation from a high-level description to layout.*

Description: The techniques to be presented can be classified into two groups; those used for decomposition of logic functions yielding a multi-level structure, and those which perform optimizations on this structure. The first group of algorithms include the algebraic methods which have been used in many commercial products and production code because of their speed and relative effectiveness.

Also included is the important area concerning restructuring for meeting timing constraints. The second group can be called don't care based methods since a common theme is the use of don't cares to achieve the optimizations. These methods include ones based on two-level minimization applied to the multi-level environment, but also techniques such as global flow, transduction, and ATPG-based methods.

The methods mentioned above are considered technology independent. These are usually followed by technology-dependent methods which do the final mapping of the optimized structure into a given library of available gates. These include rule-based methods, and technology mapping. We survey this area and include some recent techniques for optimally trading area for delay.

The tutorial should be appropriate for people who have some knowledge of digital logic design, who would like a more global perspective of this emerging and important field, or who are considering pursuing or assessing these topics in more depth later. Knowledge of testing, two-level minimization, combinatorial optimization techniques, timing analysis, and verification is useful but not necessary.

Tutorial: What's New in VLSI/CAD: A Manager's Crystal Ball

Alberto Sangiovanni-Vincentelli, University of California, Berkeley
A. Richard Newton, University of California, Berkeley

Background: *This tutorial is intended for CAD users, developers and managers. The only background required is a general familiarity with the CAD and IC industry.*

Description: In the past CAD development has often been driven by the requirements of technology. This is still true today, especially in the areas of high speed design, rapid prototyping, system design and packaging concerns. However, CAD, together with the increasing speed and interface sophistication of engineering workstations, is also driving the design of digital systems. This is especially the case in the increasing power and acceptance of different levels of synthesis. In this tutorial we survey the field of CAD and point out the new developments that may be drivers for design over the next 4 to 7 years. In addition we will survey upcoming technological advances which will, in turn, drive CAD development.

The tutorial will present sufficient technical detail to allow an appreciation of the upcoming developments and how they could impact the integrated circuit industry. The goal is to allow the participants to be able to access the literature quickly in order to make effective decisions for long range planning for both product development and acquisition.

Tutorial: Electrical Modeling of Chip and Package Interconnects

Albert E. Ruehli, IBM Corporation
Omar Wing, Columbia University

Background: *The electrical modeling and analysis of chip and package interconnects is becoming a key part in the design of a high performance digital system. This is because the interconnects may contribute more than fifty percent to the delay or cycle time of many high performance systems. The role of the interconnects will become even more important as the technologies are pushed to the limit where the transistor delays are reduced to the picosecond range. To deal with these issues many key electrical design problems must be solved, e.g., exact waveform and delay computations, coupled noise and excessive voltage drops in the voltage and ground wires due to the inductances.*

Description: In this tutorial we will introduce a set of techniques for the electrical design of such systems. Proven techniques will be given for the modeling of both two and three dimensional problems. The solutions are based on circuit analysis techniques wherever possible. This enables us to tie the interconnect models to an existing circuit analysis or simulation facility like SPICE. Techniques for resistance, capacitance and inductance computation are discussed and their application to the solution of realistic problems is considered. Both two and three dimensional models based on transmission line and partial element equivalent circuits are introduced. Many practical examples will be given.

Familiarity with circuit analysis concepts is necessary and some knowledge of electromagnetic field theory is desirable.

Tutorial: High-Level Synthesis

Raul Camposano, IBM Corporation
Michael McFarland, SJ, Boston College

Background: *High-level synthesis takes an algorithmic description of the behavior required of a digital system and produces a structure, including both data path and control, that implements the given behavior. In recent years an increasing number of researchers have been working on different aspects of high-level synthesis, and a few forward-looking companies have begun to explore its use in industry.*

Description: This tutorial consists of three parts. First we will give an overview of high-level synthesis, showing how it is divided into a set of distinct but interrelated tasks. These tasks are:

1) Specification and internal representation of the algorithm to be implemented
2) Source-level optimization, similar to compiler optimizations in software
3) Scheduling operations by assigning them to control steps
4) Creating the data path structure, including functional units, memory and interconnect
5) Assigning hardware modules to the data path elements
6) Generating a controller to drive the data path according to the schedule
7) Interfacing to logic synthesis and physical design tools to complete the design

There are three other tasks that support the preceding ones:

8) Partitioning the design
9) Estimating the cost of design alternatives
10) Supplying information on the library of available modules

Next we consider each of the tasks in detail. For each task we look at the problem to be solved, the trade-offs involved, the techniques that have been developed to solve it, and we give typical results obtained with these techniques.

Finally we look at some open problems, i.e., areas where more research is needed to make high-level synthesis practical. Participants should be familiar with the basics of digital system design, especially more complex systems such as computer systems. A basic knowledge of computer architecture should be sufficient.

Tutorial: Synthesis for Testability

Srinivas Devadas, MIT
Kurt Keutzer, AT&T Bell Laboratories

Background: *Some familiarity with basic testing concepts and with combinational logic optimization.*

Description: In the first part of this tutorial we explore the potential for logic synthesis to allow designers to more comprehensively test circuits while simultaneously diminishing their need for fault simulation and automatic test-pattern generation.

First we show how logic optimization procedures can be used to produce circuits that are completely testable for single stuck-at-faults. Testing for faults such as multiple stuck-at-faults, gate delay faults and path delay faults is a greater challenge, but we show how logic synthesis and optimization procedures can produce circuits that have high degrees of testability in these models as well. For each of these fault models we also discuss how test vectors can be produced as a by-product of the synthesis process and how vector minimization algorithms can be used in the place of fault simulation to reduce the size of the vector sets.

While the first part of the tutorial assumes that synthesis is complemented by traditional design for testability techniques such as scan design, in the second part of the tutorial we consider the difficult problem of synthesizing sequential circuits with high degrees of single stuck-at-fault coverage without incurring the area and performance penalty of scan registers. Here we show initial results at combining synthesis for testability approaches with register-transfer level automatic test-pattern generation to produce vector sets that give complete single stuck-at-fault coverage without the use of scan.

Tutorial: Sequential Synthesis

Gaetano Boriello, University of Washington
Fabio Somenzi, University of Colorado

Background: *Participants should have some background in switching and automata theory. Knowledge of logic synthesis techniques, as given by the morning tutorial, is also assumed.*

Description: This tutorial addresses the design of systems that can be conveniently represented as finite state machines (FSMs) or networks of FSMs. These systems include controllers and interface circuits and may be both synchronous and asynchronous. The techniques for the design, verification, and testing of such systems will be covered.

The techniques for lumped FSMs will be considered first. These include extraction of the FSM from a high-level description, state minimization, encoding, verification, and test pattern generation. A review of the problem of decomposing a FSM will then lead to consideration of networks of FSMs and the associated optimization techniques. Some of these techniques are based on the exploitation of don't care conditions arising from the limited controllability and observability of a machine embedded in a network. Other techniques for FSM optimization are based on retiming, the process of moving logic across latches to minimize cycle time. This process leads to a different state assignment based on timing requirements rather than area.

The design and synthesis of asynchronous FSMs will also be discussed with particular emphasis on techniques for self-timed machines. Asynchronous machines are found predominantly in interface logic and more recently in digital signal processing circuits. We will cover self-timed as well as fundamental mode synthesis methods and briefly discuss verification and testing issues.

Tutorial: Mixed Analog/Digital Simulation

Karem Sakallah, University of Michigan
Resve Saleh, University of Illinois

Background: *Mixed analog/digital simulators were introduced over ten years ago to complement circuit and logic simulators in the verification of VLSI circuits. By combining analog (electrical) and digital (logic) models in one simulation framework, mixed-mode simulators can succeed in verifying chips for which detailed electrical simulation is too expensive (unfeasible), and for which the accuracy of logic simulation is inadequate. The demand for mixed-mode simulation has accelerated over the past couple of years because of the rapid growth in the number of hybrid analog/digital chips in many application areas (automotive, telecommunication, etc.)*

Description: This tutorial covers the theory and application of mixed-mode simulation. We begin by introducing the concept of mixed analog/digital simulation and its applications, and provide the necessary theoretical background for the remaining discussion. Next, we describe the various algorithms for circuit-, logic- and switch-level timing simulation and their associated implementation issues. Mixed-mode interfacing issues such as signal mapping, event scheduling and feedback handling are addressed in the following section.

The tutorial concludes by looking at the available commercial and academic software for mixed-mode simulation, and addresses topics of future research. Participants should be familiar with the basics of modeling and simulation for at least one level mentioned above.

Panel Session: Plateaus and Dead Ends in CAD

Moderator: Kurt Keutzer - AT&T Bell Laboratories, Murray Hill

1 Plateaus in CAD

Many areas of CAD enjoy years of creative activity after which research in the area reaches a plateau. What are the areas? Here are two candidates - come cast your vote!

1.1 Debate 1: Is testing research at a plateau?

Critic: Alberto Sangiovanni-Vincentelli, Univ. of California, Berkeley

Defendant: Balaji Krishnamurthy, Tektronix, Inc.

1.2 Debate 2: Is circuit simulation research at a plateau?

Critic: Jacob White, MIT

Defendant: James Spoto, Cadence Design Systems, Inc.

2 Dead Ends in CAD

In other areas of CAD, research appears quite active, but has progress on the fundamental problems of the area ever been made or is the research at an impasse? Here's one candidate for a dead end - come join the debate!

2.1 Debate 3: Is high level synthesis research just a dead end?

Critic: Wayne Wolf, Princeton Univ.

Defendant: Raul Camposano, IBM Corp.

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